TF7
Electronics and On-Detector Processing

Part I: ASICs and front-end electronics

Christophe de la Taille (CNRS/IN2P3)
Valerio Re (INFN Pavia/Univ. Bergamo)

ECFA Detector R&D Roadmap Symposium of Task Force 7 Electronics and On-detector Processing, March 25, 2021

Scope

- Identify the grand challenges that will guide the R&D process on the medium-and long-term timescales, and define technology nodes broad enough to be used as the basis for creating R&D platforms.
- Allow concerted and efficient actions on the international scale addressing the technological challenges of future experiments while fostering an environment that stimulates innovation and collaboration with industry

(from the 2020 Update of the European Strategy for Particle Physics)

Scope

- The development of electronics in general and ASICs in particular will continue to play a very important role for all future experiments in HEP.
- These HEP developments will have to follow the microelectronics industry to smaller feature sizes in order to benefit from the increasing transistor density, the intrinsic high speed and the lower power consumption.
- Infrastructures at the HEP institutes for the design of complex mixed-mode CMOS ASICs have to be built up to match future challenges and emerging design and verification methods need to be explored.

Scope

- The radiation tolerance for the electronics required by future experiments, in particular those at hadron machines, is unique to applications in HEP and needs to be addressed in a common international effort
- Interconnection technologies, post processing and packaging will become essential for future high-density detectors.
- Access to these sophisticated technologies is often restricted to large size projects, and will benefit from a community-wide approach.

Inputs from questionnaires

- A lot of suggestions and stimulating ideas from our community, which will be addressed by the talks in this session and by the following discussion

- For ASICs and front-end electronics:

  Going to advanced CMOS nodes below 65 nm: better performance, bigger challenges (design tools and strategies, collaboration between institutes, recruitment of skilled designers,…)

  Integration of dissimilar technologies (sensor, front-end electronics, silicon photonics,…), CMOS sensors

- The next slides provide a selection of inputs from the questionnaires on the subject of on-detector electronics

Performance and new functionalities

- Better Time resolution (< 50ps) , spatial resolution, higher data rates (≥ 25Gbps serial links), on-chip data reduction, lower power
- Radiation hardness, low noise
- Processing of data for selection & sparse readout (Pre-trigger logic).
- Fast and compact ADCs (more bits) and TDCs.
- Compact and very reliable large bandwidth data transmitters and slow control adapters on single chips
- Compact, flexible and very reliable power management
- Electro-optical and opto-electrical conversion

Which CMOS technologies?

- 65nm and 28nm would seem sensible to target. 28nm is likely to be a must have for timing and data aggregation & transmission.
- Two technologies seems reasonable; an expensive option for 'high-end' requirements and a cheaper alternative for less-demanding applications.
- immediate need to implement much more advanced silicon CMOS technologies, with nodes in the range 28nm -14nm, in the experiment upgrades during the following 5-10 years.
- energy saving is the hallmark of the newest technology nodes, such as the 7 nm of TSMC

Design strategies, verification, testing

- Design of complex readout chips: verification and testing by specialized teams (independent from designers)

- Synthesize automatic circuits that include analog circuits. AI algorithms that can utilize the experience and know-how of circuit designers will be required

- Pushing more intelligence to the front-end?

A) Add more programmability and data processing to avoid shipping out useless data and minimize power dissipation.

B) would be a very bad idea. Data should be forwarded to the off-detector electronics as early as possible and with only simple pre-processing (more flexibility and less problems wuth radiation in off-detector electronics)

Front-end ASICs and FPGAs

- bring FPGAs as close as to the FE ASICs for local triggering purpose. We don't think ASICs could beat the FPGA flexibility. ASICs would be there for the analogue amplification (if any) and to digitize the detector signals as fast as possible, FPGAs wuld do the processing
- *Integrate part of the FPGA in the frontend ASIC.*

Microelectronics and CMOS sensors

- CMOS sensors rely on CIS technologies with an epitaxial layer and charge collection performance is a crucial criterion in the final choice.
- Thus, the foundry should be available to exchange process information and be open to possible adjustments.
- 2 or 3 foundries with which to develop contacts; a 28 nm CIS could be investigated in the near future.
- CMOS sensor are well suited for 3D IC. A pioneering development happened 10 years ago in HEP. The crucial point for developing such a technology is having a reliable and constant access to a cooperative foundry

Interconnection, integration of dissimilar technologies

- Hybrid or monolithic integration of electronics and photonics for data transmission at very high rate (trade off between bandwidth, power, radiation hardness)

- R&D in TSVs, ACF, and bumpless is important for our detector developments, it should become a standard technology like bump-bonding.

Organization and teams

- Microelectronics organization should follow what was done for computing decades ago : CERN as TIER0 and large national labs as TIER1s. The national TIER1s could supervise more exploratory work done in TIER2s.
- A high level of specialisation which can not be maintained and developed on an individual basis: such expertise can only develop in teams with a critical mass of people
- University/institute teams to specialise and come together to work on different aspects of a single project
- More powerful&memory computers are needed to simulate completely (post-layout) complex chips
- Cooperation like CERN-TSMC-Universities extended to develop together more complex SoC chips. Solve problems with licenses (e.g. Cadence) and workout effective model of sharing designs.

Labor

- Ensure long term specialized staff positions and transfer of know-how.
- Reduce primary dependency on early career young people on design effort.
- Attract specialists with an Electronics Engineering background.
- Subcontracting should be used more and people should adapt to using it. This can cover many aspects such as IC building-block design, PCB design, firmware, production testing and quality assurance.

ASICs and front-end electronics: talks and discussion

- In the zoom Q&A window you may ask questions and write comments, that will be addressed during the discussion sessions
- Collaborative issues will be kept for the open discussion at 4pm

09:20 → 09:35 **Part A Introduction: ASICs and front-end electronics** 15m

Covering scope and summary of inputs

Speaker: Valerio Re (Universita and INFN (IT))

09:35 → 10:05 **Keynote talk: Future trends, challenges and opportunities in ASICs for HEP: a birds-eye view** 30m

Speaker: Angelo Rivetti (INFN - National Institute for Nuclear Physics)

10:05 → 10:15 **Topical invited talk: Moving to leading-edge technology nodes** 10m

Speaker: Federico Faccio (CERN)

10:15 → 10:25 **Topical invited talk: 3D integration** 10m

Speaker: Christophe Wyon (CEA French Alternative Energies and Atomic Energy Com)

10:25 → 10:35 **Topical invited talk: Perspectives on future development (TBC)** 10m

Speaker: Erik Heijne (Czech Technical University in Prague (CZ))

10:35 → 11:05 **Comments and brief discussion** 30m

Identifying points to take to afternoon discussion

Speaker: Christophe De La Taille (OMEGA (FR))