ECFA

European Committee for Future Accelerators

Feedback from the community – survey responses

Links, powering and packaging

Francois Vasey, Marc Weber

We received a wealth of responses

Many of them by groups or institutes

Many thanks!

The slides below are the distilled summary of the comments you sent

Link and general requirements

- There is consensus that the number of electronic channels and the data bandwidth will continue to increase

  Timing information, e.g., might add substantially to data volume per channel

- Quantitative estimates on pixel number and required bandwidths are difficult and experiment-dependent

Two schools of thought:

- triggers and data reduction/aggregation on detector will still be needed
- want to go trigger-less

High-throughput data links are key. Robustness and costs will drive design choices

Link technologies

- Very radiation-hard optical links
- Silicon photonics
- Tight integration of front-end ASIC and photonic drivers
- 3D technology to link electric driver to silicon photonic device

- More complex keying schemes and/or wavelength division multiplexing to increase bandwidth/fiber
- For many applications 10 Gb/s links driven by 65 nm CMOS may do – provided they can be made lower power and low cost;
  25-50 Gb/s or more will be preferable elsewhere
- Forward error correction

Link technologies (cont.)

- Balance higher bandwidth/fiber and local data aggregation versus more, cheaper and less power-hungry links
- Similarly, have two variants of transceivers: a flexible low-speed and a less flexible high-speed variant
- Machine learning intelligence at on-detector concentrator / aggregator nodes

- For the back-end, must closely follow industry standards and match front-end
- Reliable optical connectors
- Bi-directional optical fibers
- wireless links or free space optics (in dense areas or to connect tracking layers)

Powering requirements

- Will have to cope with large currents at very low voltages
- Regulators and converters need to be robust, radiation-hard, low-noise, functional in magnetic fields, „small“ and coolable
- Likely a (large) range of different voltages will have to be supplied

Powering will remain a key challenge relying on dedicated know-how and specialized technologies

Powering technologies

- DC-DC conversion remains important; needs to be pushed further to cope with new environments
- Galvanic isolation
- Serial powering for systems with severe material budget constraints
- Powering systems should be compatible with 48V industry standard
- Power management (e.g. power pulsing)
- Constant-current charging stages
- GaN technology offers intrinsicly good radiation tolerance and low on-resistance

Powering technologies (cont.)

- Sophisticated powering control and monitoring systems
- Cooling schemes and interfaces for converters/regulators

- Power over fiber
- Batterie power or wireless chargers for low-power loads or for very clean supplies e.g. for HV
- Radiation-hard switches for HV lines

Interconnect requirements

- Enable very low-mass designs for modules and hybrids
- Simplify module designs
- Minimize costs and facilitate mass production
- Cooling will be ever more important

Interconnect R&D might well be more expensive than links or power. Access to vendors is critical.

Interconnect technologies

- Micro-channel cooling for very high-speed and low-mass sensors
- Connectors to in-silicon cooling channels
- Etching techniques for micro channels and top layer sealing deposition to avoid wafer-to-wafer bonding
- Cooling at very low temperatures of e.g. -60 ºC

- Stitching to obtain large area silicon sensors
- Redistribution layers
- Tiling and 4-sides buttability

Interconnect technologies (cont.)

- Low-cost bonding techniques like laser soldering
- Flip-chip technologies and 3D chip stacking

- Alternatives to fine-pitch bumping technologies: through-silicon vias (TSV), anisotropic conductive film (ACF)
- TSV and interconnects between microelectronics and e.g. photonic chips

- Embedded passives in rigid (and flexible) printed-circuit boards
- Access to plastic packaging of chips
- Aluminium flexible circuits for minimum mass
- Miniaturized connectors, maybe with integrated high-speed data, power and slow-control links

Other comments

- Watch electromagnetic interference issues
- Establish grounding policies
- Define maximum tolerable thresholds for noise emissions
- Define minimum noise immunity

Possible focus points for R&D

- Radiation-hard optical links
- Silicon photonics
- Co-packaging electronics and optics components
- Wireless links

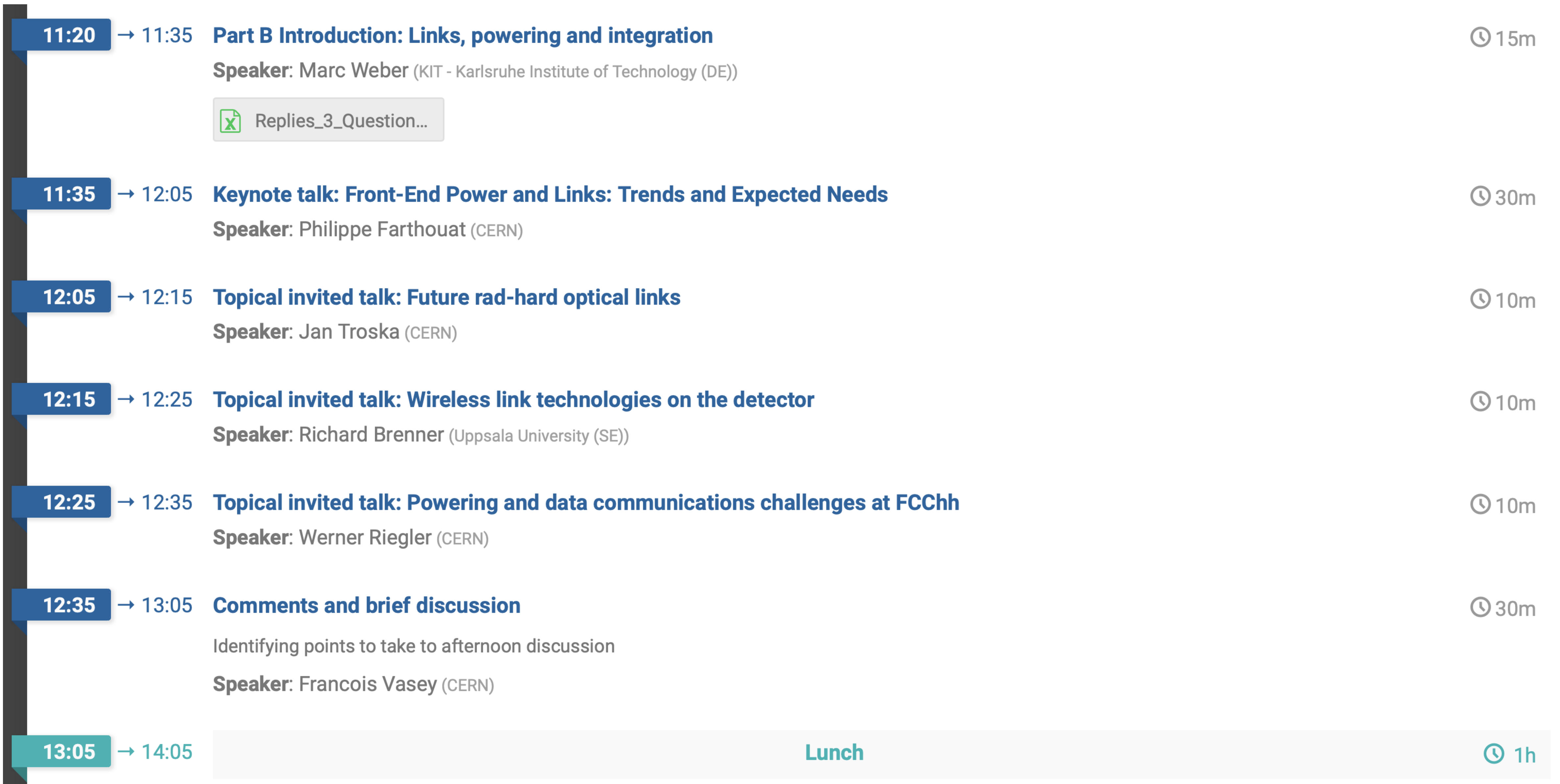
- Power distribution
- All stages of DC-DC converters (input stage with large conversion ratio and on-chip power management)
- Availability of powering know-how and technologies (for DC-DC and serial powering)
- GaN technology

Possible focus points (cont.)

- Power over data links

- Advanced packaging solutions and high-density interconnects
- Scaling to large-size stitched and tiled assemblies
- Cooling techniques for very high-density electronics

Any novel technology not yet tested in extreme radiation and noisy environments e.g. wireless


11:20 → 11:35
Part B Introduction: Links, powering and integration
15m
Speaker: Marc Weber (KIT - Karlsruhe Institute of Technology (DE))
Replies_3_Question...
11:35 → 12:05
Keynote talk: Front-End Power and Links: Trends and Expected Needs
30m
Speaker: Philippe Farthouat (CERN)
12:05 → 12:15
Topical invited talk: Future rad-hard optical links
10m
Speaker: Jan Troska (CERN)
12:15 → 12:25
Topical invited talk: Wireless link technologies on the detector
10m
Speaker: Richard Brenner (Uppsala University (SE))
12:25 → 12:35
Topical invited talk: Powering and data communications challenges at FCChh
10m
Speaker: Werner Riegler (CERN)
12:35 → 13:05
Comments and brief discussion
30m
Identifying points to take to afternoon discussion
Speaker: Francois Vasey (CERN)
13:05 → 14:05
Lunch
1h

Thank you!