On&Off detector processing

Dave Newbold (STFC) & Niko Neufeld (CERN)

A community-driven project

- Thanks to everybody who took the time to answer to the questionnaire
- This talk tries to summarise the Off-detector part based on what was received until the beginning of this week
- Your opportunity for input does not stop here – the panel is most grateful for any input

Challenges for FPGAs on the Front-ends

- 17 replies
  - In general getting processing & intelligence to the front-end reduces complexity downstream and data-transport needs (power!)
- Main challenges:
  - **Power dissipation**
  - **Radiation** (where applicable)
  - Radiation tolerance difficult to assess (closed IPs, black-box hardware) and auxiliary chips
  - All the complexity challenges for FPGAs on the back-end get worse on the front-end
- Potential for concerted (ECFA) R&D: FPGA technology as such is industry driven; **however R&D needed for questions of radiation tolerance (testing, IP design techniques)**
  - **Cooling issues very important → see later**

COTS elements other than FPGA

- 15 replies
- Main challenges:
  - complexity and cost of ASIC design make it unattractive to use *custom*-ASICs in the back-end
  - Machine Learning ASICs & SOCs (taken to be a FPGA/CPU combination in a chip) for the back-end, for the front-end if no radiation and power permitting
  - SoCs (in the sense o FPGA/CPU combinations) for complex intelligence, as chipset with the ASIC (but again radiation where applicable is/will be a concern), cooling
- Potential for R&D: ?

High Power elements

- 12 replies
- Main challenges:
  - **Power dissipation will be a very critical issue,**
  - Micro-channel cooling
  - Low-power design attitude ”do what you must” vs “do what you can” , power issues must be considered early on
  - Crate standards for back-end (xTCA)
- Potential for R&D: micro-channel cooling, low-power design blocks /rules, participation in standardisation process for electronics infrastructure

Design & testing, circuit boards

- 9 replies
- Main challenges:
  - Signal integrity & speed
  - Component density
  - Complexity, adoption of industry methods, organization of large, distributed design teams
  - See collaboration with industry, co-design?
- Potential for R&D: not really for R&D but for community education and industry collaboration

Links and data aggreagation

- 9 replies
- Main challenges:
  - Choice of speeds / link technologies might become more restricted due to optical co-packaging in the future
  - Fast links require aggregation on “big”, relatively low-rate detectors
  - Interoperatbility with commmercial networks
- Potential for R&D: interoperability with indstry standard protocols (Ethernet, maybe PCIe)

Timing & Synchronisation

- 11 replies
- Main challenges:
  - Asynchronous r/o: Bandwidth needed for time-stamps, high precision clock distribution
  - Synchronous r/o: very stable clock distribution, frequency ranges very narrow and in the future unlikely that commercially required standards are compatible with multiples of bunch-crossing frequency
- Potential for R&D:
  - For both approaches, ultra-fine phase monitoring and compensation - required at back-end
  - Asynchronous: rad-hard DDS and RF components, very stable local osciallators, extension of white-rabbit to rad-hard
  - Synchronous: Fixed and deterministic super-clean PLLs, can probably not be sourced comercially
  - Extend the use of White-rabbit

Control & Monitoring in harsh environemnts

- 6 replies
- Main challenges:
  - Tradeoff between complexity and reliabiliy, errror-correction
  - Component replacement
- Potential for R&D
  - No clear directions / to be checked with other fields (space, nuclear industry)

Software for Control & Monitoring

- 6 replies
- Main challenges:
  - Fast deployment,
  - CI & CD
  - Uniformity and long-term maintenance
- Potential for R&D: ?

Intelligence on the Front-end

- 15 replies
- Main challenges:
  - Simplicity of design vs data-rate (which entails high power-consumption)
  - Distribution of intelligence (FE least popular, concentrator – “mid-town”, or back-end)?
  - Can AI be of use and how to get this onto the FE in a radiation environment
- Potential for R&D
  - ”simple, low-power functions” e.g. clustering?

Soft- and firmware management

- 11 replies
- Main challenges:
  - Adopting industry policies
  - Manage scarce human resources
  - *Standardisation* – how to fight ”NIH”
- Potential for R&D
  - Training…

Verification and long-term maintenance

- 13 replies
- Main challenges:
  - Human resources for additonal development of e.g. unit tests is scarce
  - Add self-test features
  - *Standardisation*
- Potential for R&D ?

Reduce cost for off-detector electronics

- 13 replies
- Main challenges:
  - Get more uniformity and genericity by common projects, requiring large cross-insitute teams, while ensuring funding
  - Get rid of back-end by moving processing partially up (to the FE) / partially down to the software filtering and readout using a standard protocol (== Ethernet).
  - *Standardisation*
  - *Modular, open designs*
  - Add more “system-engineering”
- Potential for R&D
  - Prototype of Ethernet based front-end

Which R&D do we think we need to do?

- Radiation hardness of FPGAs (and potentially other ASICs/SOCs) for use in detectors which need it
- Low-power design techniques and advanced cooling techniques (micro-channels)
- (Rad-hard) components for extremely precise timing and clock distribution
- Instudstry standard compatible protocol from the front-end
- ???

How do we think we need to get organized?

- We need more standardisation and have to avoid reinventing the wheel (badly)
- This needs to be compatible with having expertise, responsibility and credit spread over multiple institutes → can we learn lessons from the “Grid”?
- Large, distributed, long-lived projects like in software
  - Longevitiy incentivizes adotpion because of lower risk
- At the same need to remain open for new, off-mainstream ideas
- Open and modular designs need maintenance and a repository and an active community around them (like in software)

Your contributions are vital!

- ***Please put your comments, questions into the Zoom Q&A Window***
- We will then pick them up during the discussion session

14:05 → 14:20	**Part C Introduction: Off-detector systems** **Speaker**: Niko Neufeld (CERN)	15m	
14:20 → 14:50	**Keynote talk: DAQ and Trigger Beyond HL-LHC** **Speaker**: Dr Emilio Meschi (CERN)	30m	
14:50 → 15:00	**Topical invited talk: Challenges of large software-oriented TDAQ systems** **Speaker**: Dr Alessandro Thea (Rutherford Appleton Laboratory (GB))	10m	
15:00 → 15:10	**Topical invited talk: Using COTS processing technologies effectively** **Speaker**: Conor Fitzpatrick (University of Manchester (GB))	10m	
15:10 → 15:20	**Topical invited talk: Moving intelligence onto the detector** **Speaker**: Farah Fahim (Fermilab)	10m	
15:20 → 15:50	**Comments and brief discussion** Identifying points to take to afternoon discussion **Speaker**: Dave Newbold (STFC Rutherford Appleton Laboratory (GB))	30m	