Angelo Rivetti

Future trends, challenges and opportunities in ASICs for HEP

a birds-eye view

INFN
Istituto Nazionale di Fisica Nucleare

Overview

- Relevant non-HEP related trends
- Relevant HEP ASICs trends and perspectives
- Some “experienced-based” remarks

Common features of ASICs for HEP

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- We need ASICs mostly for front-end, power management, data transmission;
- High resolution timing is becoming a must for many detectors;
- Finer granularity (but not so extreme), less power
- In (inner) layers of hadron colliders, life is complicated by radiation damage, which imposes lengthy technology testing procedure;
- We are adding cold ASICs to the menu;
- Production volumes are, at best, very modest compared to industry standard;
- HEP ASICs are very specific systems fabricated in mainstream technologies built out of very common critical blocks (ADCs, TDCs, PLLs, DLLs, Power converters, ser-des, etc..)

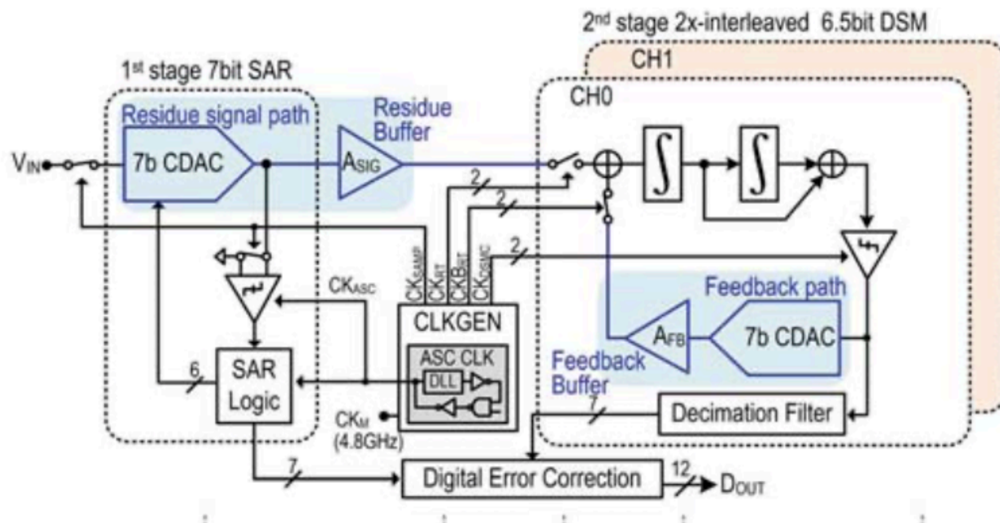
Key IPs: ADCs

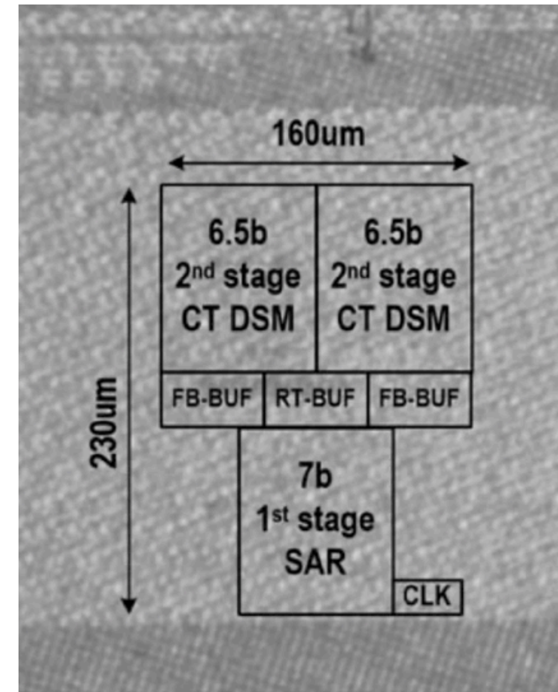
ISSCC 2021

10.5 A 12b 600MS/s Pipelined SAR and 2×-Interleaved Incremental Delta-Sigma ADC with Source-Follower-Based Residue-Transfer Scheme in 7nm FinFET

Seungyeob Baek, Ilhoon Jang, Michael Choi, Hyungdong Roh, Woongtaek Lim, Youngjae Cho, Jongshin Shin

Samsung Electronics, Hwasung, Korea





Power: 13 mW

Very good performance ADC in many different technology nodes
Extremely scaled nodes may bring density more than low power

Key IPs: ADCs

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322 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 55, NO. 2, FEBRUARY 2020

A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier

Wenning Jiang, *Student Member, IEEE*, Yan Zhu, *Member, IEEE*, Minglei Zhang, *Member, IEEE*, Chi-Hang Chan, *Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

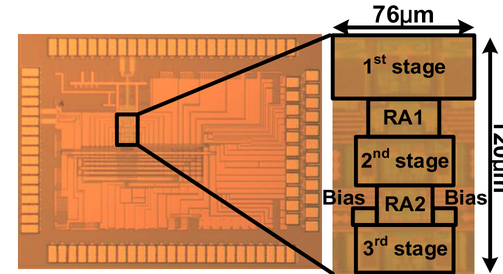


TABLE II
ADC PERFORMANCE SUMMARY AND COMPARISON

	This work	VLSI 2017[16] K.-J. Moon	JSSC 2018[3] R. Sehgal	ISSCC 2017[9] L. Kull	ISSCC 2017[17] H. Huang	ISSCC 2019[25] B. Hershberg	JSSC 2019[4] J. Lagos
Architecture	Pipelined SAR	Pipelined SAR	Pipeline	Pipelined SAR	Pipelined SAR	Pipeline	Pipeline
Residue Amplifier	Open-loop Gm-R	gm-cell	Open-loop Integrator	CML Amplifier	Dynamic Amplifier	Ring Amplifier	Ring Amplifier
Technology	28nm	28nm	28nm	14nm	65nm	16nm	28nm
Resolution [bits]	12	10	12	10	12	11	12
Sample Rate [MS/s]	1000	500	280	1500	330	600	1000
Supply Voltage [V]	1	1	1	0.95	1.3	0.85	0.9
SFDR @Nyq. [dB]	74.56	69.2	77	58.39	75.8	78.3	73.1
SNDR @Nyq. [dB]	60.02	56.6	64	50.1	63.5	60.2	56.6
Power [mW]	7.6	6	13	6.92*	6.2	6.0	24.8
FoM_{Walden} @Nyq. [fJ/conv-step]	9.28	21.7	35.8	17.7*	15.4	12	45
$FoM_{Schreier}$ @Nyq. [dB]	168.2	162.8	164.3	160.5*	167.8	167.2	159.6
Area [mm^2]	0.0091	0.015	0.22	0.0016	0.08	0.037	0.54

* including the reference buffer

Key IPs: ADCs

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 68, NO. 2, FEBRUARY 2021

A 91.0-dB SFDR Single-Coarse Dual-Fine Pipelined-SAR ADC With Split-Based Background Calibration in 28-nm CMOS

Yuefeng Cao, *Member, IEEE*, Shumin Zhang, Tianli Zhang, *Member, IEEE*, Yongzhen Chen, *Member, IEEE*, Yutong Zhao, Chixiao Chen, *Member, IEEE*, Fan Ye, *Member, IEEE*, and Junyan Ren, *Member, IEEE*

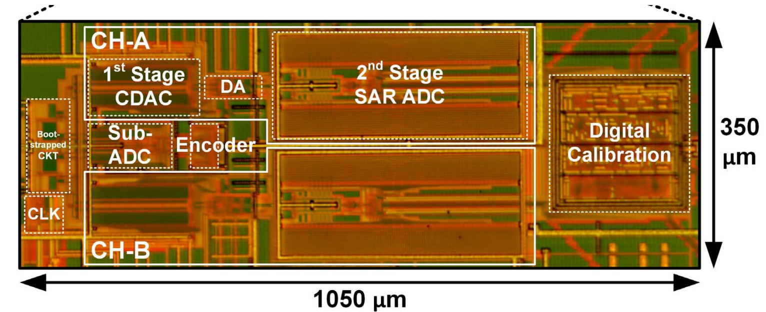


TABLE II

COMPARISONS TO OTHER DESIGNS WITH COMPARABLE SAMPLING RATE AND RESOLUTION

		Kapusta JSSC'13 [41]	van der Goes JSSC'14 [7]	Akter JSSC'18 [42]	Xu JSSC'19 [22]	Hung CICC'19 [43]	Seo VLSI'19 [44]	Liu ISSCC'20 [45]	Zhang ESSCIRC'19 [24]	This work
Process (nm)		65	28	40	65	90	40	40	28	28
Resolution (bits)		14	14	12	14	16	12	13	14	14
f_s (MS/s)		80	80	53	75	40	200	40	60	60
Supply voltage (V)		1.2	1.0	1.0	1.2	1.1	0.9	-	1.05	1.05
Core area (mm^2)		0.55	0.131	0.76	0.342	0.506	0.026	0.005	0.28	0.368
Calibration		analog	analog + statistical	analog + split-ADC	split-ADC+ LMS	no calib.	no calib.	-	split-ADC+ ML	split-ADC+ LMS
SNDR (dB)	@ low fin	73.6	68	-	77.8	72.6	61.1	70.8	66.2	66.9
	@ Nyq.	71.3	66	66	70.8	71.2	62.1	69	63.9	64.1
SFDR (dB)	@ low fin	-	80.7	-	92.1	-	65.2	86.5	93.7	91.0
	@ Nyq.	88.6	74.0	77.3	89.6	86.8	67.1	79.2	83.3	84.1
Power (mW)		31.1 *	1.5	9 *	24.9 *&	5.5 *	3.9	0.591	2.79	4.26 *#
FoM_S (dB)	@ low fin	164.7	172.3	-	169.6	168.2	165.2	176.1	166.5	165.4
	@ Nyq.	162.4	170.3	160.7	162.6	166.8	166.2	174.3	164.2	162.6
FoM_W (fJ/conv.-step)	@ low fin	99.4	9.1	-	52.3	39.4	21.0	5.2	27.9	39.3
	@ Nyq.	129.5	11.5	104.1	117.2	46.3	19.0	6.4	36.3	54.2

$FoM_S = SNDR + 10*\log_{10}(f_s/2/Power)$; $FoM_W = Power/(f_s*2^{ENOB})$.

* including clock buffer   & including reference buffer   # including digital calibration

- **Very good performance ADC in many different technology nodes**
- **External nodes may bring density more than low power**

A word on ADC architectures

- While technology has clearly a role, architectures have their share, too
- Many architectures employ SAR as main ADC or as a sub-unit
- Key changes in SAR topologies occurred 10-12 years ago the allowed much higher speed and low power (50 MS/s, 1 mW, 10 bit in 130 nm)
- If such architecture were there 10 years before, chip designed for LHC in 250 nm might have looked significantly different…

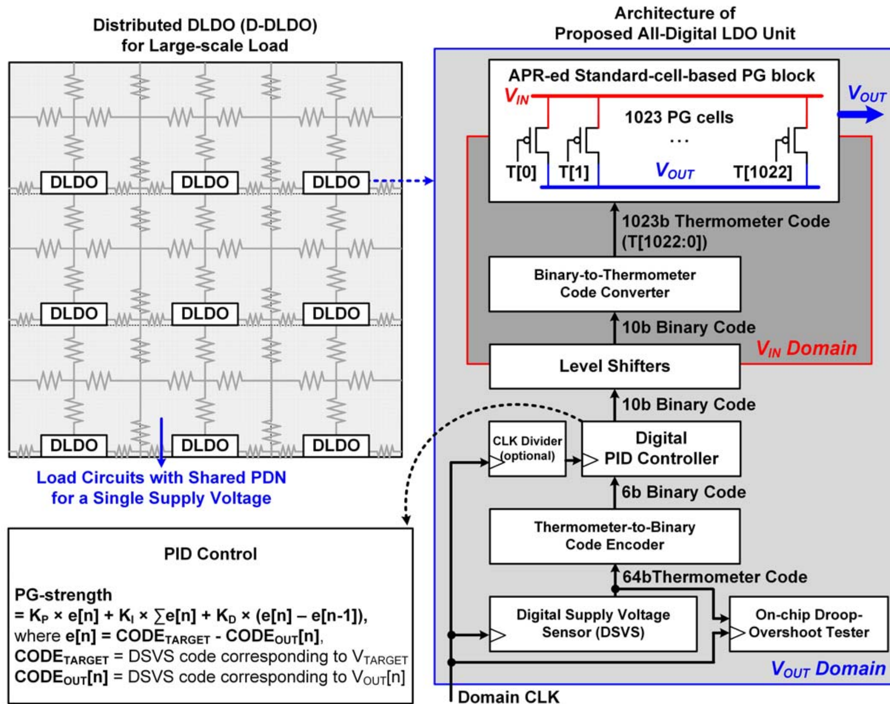
Key IPs: LDO

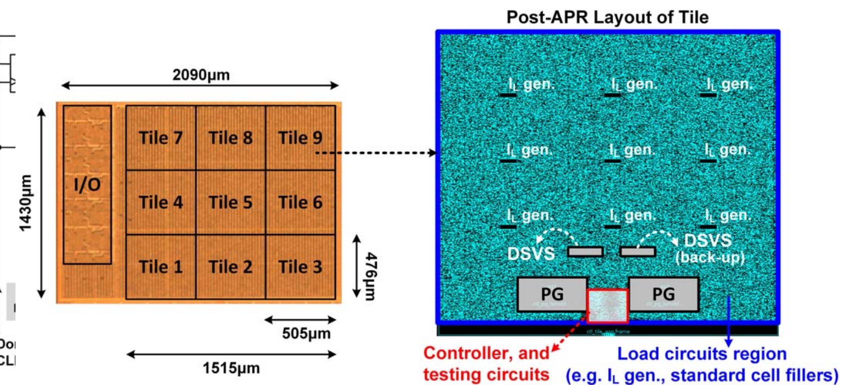
25.1 A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS

ISSCC 2020

Suyoung Bang, Wootaek Lim, Charles Augustine, Andres Malavasi, Muhammad Khellah, James Tschanz, Vivek De

Intel, Hillsboro, OR





- **Careful and distributed power management key for good performance**
- **Analog function designed with digital approach**
- **On chip DC-DC converters**

Mean & Variation of Measured DSVS Code of 9 Tiles at 1.5GHz

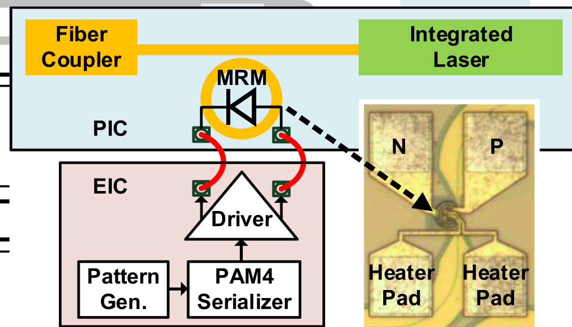
VOUT (0.840V) 100mV/div

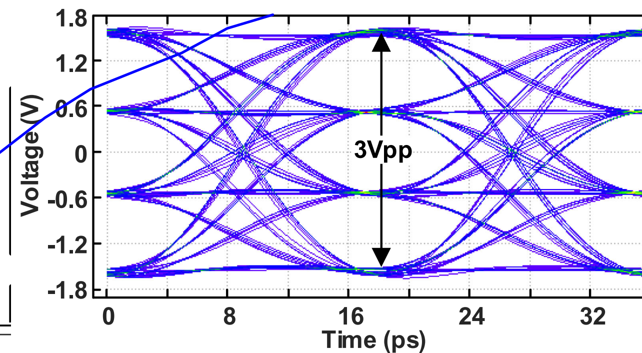
VOUT (0.840V) 100mV/div

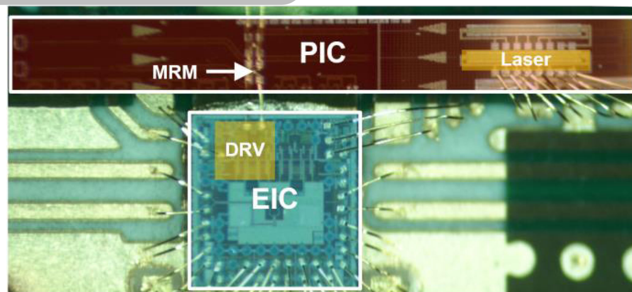
ke ... ran

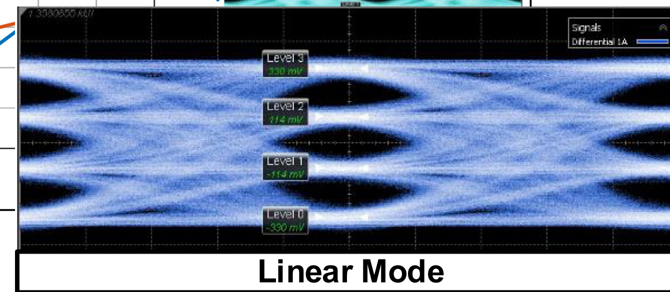
Silicon Photonics Transmitter
lodulator and CMOS Driver

, Jie Sun, Jeffery Driscoll, Ranjeet Kumar, Hasitha Jayatilleka,
Member, IEEE, James Jaussi, and Bryan Casper









(a)

28 nm + Silicon Photonics

Key IPs: TDC

Output code

Fig. 8. INL of proposed CB-VDL TDC.

A 0.6 V, 1.74 ps Resolution Capacitively Boosted Time-to-Digital Converter in 180 nm CMOS

ISCAS 2019

Arjun Ramaswami Palaniappan[1,2] and Liter Siek[1]
[1]School of Electrical and Electronic Engineering, VIRTUS, Nanyang Technological University, Singapore 639798, Singapore
[2]NXP Semiconductors, Singapore 138628, Singapore
Email: arjun011@e.ntu.edu.sg

TABLE I. PERFORMANCE COMPARISON OF TDC DESIGNS

TDC	**Proposed**[a]	[16]	[17]	[18]	[15]
Architecture	Cap Boost VDL	Stoch	Time Amp	Cyclic	Pipeline
Process	180 nm	14 nm	65 nm	0.35 µm	65 nm
Supply (V)	0.6	0.6	1.2	3.3	1.2
Power (mW)	0.217	0.78	2	80	15.4
Range (bits)	6	10	8	13	9
Resolution (ps)	1.74	1.17	2.6	0.61	1.12
INL (LSB)	1.45	2.3	2.36	7.38	1.7
F_s (MHz)	50	100	80	0.8	250
FOM (pJ/con.step)	0.166	0.025	0.328	102.3	0.325
Area (mm^2)	1.225[b]	0.036	0.07	0.61[c]	0.14

a. Simulated results
b. On-chip calibration
c. Off-chip calibration

Timing resolution defined at the interplay between the sensor and the very front-end

How small can be a

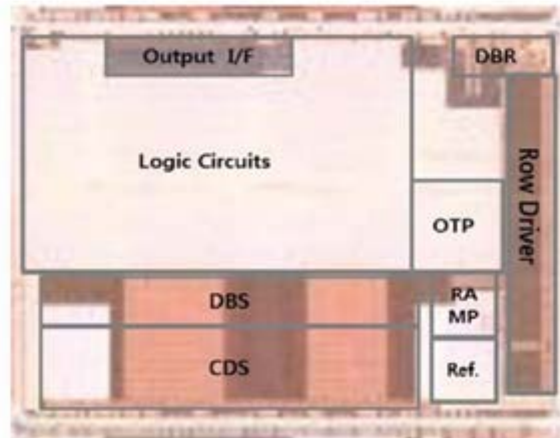
0.1
0 200 400 600 800
Output [DN]

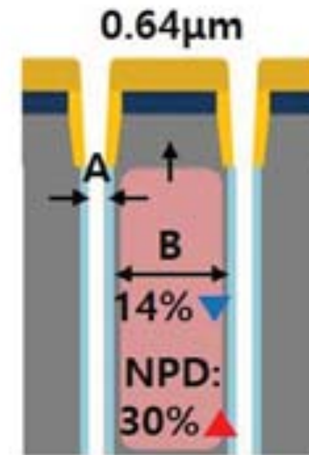
7.9 1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64μm Unit Pixels Separated by Full-Depth Deep-Trench Isolation

JongEun Park, Sungbong Park, Kwansik Cho, Taehun Lee, Changkyu Lee, DongHyun Kim, Beomsuk Lee, SungIn Kim, Ho-Chul Ji, DongMo Im, Haeyong Park, Jinyoung Kim, JungHo Cha, Taehoon Kim, In-Sung Joe, Soojin Hong, Chongkwang Chang, Jingyun Kim, WooGwan Shim, Taehee Kim, Jamie Lee, Donghyuk Park, EuiYeol Kim, Howoo Park, Jaekyu Lee, Yitae Kim, JungChak Ahn, YoungKi Hong, ChungSam Jun, HyunChul Kim, Chang-Rok Moon, Ho-Kyu Kang

9365751

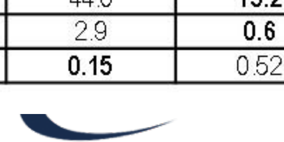
Items	unit	0.7um	0.64um
Linear FWC	e-	6,000	6,000
Dark current	e-/s	1.3	1.1
White spot[1)]	ppm	10	15
Random noise	e-	1.4	1.4





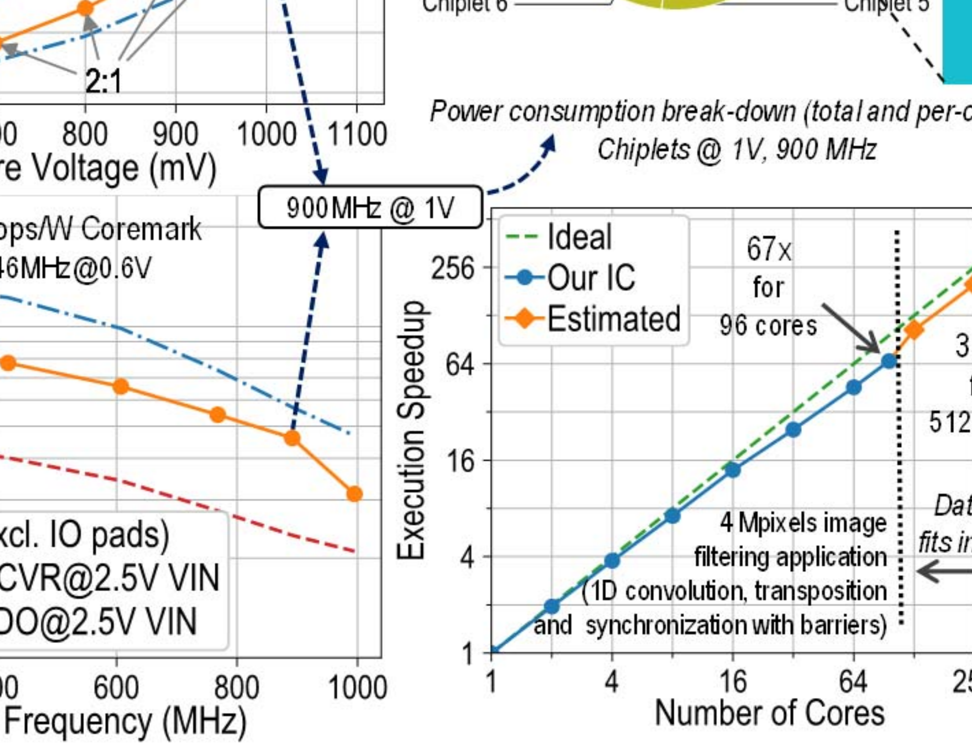
...idth Density	0.5	**3.0**	1.6	Tb/s/mm²
...h Cross Section	**0.9**	N/A	0.8	Tb/s/mm
...e inter-Chiplets	394	133	640	GB/s
...andwidth	527			

End to end latency	**7.2**	44.0	**15.2**
Propagation speed	4.8	2.9	**0.6**
Energy / bit / mm	0.29	**0.15**	0.52



2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm

ISSCC 2020@IEEE

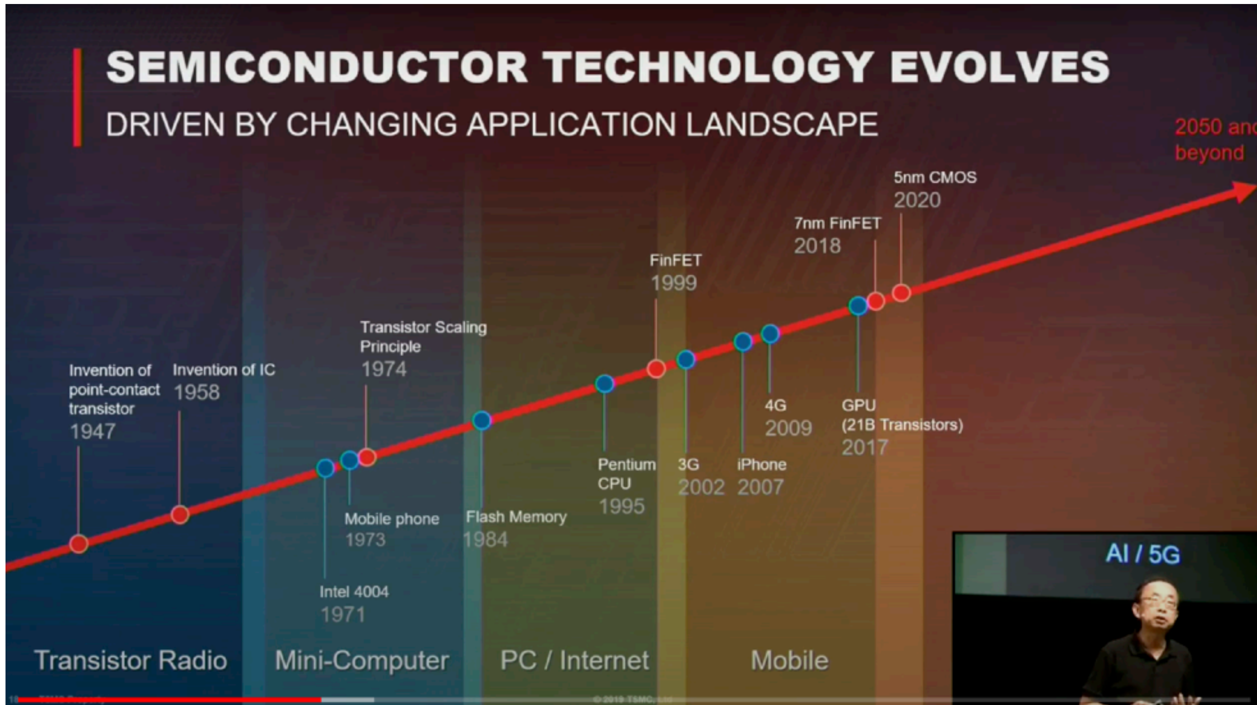


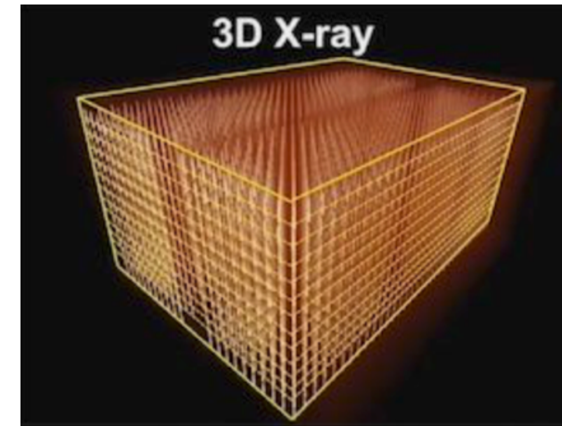
Power consumption break-down (total and per-chiplet)
Chiplets @ 1V, 900 MHz

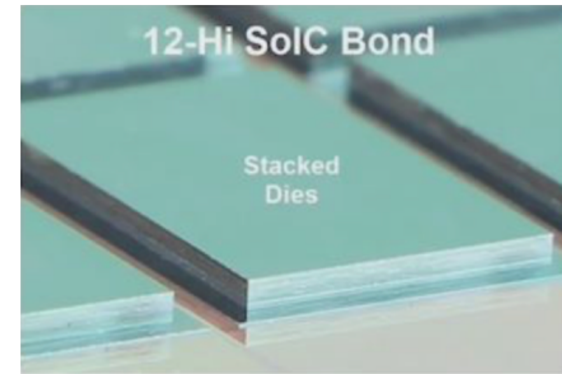
		This work
Technology	Chiplet Technology	FDSOI 28nm
	Interposer Technology	**Active** CMOS 65nm
	Interposer extra features	**yes**
	Total system yield	High, using active interposer mature technology and low transistor count
	Die-to-Die µbump pitch	**20**
Power Mgt	Voltage Regulator (VR) type	**Integrated in interposer,** 1 SCVR per chiplet with **MOS+MOM+MIM**
	VR area	34% of active interposer
	VR peak efficiency	**82%**
Interconnect	Interconnect types	**Distributed NoC meshes** for scalable chip-to-chip cache-coherency traffic
	3D Plug power efficiency	0.59
	BW density	**3.0**
	Aggregate 3D bandwidth	527
CPU	Number of chiplets	**6**
	Number of cores	**96**
	Max Frequency	1.15
	Gops (32b-Integer)	**220 (peak mult./acc.)**

Moore after Moore

https://www.youtube.com/watch?v=O5UQ5OGOsnM





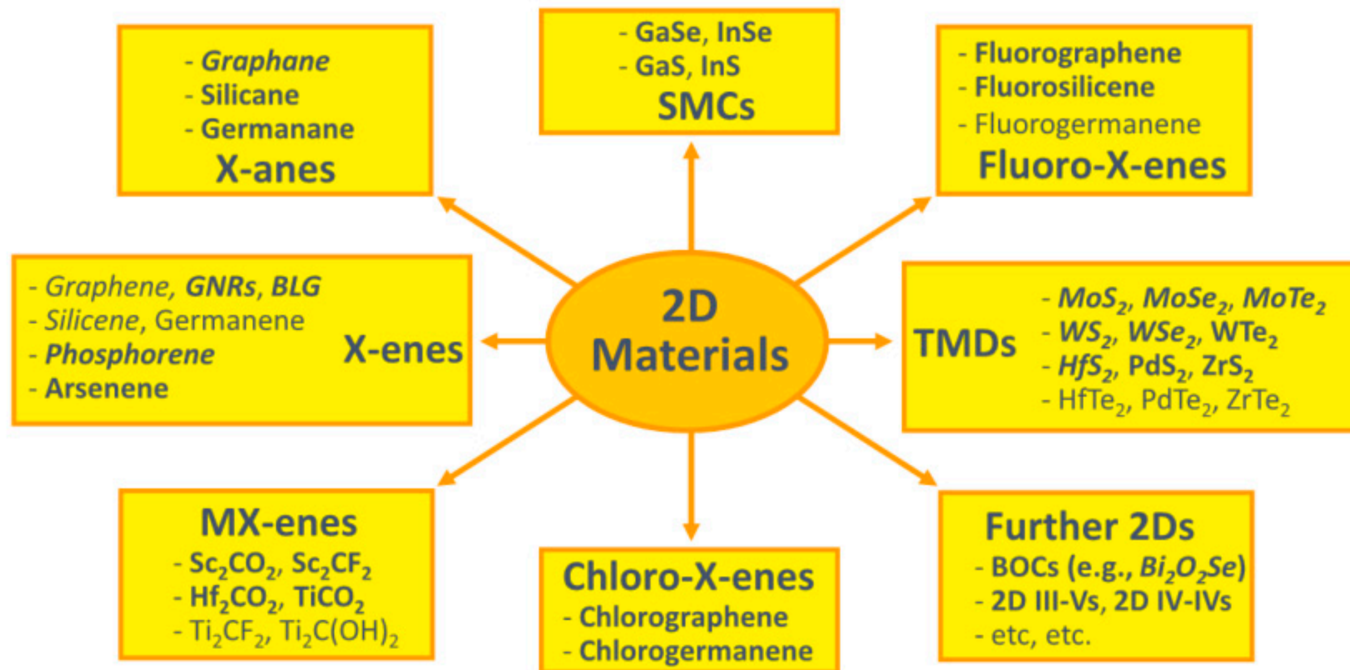


P. Wong, TSMC Vice President for R&D: "Moore law is not dead, it is not even sick!"

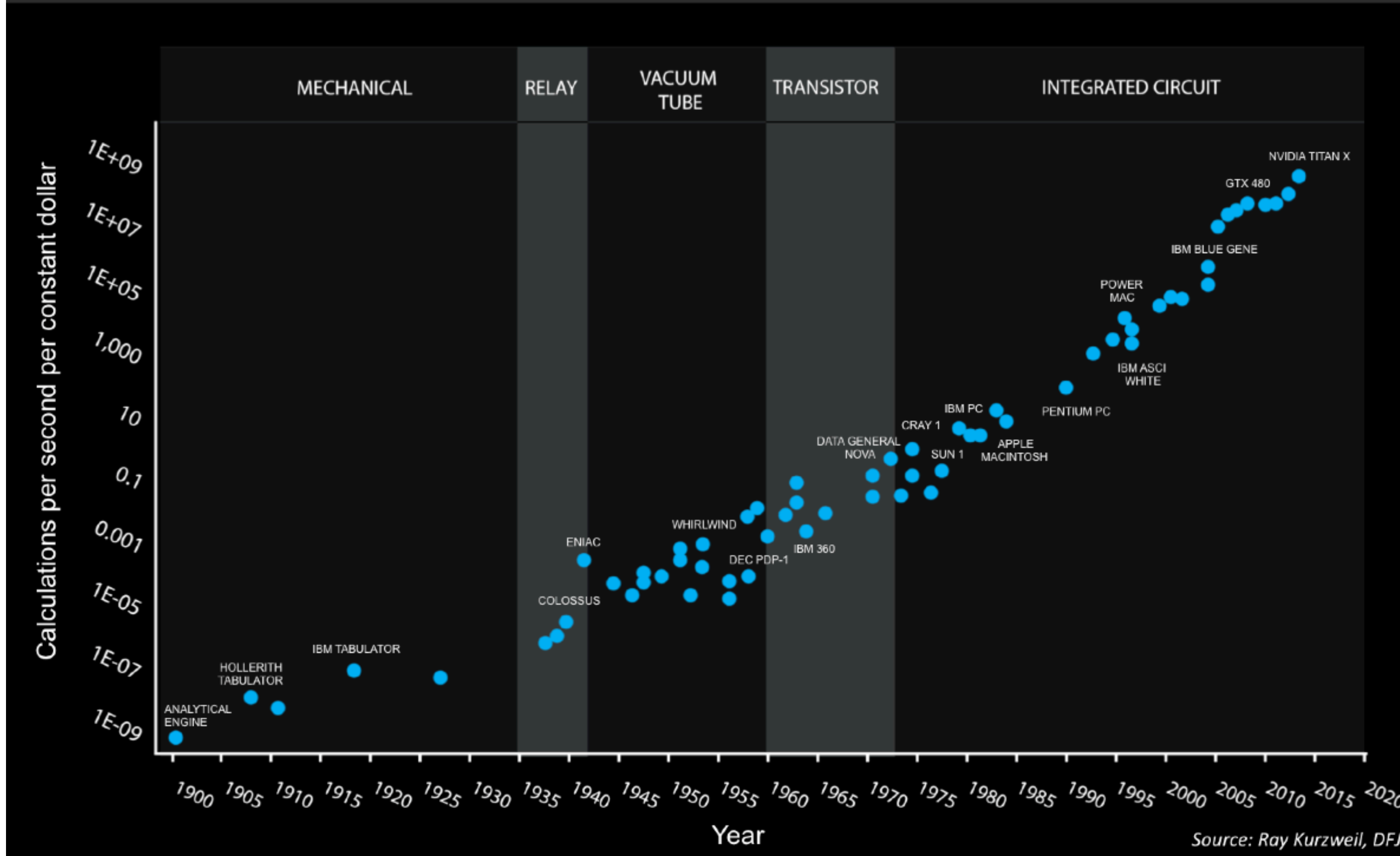
- **Moore laws may continue due to 3D integration and new devices**
- **New technologies may surprise us and open unexpected possibilities**

New materials being investigated

Nanomaterials **2020**, *10*, 1555



Moore before Moore



https://upload.wikimedia.org/wikipedia/commons/6/62/Moore%27s_Law_over_120_Years.png

IC economics

Hardware Design Cost

>10 M$

Verification!

1.5 M$

0.4-0.8 M$

Hardware Design Cost ($M)

210.000
180.000
150.000
120.000
90.000
60.000
30.000
0.000

23.185
32.313
51.843
94.976
192.950

IP Qualification
Architecture
Verification
Physical Design

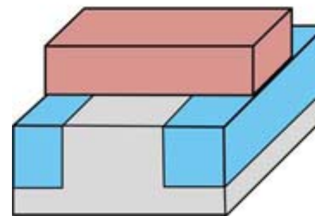
65nm
40nm
28nm
20nm
16/14nm

Technology may also saturate (at least for a long while…)

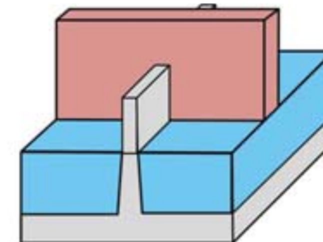
- because of physics…

- Expected at least 90 years in service

- … cost

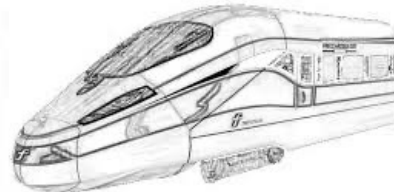


Planar FET

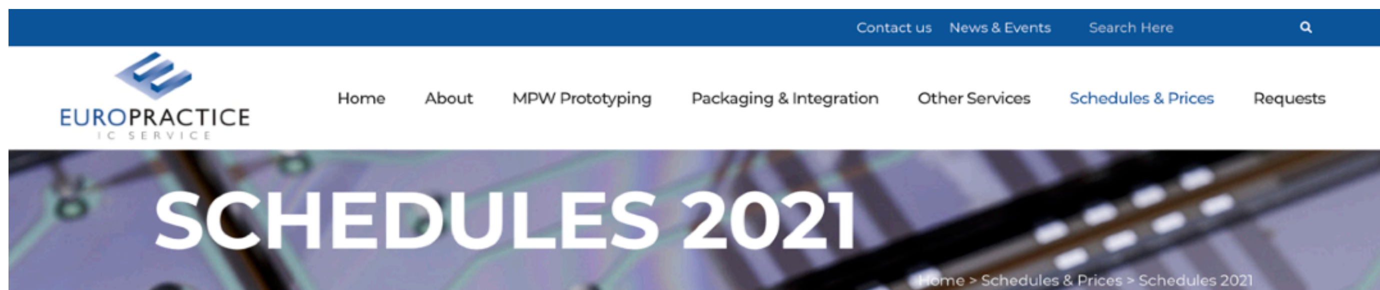


Fin FET

Technologies can coexist for an indefinite time

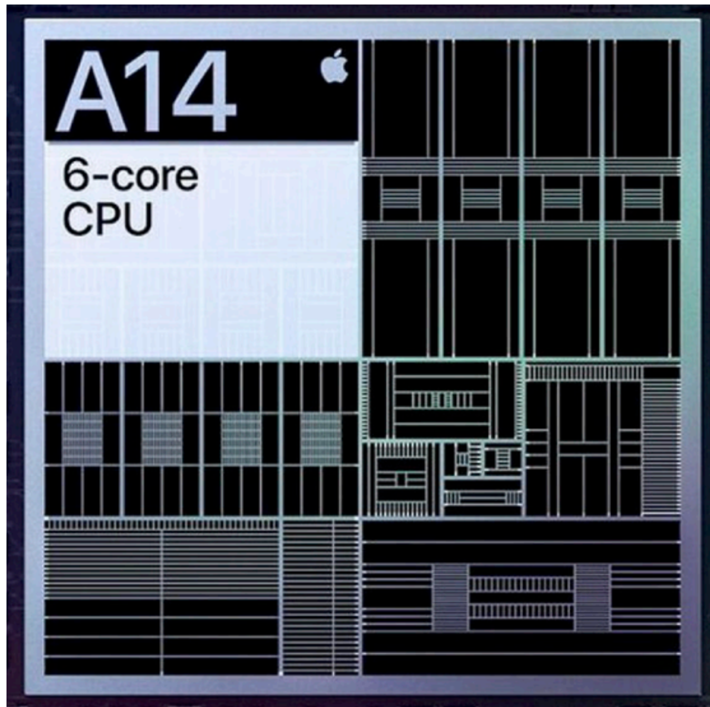


https://europractice-ic.com/schedules-prices/schedules-2021-2/



- **Two order of magnitudes in transistore gate length (and in price): from 0.7 um (at 300 eur/mm^2) to 12 nm (26.000 eur/mm^2)**

One extreme…



- 5 nm technology
- Exa-core
- 64 bits
- Neural engine
- 11.8 billions transistors
- 88 mm^2
- 130 millions transistors/mm^2

- In a typical mobile SoC: 60% logic, 30% RAM, 10% analog
- In comparison, we have onboard our chips just a bit of logic…

…and the other

https://efabless.com

efabless.com

COMPANY CONTACT MARKETPLACE LOGIN REGISTRATION

efabless.com + arm®

Low cost custom ASIC for Edge IoT Products

$70K
20 WEEKS
100 SAMPLES

LEARN MORE

OPEN MPW SHUTTLE

The first Google sponsored open-source shuttle completes tapeout for open SKY130.

YEAR IN REVIEW

Check out these highlights for 2020.

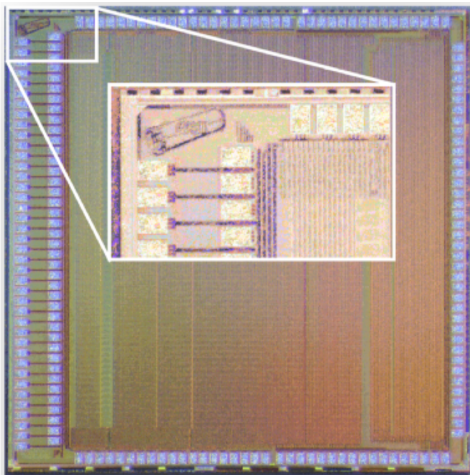
EFABLESS PRESENTS

See our latest presentation at the FOSSi Dialup.

https://www.skywatertechnology.com

Technology wrap-up

- There are much more opportunities than what we can possibly explore
- Average technology node life-time proved to be much longer than imagined in the past
- Choosing a technology, to some extent, is always a bet
- No particular concerns on performance achievable for key IP blocks in very advanced nodes
- What you really buy is density, speed and power for digital components and you should use it
- R&D on most advanced nodes should be definitely supported
- The key issue is to have enough engineers to work out the best of it to our needs
- E.g. 9 mm2 in 12 nm = 234 k euros= 20.000.0000 transistors. What do you do with that!?
-



- 110 nm technology
- 5 mm x 5 mm
- 64 channels
- 10 bits ADC, 50 ps TDC per channel
- 30 keuros for protoyping, 170 keuros for production

We need to move, but we should not be in a hurry
Take the time to think…

Trends in ASICs for HEP

Present/near term

SALT: 128 ch. ASIC for strip readout in LHCb - M. Idzik, TWEPP 2019

128 channels
IN[127:0]
inputs x128
Preamplifier
Shaper
Single to Diff
ADC
6-bit SAR
DSP
Memory buffer
Serialiser
Deserialiser
6 e-links
SLVS
6x data output
TFC input
TFCcmd
adc_clk
DLL
64 CLK Phases
calib_clk
data_clk
Test pulse generator
TFC counters
Configuration Registers
PLL
x4
Calib
Biasing DACs
I2C
control signals
MAIN_CLK

FLAME for LumiCal

FLAME
FcaL Asic for Multiplane rEadout
FLAME channel x16
FE
10-bit ADC
TEST MODE 1
TEST MODE 2
TEST MODE 3
Data header
8b / 10b coding
x26*
Initial serializer
Final serializer
SST
Multi-phase PLL
Channel biasing
Slow control
x16

FLAME layout: the size is 3.7mm x 4.3mm

Cable Type I
Service module
Cable Type II
New
Cable Type III
New
Cable Type IV
Reused
Power Supply
~1.5m
PP1
~15m
PP2
~30m
PP3
~90m
PP4

Trends in ASICs for HEP

Likely evolution in multi-purpose ASICs

- Include also TDC for timing
- Higher resolution, flexible ADCs
- Fully fledged on board DSP
- High granularity on board power management
- Looks very promising for advanced nodes

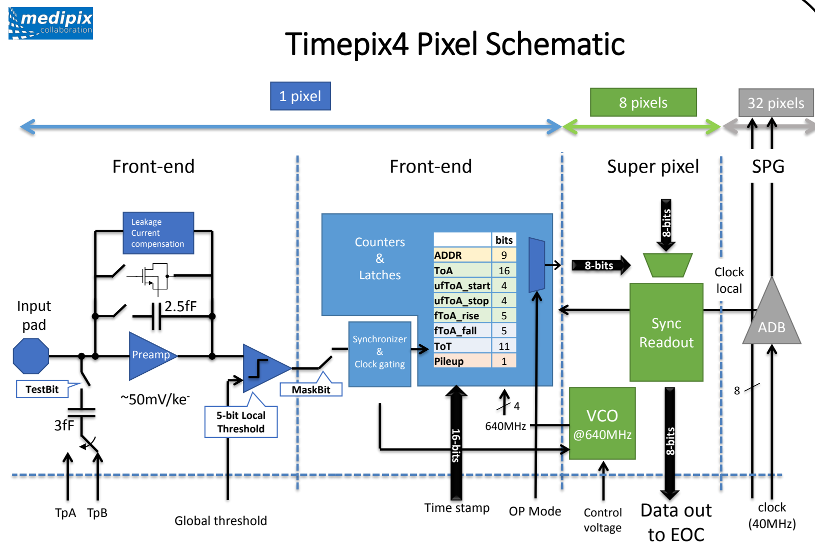
How much intelligence do we need on chip?

- In very advanced node it is natural to have more processing power
- Exact partitioning between on-board and off-detector signal processing to be determine with detailed detector studies
- Fully fledged on board DSP
- High granularity on board power management

Trends in ASICs for HEP: hybrid pixels

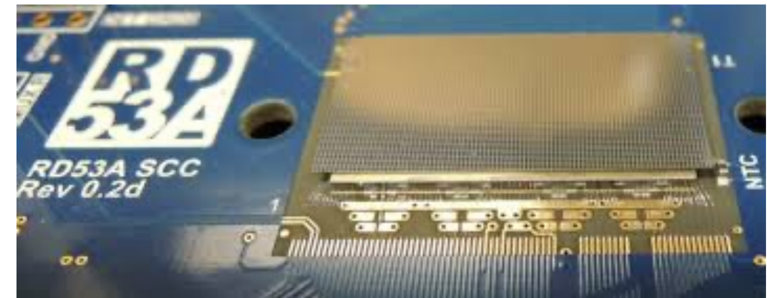
Present/near term

TimePix4



- Time resolution 200 ps
- 55 micron pixel pitch
- 4 sides buttable with TSV
- 3.5 MHit/mm²/s
- 65 nm CMOS

RD53 series



- Common baseline development
- Final chips customised in some details
- 50 x 50 um pixels
- > 1 GHz/cm2
- 65 nm CMOS

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Trends in ASICs for HEP: hybrid pixels

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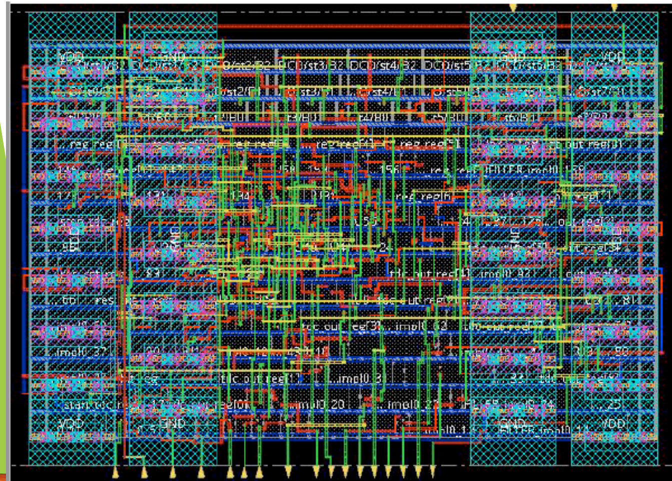
Likely future evolutions

- Reduced pixel cells (towards 25 um x 25 um @FCC-hh
- Move to more scaled technology nodes: 28 nm, ??
- High time resolution per pixel (< 100 ps)
- New interconnection technologies: high performance
- More processing on chip

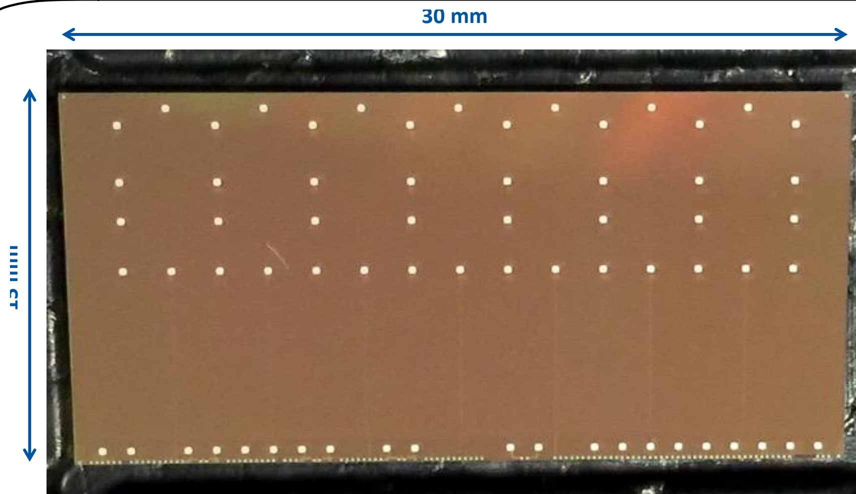
68.0 58.0 50.0 42.0 34.0 26.0 18.0
jitter [ps]
1.0 3.0 5.0 7.0 9.0
power [uW]



- TDC on the INFN Timespot ASIC
- 55 um x 55 um pixels
- TDC size 22 um x 15 um
- Real time time-walk correction
- 28 nm CMOS

Trends in ASICs for HEP: monolithic

State of the art



- 180 nm CMOS
- Sparsified readout
- 28 um x 28 um pixels
- 24000 sensors for 10 m2

Likely future evolutions

- Ultra-thin, wrap-around CMOS sensors
- Beyond reticle size with stitching
- Fully depleted CMOS
- CMOS sensors with timing capabilities
- Due to 3D integration, monolithic and hybrid may converge in high performance solutions
- In outer layers lots of 2D CMOS sensors

Final thoughts

- Accelerators are expected to follow an evolutionary approach: requirements in ASICs rather clear even for the very far future;
- In term of technology, only problematic case: FCC-hh at < 40 cm: but we have some time ahead
- For the rest, it is mostly a question of budgets
- Biggest issues will not be technology per se, but costs at large
- We need to profit more by the latest advances in CAD tools, which are tuned to chip extremely more complex that the ones we typically need to develop
- Promote collaboration more than competition (e.g. avoid “parallel options”)
- Incorporate early realistic ASICs description in detector simulations
- Open ecosystem of IPs
- For full size ASICs have teams of appropriate size (both too large and too small can be a problem) with roles and tasks
- Multilateral funding implies multilateral teams