Moving to leading-edge technology nodes (seriously?)

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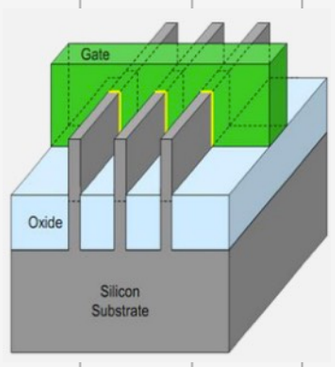
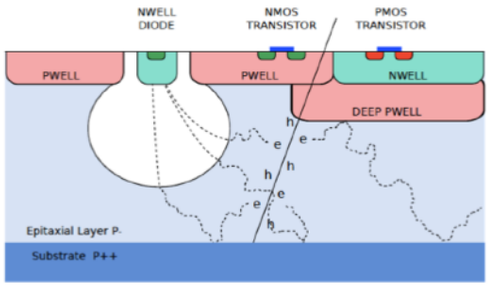
Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab

SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
STMicroelectronics	STM	STM	STM	STM	STM					
HLMC	HLMC		HLMC	HLMC	HLMC					
UMC	UMC	UMC	UMC	UMC	UMC		UMC			
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC		SMIC	SMIC		
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF			
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	
250 nm	180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

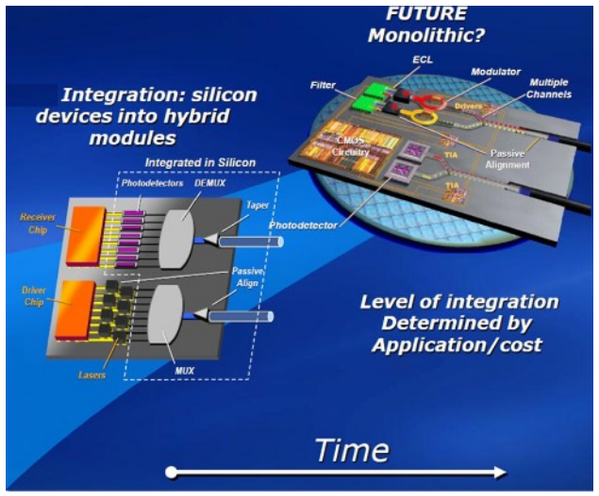


Monolithic Si detectors



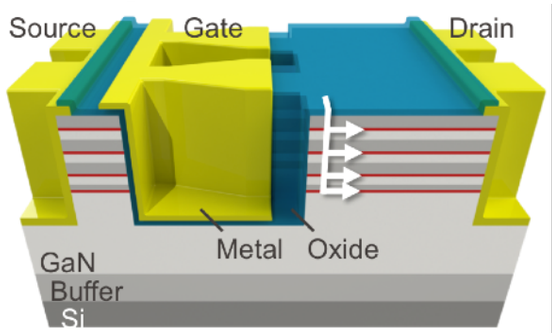
Schematic cross-section of CMOS pixel sensor
(ALICE ITS Upgrade TDR)

Silicon Photonics



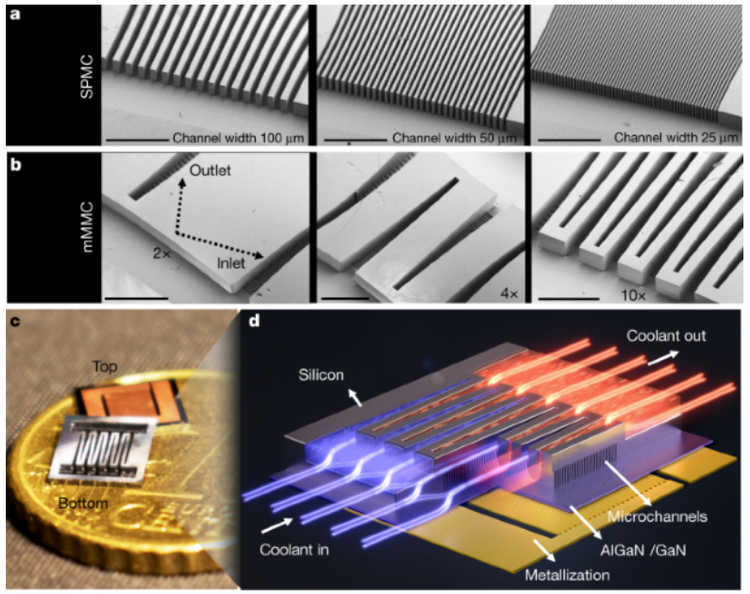
G.Tzintzarov et al., "Optical Single-Event Transients Induced in Integrated Silicon-Photonic Waveguides by Two-Photon Absorption", 2020 NSREC

GaN power devices on Silicon

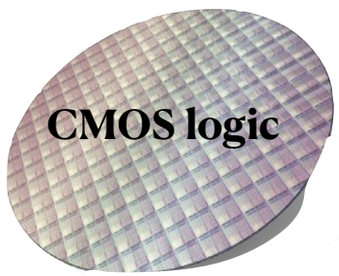


E.Matioli, "Nanoscale design for large-scale challenges: New technologies for efficient power devices, effective thermal management and faster electronics", ESE group seminar (CERN indico event 998073)

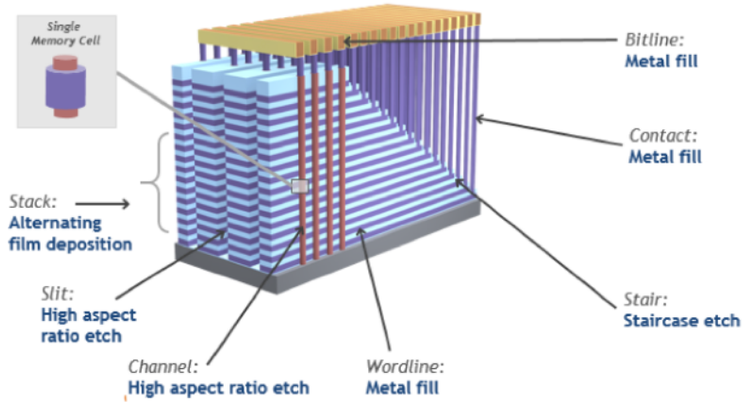
Cooling channels on silicon

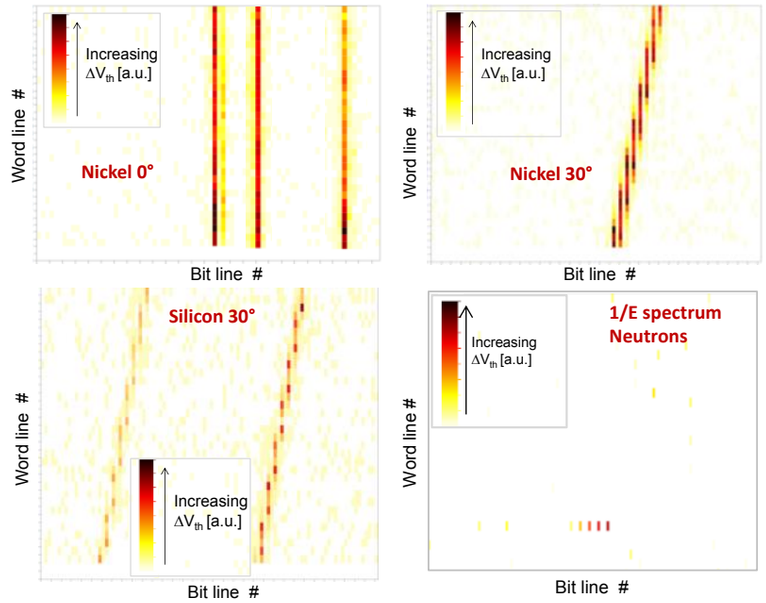


R. van Erp et al., "Co-designing electronics with microfluidics for more sustainable cooling", Nature, Sept.2020



Particle detection in 3D Flash NAND





from M.Bagatin et al., IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 67, NO. 1, JANUARY 2020

more advanced

Moving to ~~leading-edge~~ technology nodes

WHY?

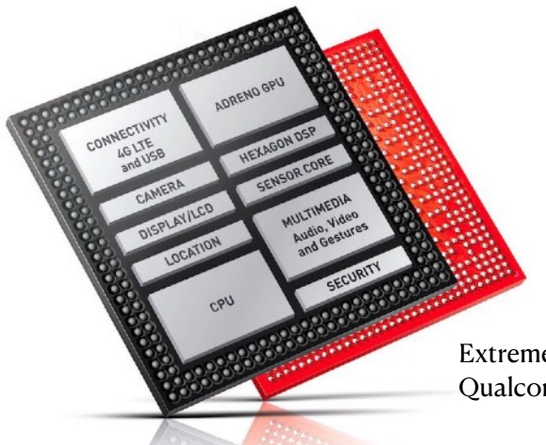
Performance

Speed

Fast timing detectors
High-speed communication

Integration

More functions on-chip



Extreme example:
Qualcomm Snapdragon

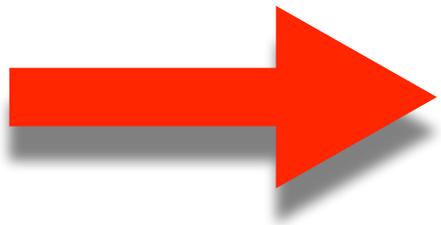
Low power per function

more advanced

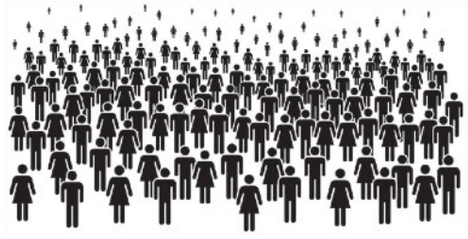
Moving to ~~leading-edge~~ technology nodes

WHY?

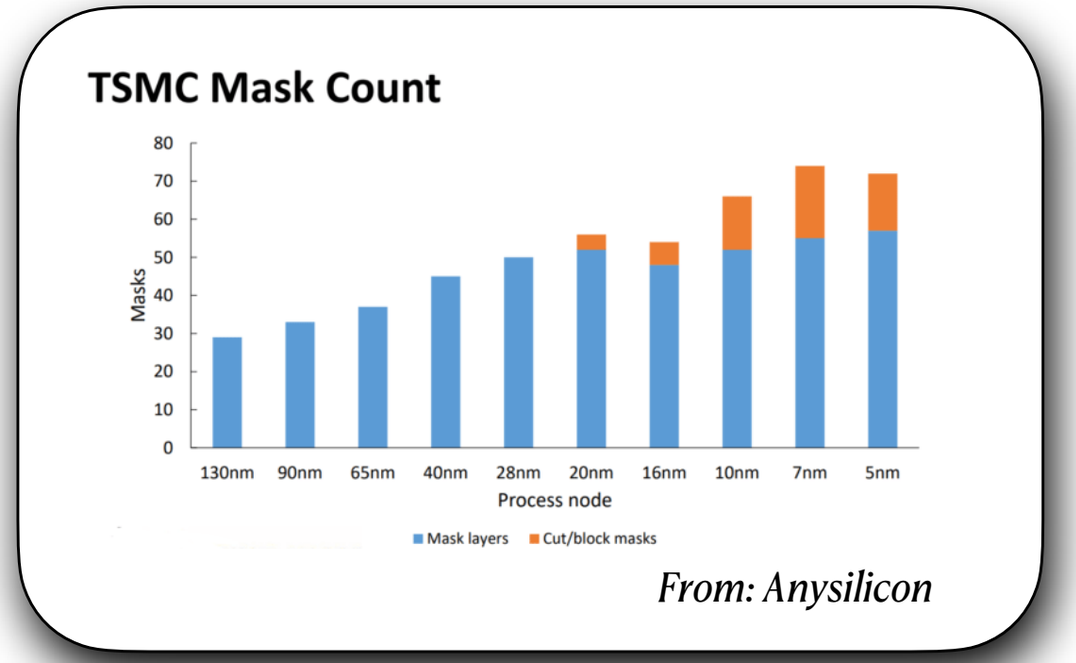
We can do so much more!



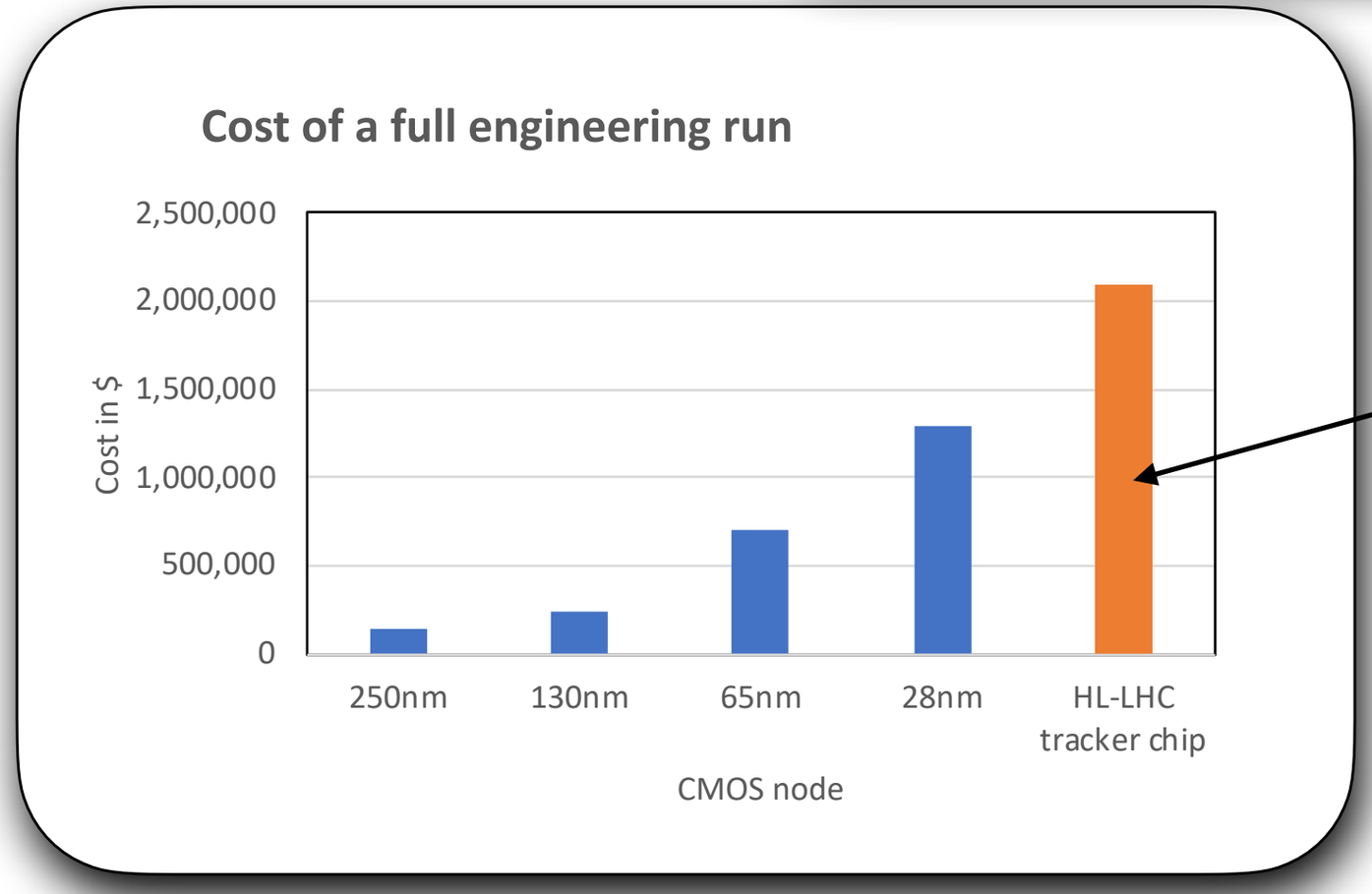
….. but it can not be done in the same way



The increasing complexity in silicon manufacturing is expensive for low-volume ASICs

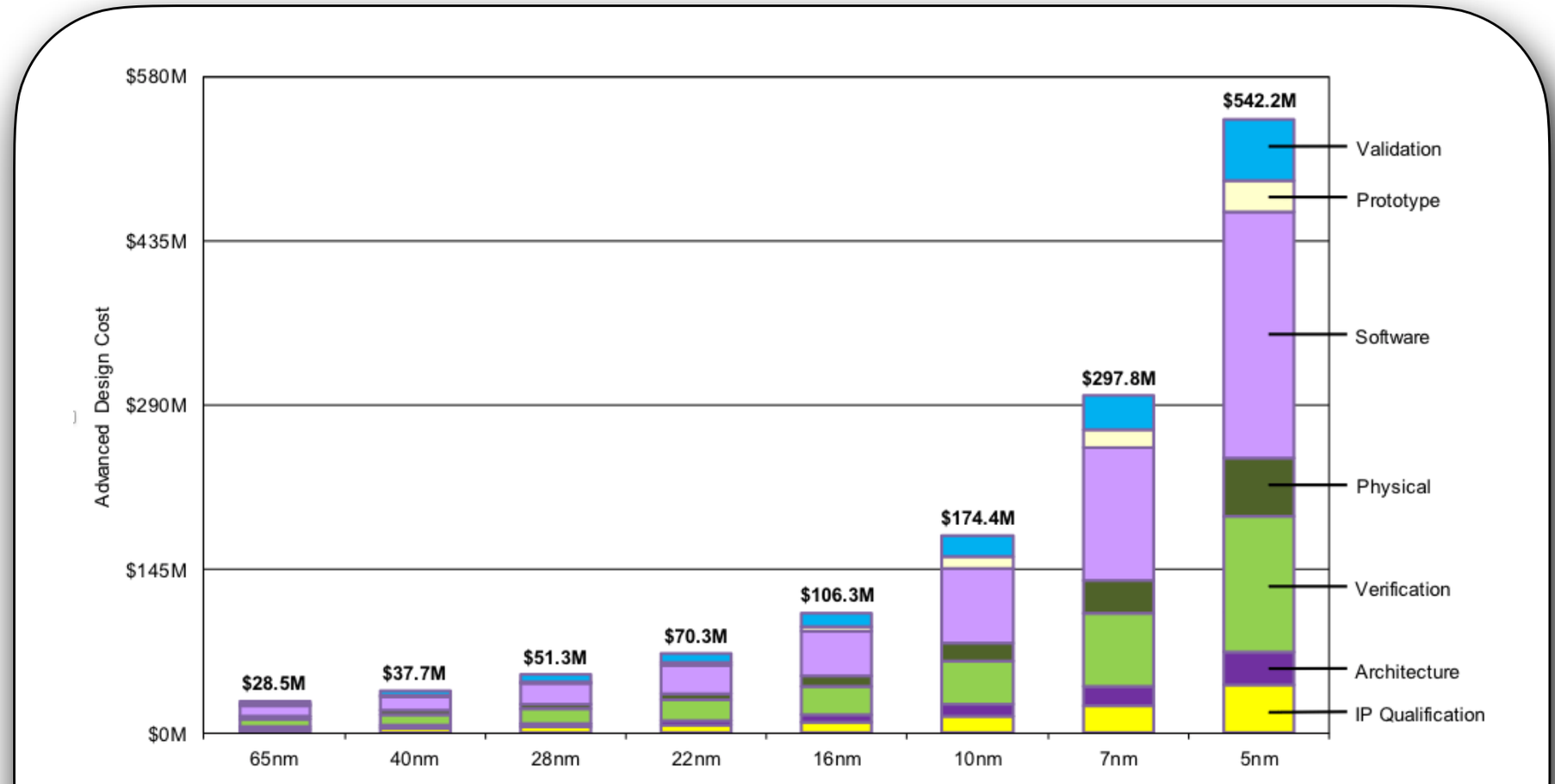


From: Anysilicon



Cost of masks + 600 production wafers (full volume, 130nm)

Silicon is not the only expensive item:
IC development requires trained people and advanced software



From: Semiconductor Engineering

The round of competences/toolsets needed to design a complex ASIC

Infrastructure

Technology infrastructure

Technology access (NDAs, ...)
PDK
Design flow
Choice of options:
- metal stack
- V_{th}
- library (28nm = 45 library sets)

IP infrastructure

Foundry, 3rd party, collaboration
Blocks qualified on Si:
ESD protection
Memory generators
CMOS/SLVS pads
Bandgap, DACs, ...

IT infrastructure

Hardware
EDA tools
Versioning tools

+ Radiation Effects (TMRG, SET verification, ...)

Project-Specific

Project-specific analog blocks

Spectre
Virtuoso schematic/layout
Liberate AMS
Quantus QRC

Custom (low-noise, high-speed, power management...)
Behavioural model/Abstract generation
Analog design, verification

Digital code

TMRG

High-level description
of all functions
Triplication
Addition of testability

Design verification

Conformal LEC
Xcelium simulation
Manager
Jasper Gold

UVM/System Verilog Test Bench
Formal verification
Fault tolerance
Mixed-signal simulation (AMS)
Logic-equivalent check (LEC)
Post-layout simulation

Physical implementation

Quantus QRC
Modus
Genus
Innovus

Floorplan
Synthesis
Design For Testability (DFT)
Place & Route

CHIP sign-off

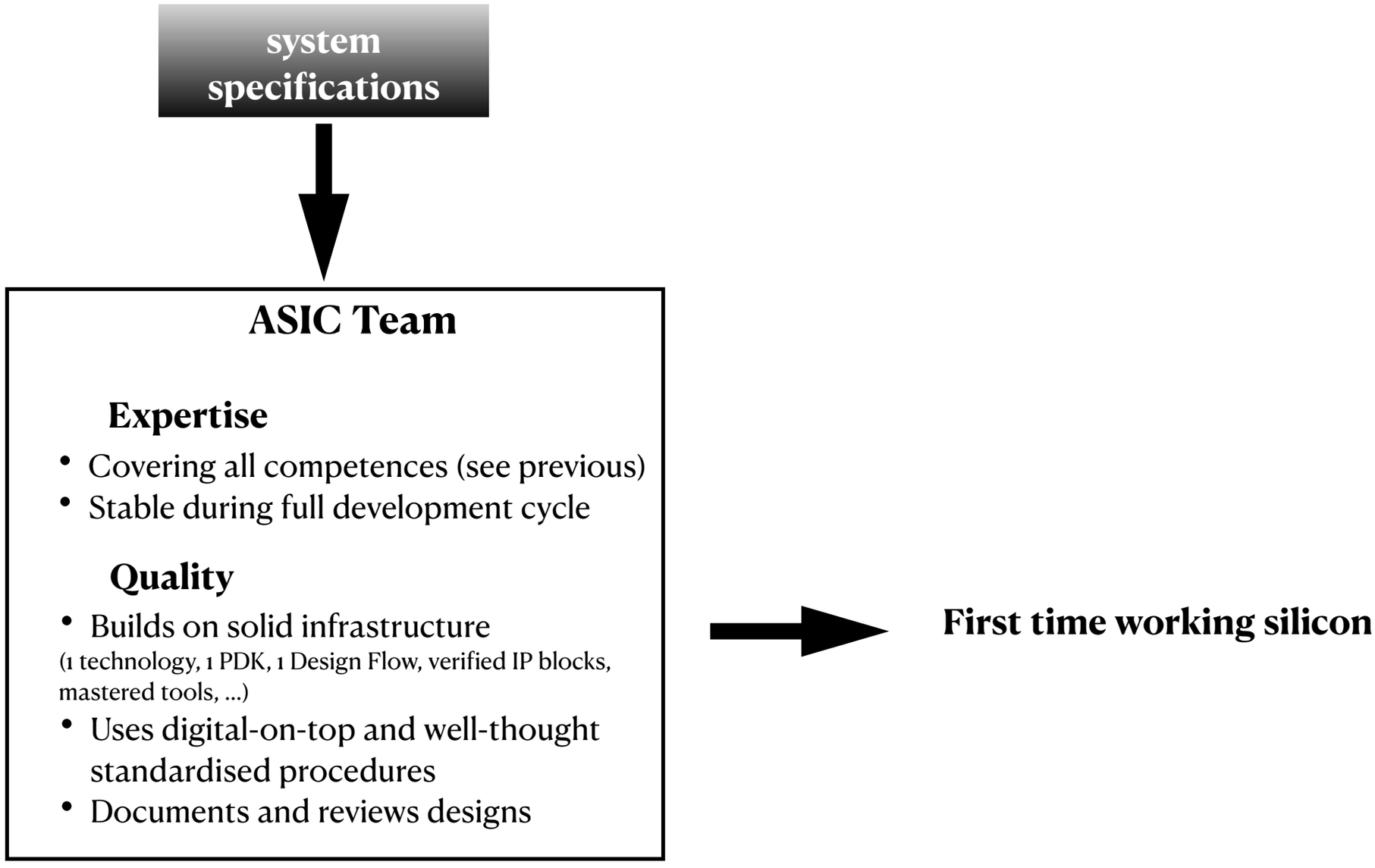
Calibre
Tempus
Voltus

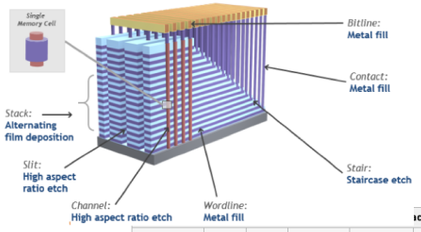
Static timing analysis
Physical verification
Power integrity

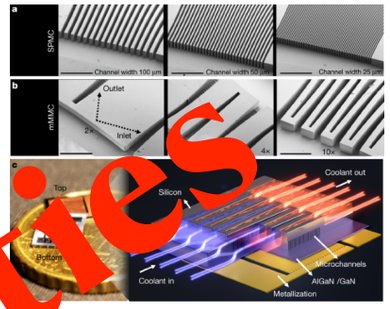
Example: lpGBT

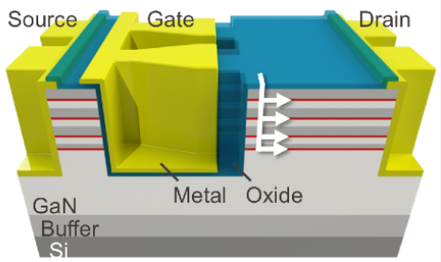
# of transistors	9×10^6
Lines of code in the design:	
RTL (design)	7.5×10^4
Verification	9×10^4

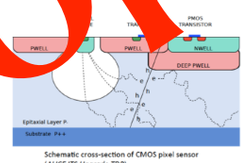
Complex ASICs: some necessary ingredients to a successful development











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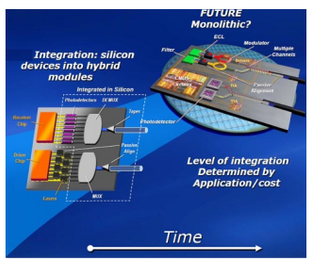

Opportunities

Expertise

Quality

= more resources in microelectronics