Electronics and On-Detector Processing

Part I: ASICs and front-end electronics Q&A (sorted by popularity)

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- Gianni Mazza 09:42 AM “access to CAD design”
  - A possible issue is the increasingly difficult access to CAD for ASIC design, especially for research institutes.
- Stefan van Waasen 09:50 AM ”more system level input”
  - We need to improve in general the development flow with much more system (high level) design as input for chip solutions for best partitioning and optimized overall system solutions. This also need to include input also detector physics as input for design. In principal not always a e.g. better ADC is the best solution. This can be much easier seen on system level.

- Magnus Hansen 10:45 AM ”long term attractivity”
  - Todays speakers and myself will have retired when a new collider moves into the commissioning phase and chances are that so are their students. One key target must be to attract, continously through the coming 30 years young engineers AND physiscists, to HEP. It is difficult to imagine a fresh team to design, construct and commission a performant and performing detector system for e.g. an LHC experiment as a first construction project.
  - Definitly a very important step. Also smaller scale projects can help to explore several new approaches, before betting on a single horse.

- Stefan van Waasen 09:36 AM ”really getting 3D”
  - What is the best way to enable real 3D integration (incl. TSV) for us? Especially to bring together optimized designs of optical and electronic solutions. We definitively need to bundle it to get enough power.

- Magnus Hansen 10:34 AM ”getting the specs early”
  - First time working silicon - provided that the requirements are well known, understood and accepted by the ASIC design team early enough. This probably means the infrastructure chips, essentially data transfer and controls, are defined and perhaps implemented first as the top level system design will take this (data transfer capacity and means of controls) as input.

- Xavi Llopart Cudie 10:38 AM
  - We need to have well defined specifications when starting a project. Moving to advanced technology nodes forces a top down design approach where full systems are modeled even before start designing any ASIC. The bottom - up approach that has been followed is not cost and time effective anymore. System level verification is a must!

- Stefan van Waasen 09:32 AM ”availability of IPs”
  - Not only faster and better ADCs/TDCs is cruical. Best would be availibility of IP which is scalable in performance (bit width, sampling rate) and power consumption!
  - Gianni Mazza 09:53 AM As a key IP I would emphasize low jitter PLLs, which are needed by SAR ADCs, high speed data transmission and many TDC architectures
  - Stefan van Waasen 10:01 AM This is a very im portant IP but should also consider if it is possible/allowed to use LC-based structures. In high magnetic field or general distorted environments that could difficult. This means also LC-free structures can be very useful.

- Adriano Lai 09:51 AM : “open source and legal issues”
  - Increasing of costs and complexity in ASIC design and production require to concentrate efforts and resources. This makes the pair with knowledge exchange and expertise circulation. Such a process is strongly counteracted by NDA and licensing rules. For the future of the HEP community of ASIC designers is absolutely vital to build a different work scheme and somehow convince foundries and tool providers to treat us in a different way
  - Johannes Wüthrich 09:54 AM I already commented this above, but the push towards Open-Source in IC Design is already happening (see for example the Open-Source Skywater PDK: https://github.com/google/skywater-pdk).
  - I would be amazing, to also put the weight of our comminuty behind this effort, and potentially convince more foundries to also go into this direction.
  - Adriano Lai 10:01 AM Unfortunately I do not think that open-source is the solution. Th eproblem is much more complex at the legal level
  - Stefan van Waasen 10:02 AM This is a very im portant IP but should also consider if it is possible/allowed to use LC-based structures. In high magnetic field or general distorted environments that could difficult. This means also LC-free structures can be very useful.
  - Stefan van Waasen 10:25 AM "Army of Enginneers" sounds not very appreciting. These are absolut specialists in engineering science and can earn double or three time in industry. So we should be very welcoming to them with interesting tasks and responsibilities.
  - Federico Faccio 10:33 AM No depreciation of these engineers was meant, quite the opposite. “Army” refers to the number and organisation in the industry. Of course we should welcome them. In my section at CERN we have just hired 2 verification engineers from industry, and they are bringing so much with them!
  - Christian Grewing 10:38 AM This soldier agrees with Stefan, but I see what was meant..

- Wei Shen 10:12 AM ”low temperature design”
  - What about the trend at low temperature especially for Dark matter search and neutrino physics more relevant? This is definitely not an industrial requirement. However, certain synergy is probably necessary to push forward or benefit from using Standard CMOS technologies.
  - Andre Zambanini 10:18 AM Characterizing the technology for tempertures outside the specification is a must then. Luckily, the differences are not too severe from what we saw so far.
  - Stefan van Waasen 10:29 AM Make a close conection to the quantum community and astro physics. They use CMOS for cryo applications as we do it in Juelich.

- Nathalie Seguin-Moreau 10:28 AM ”ASICs outside CERN”
  - will there be possible ASIC design outside CERN ?
- Erik Heijne 09:59 AM
  - If particle physics as a whole can put their 'act' together, it can represent a reasonable buying power, even for industry such as TSMC or Sony. CERN would be the logical center for such representation, but CERN should not give an 'imperialistic face towards the national institutes and universities. In the microelectronics group we tried...

POLL :

1. Do you think its vital to go to very advanced CMOS technologies for future FEE?
2. How do you see the organization of future design teams (centralized, distributed, etc)
3. how to get the specs ans system level inputs
4. IP sharing and legal terms
5. Do you think we need to invest in R&D on 3D integration?