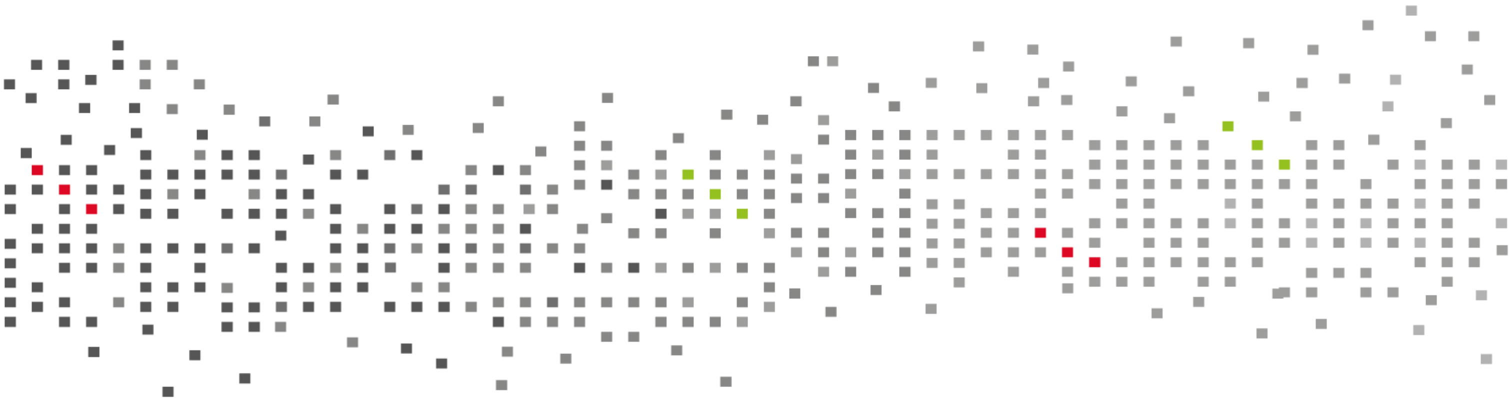
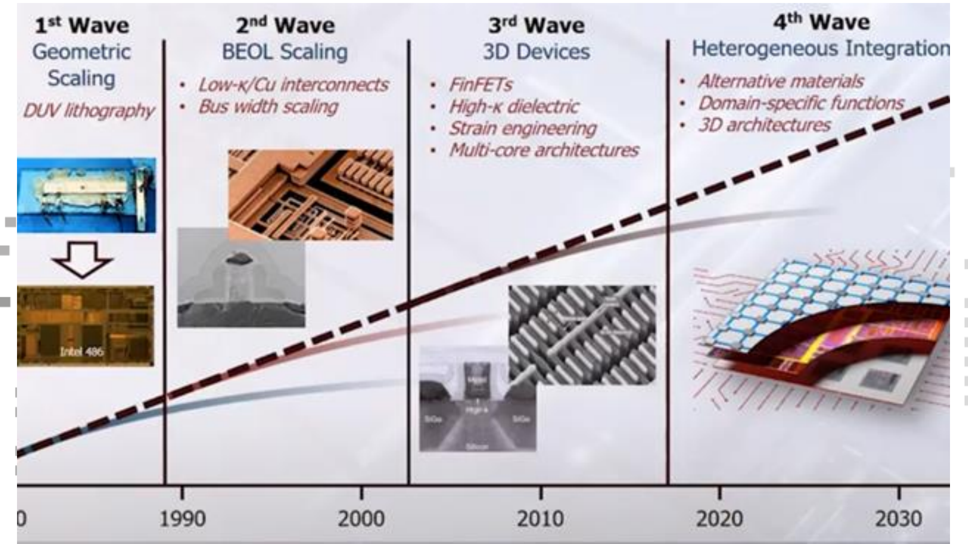




3D INTEGRATION IN NANOELECTRONICS

ECFA Detector R&D Roadmap Symposium of Task Force 7 Electronics and On-detector Processing

Christophe Wyon, March 25, 2021

leti ceatech

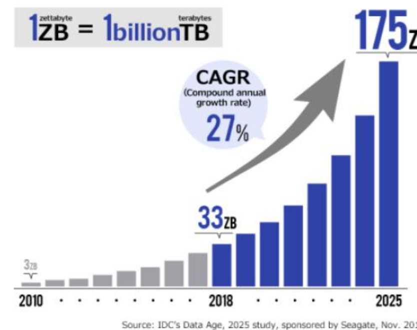
MAIN TECHNOLOGY DRIVERS TO MOVE TOWARD 3D INTEGRATION

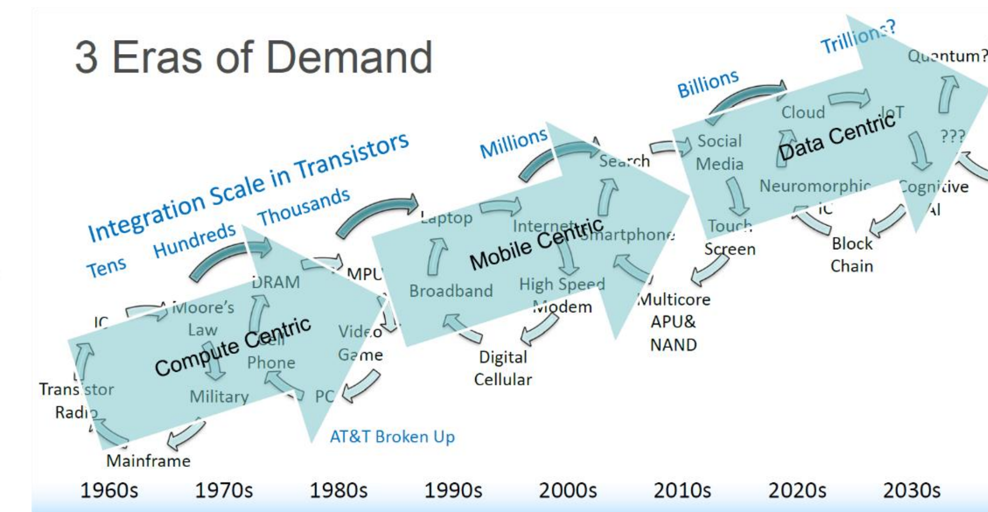
2D-Moore’s law is slowing down

- **Technical issues and associated Costs to:**
  - **Produce the chips:**
    - 2-3nm fab. => CAPEX: 30B$
    - EUV Litho: 120-150M$ for 7nm
  - **Design the chips:**
    - 7nm => 300M$
    - 5nm => 550M$

2 paradigm shifts

- **Move to a System Approach (SoC or SiP)**
  - **Parameters**:
    - Performance, footprint, form factor
    - **Energy consumption**
    - Cost
- **Move to a data centric paradigm**
  - Data is the fuel of our digital society
  - **Only 2% of stored data is used => AI**

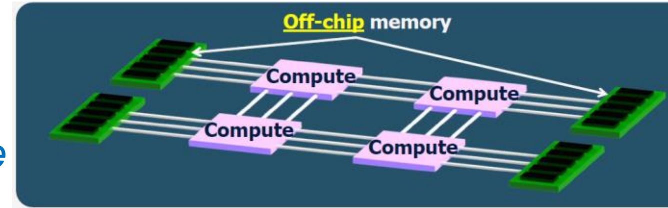


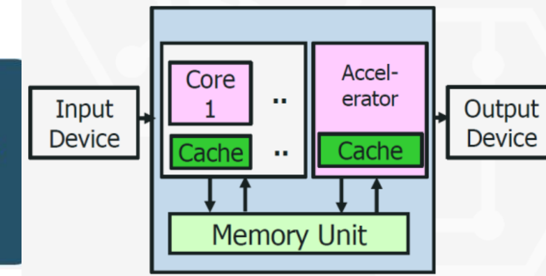


MAIN TECHNOLOGY DRIVERS TO MOVE TOWARD 3D INTEGRATION

Performance and latency

- Von Neumann architecture *Memory BW=* w_{bus} *f_{bus} *data rate*
- **Increase the interconnect density**



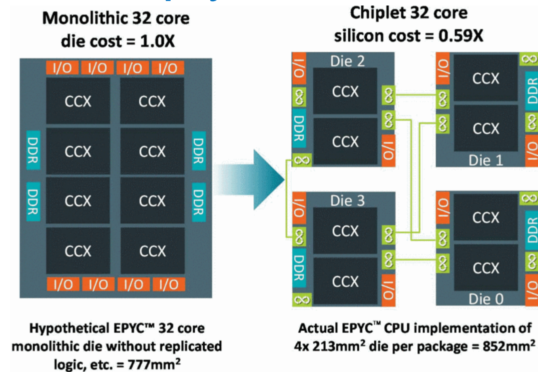


Power/Energy consumption

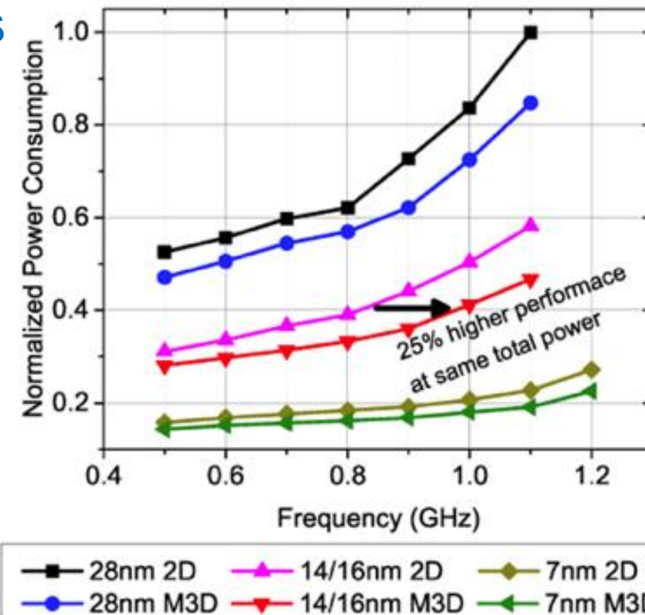
- Bit: PE ⟺ memory consumes a lot
- Power for moving a bit in a conductor: *P= data rate*L/cross section(w)*
- **Reduce L and/or move to photonics**

Cost savings

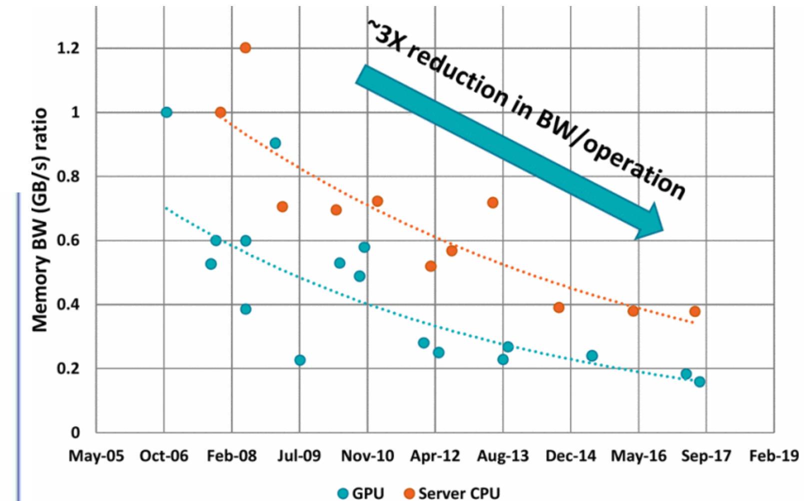
- Wafer cost increases with:
  - node and Si area
- Chip yield ↘ when Si area ↗



Lisa Su – IEDM 2017



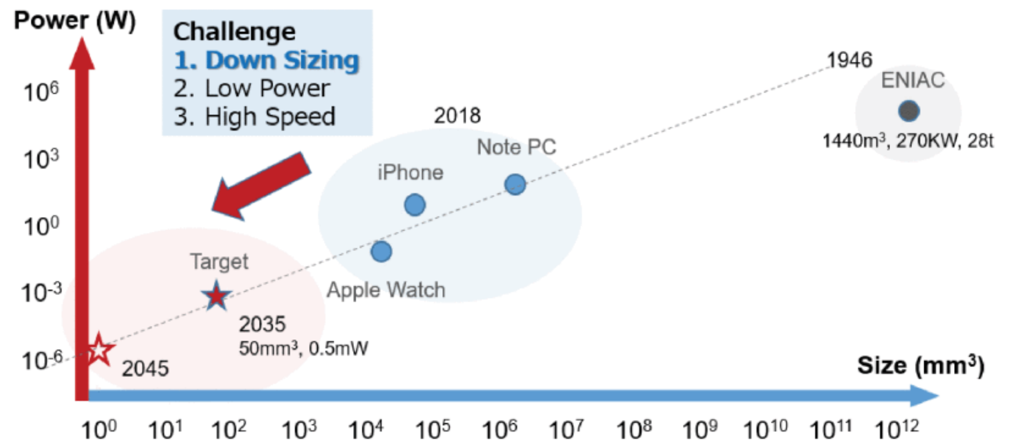
Sinha, 2020 – Monolithic 3D

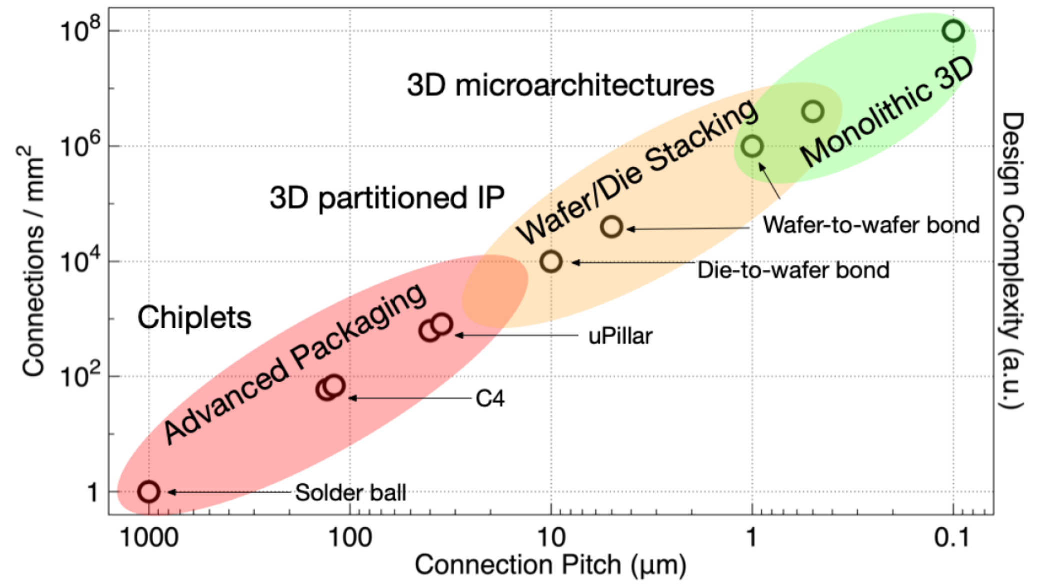


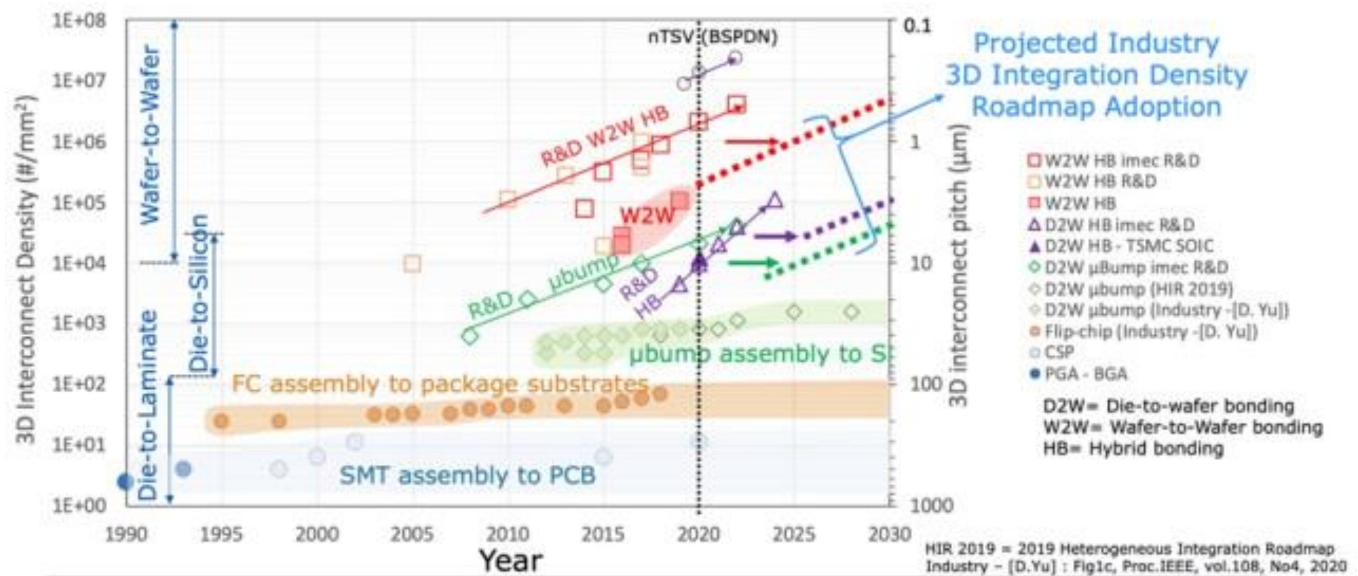
Memory bandwidth per operation in server CPU and GPUs

Lisa Su – IEDM 2017

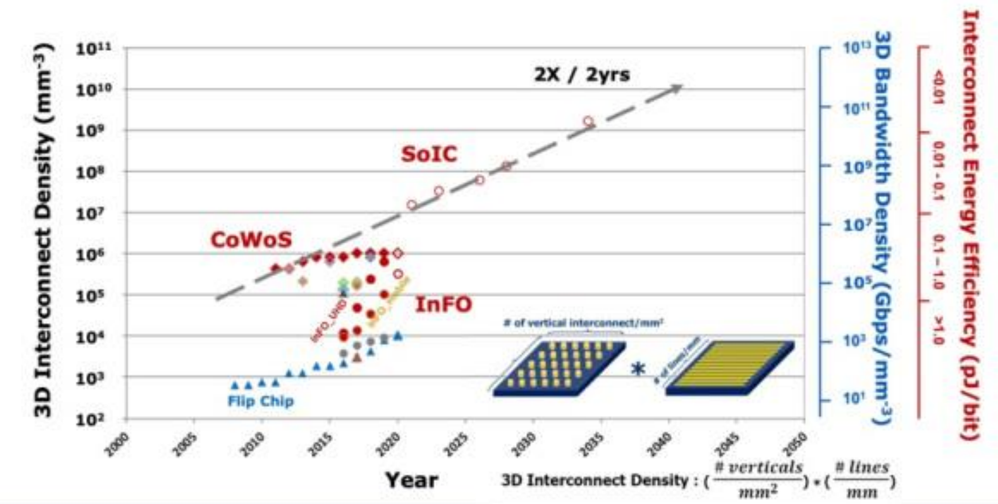
3D INTEGRATION ROADMAPS







Interconnect Scaling for Higher Bandwidth

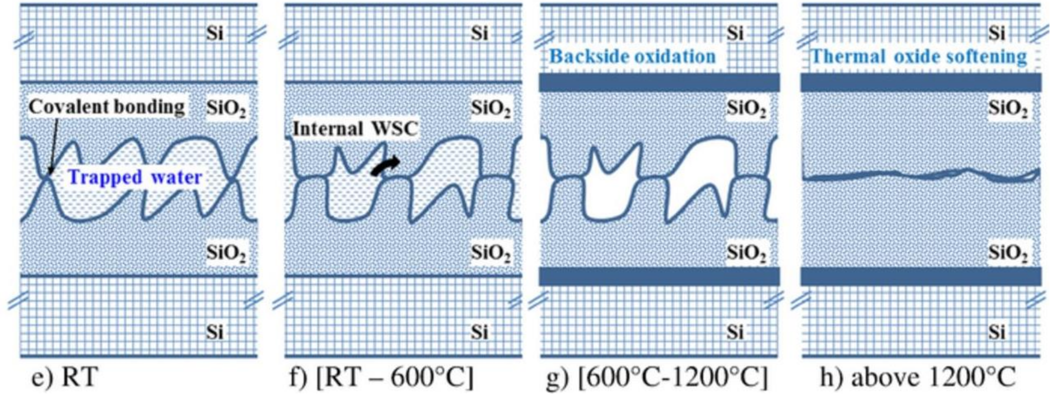


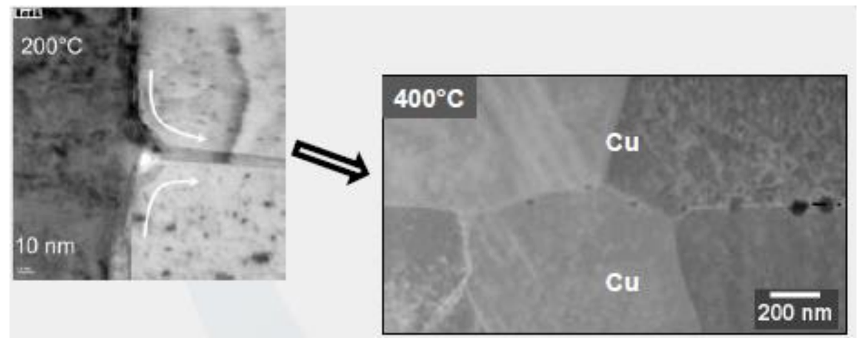
ISSC 2021

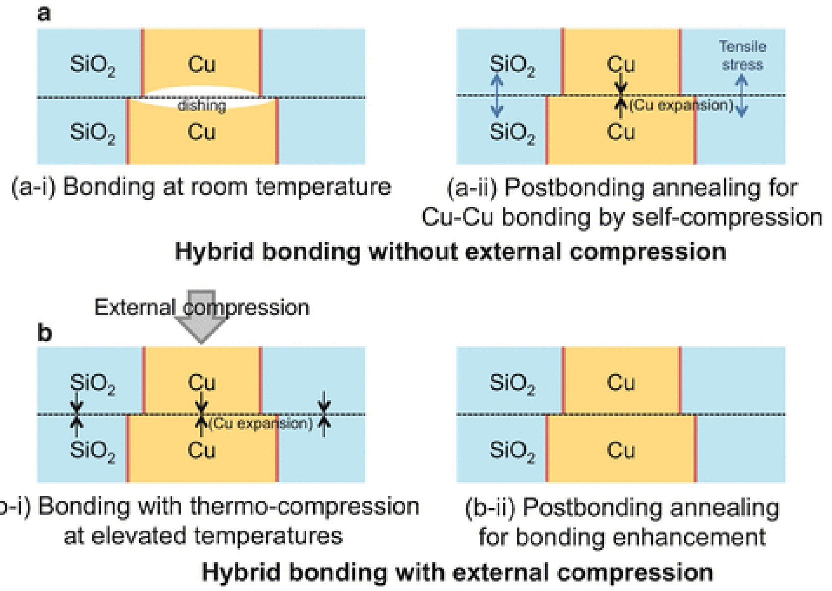
W2W (HYBRID) BONDING FOR DECREASING THE CONNECTION LENGTH (L)

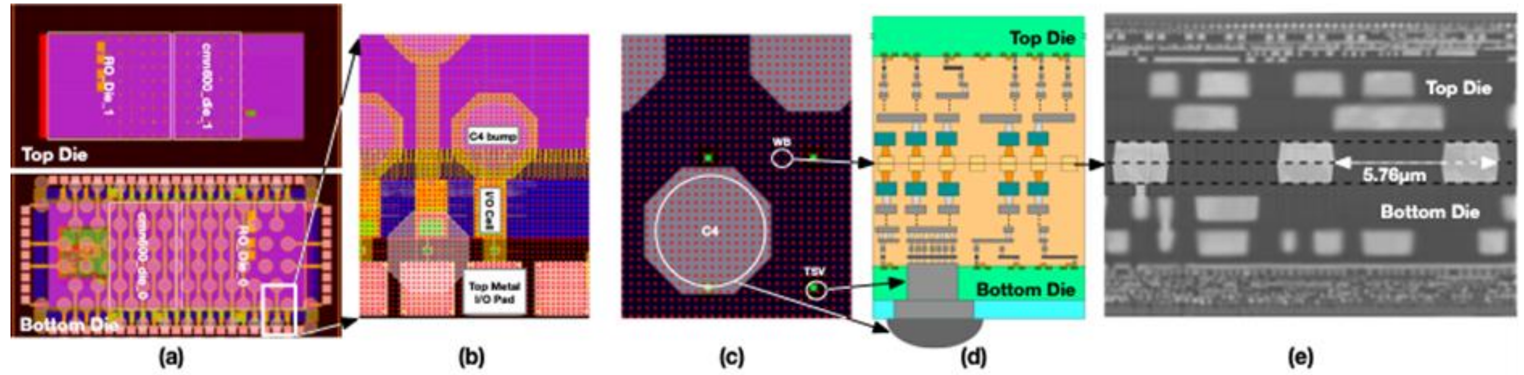
- **SiO_2-SiO_2 bonding: the most efficient**
  - Si-Si bonding not useful for 3D integration
- **Metal-Metal bonding**
  - Cu-Cu is widely used (Ti-Ti also works)
- **Hybrid Cu-SiO_2 bonding** => replace TSV
  - Used for W2W and D2W bonding

Fournel, 2015

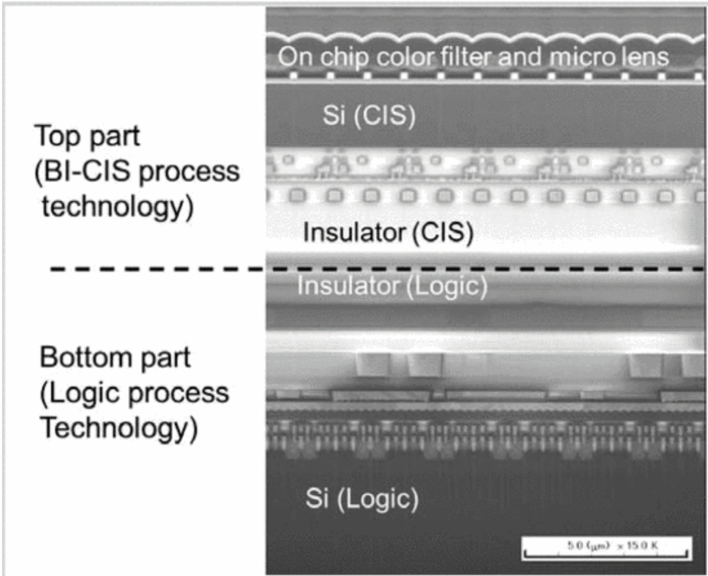








W2W HYBRID BONDING: CMOS IMAGE SENSORS

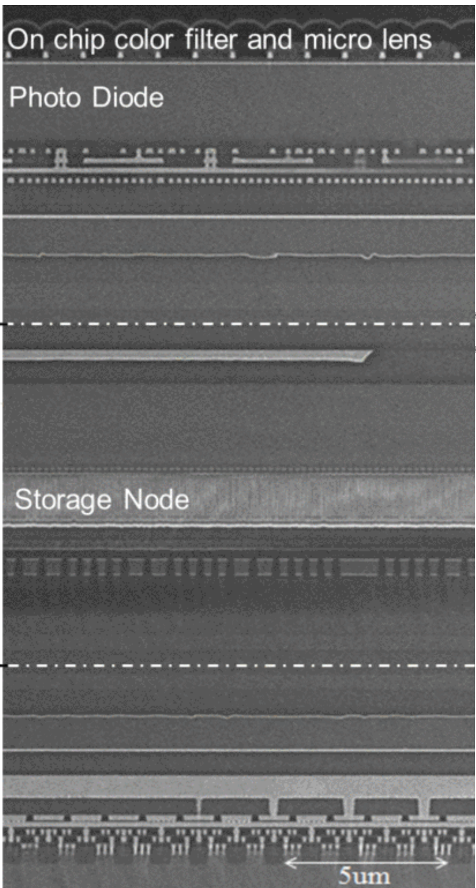


Sukegawa, 2013

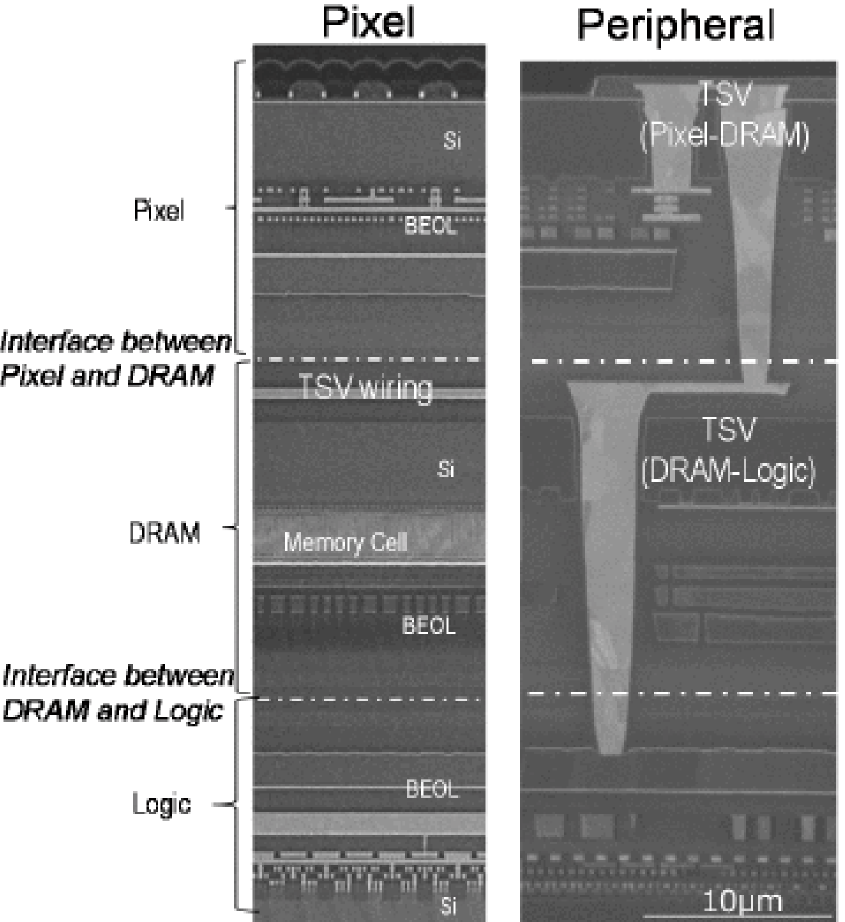
Top part
(BI-CIS process technology)

Middle part
(DRAM process technology)

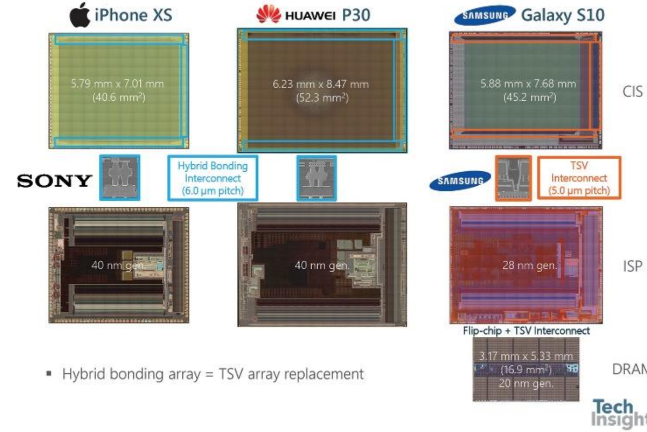
Bottom part
(Logic process technology)



Haruta, 2017



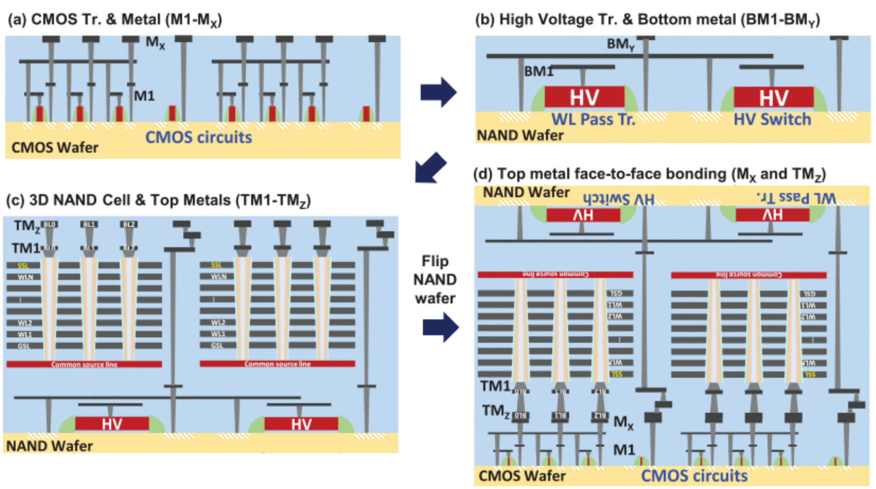
Kagawa, 2019



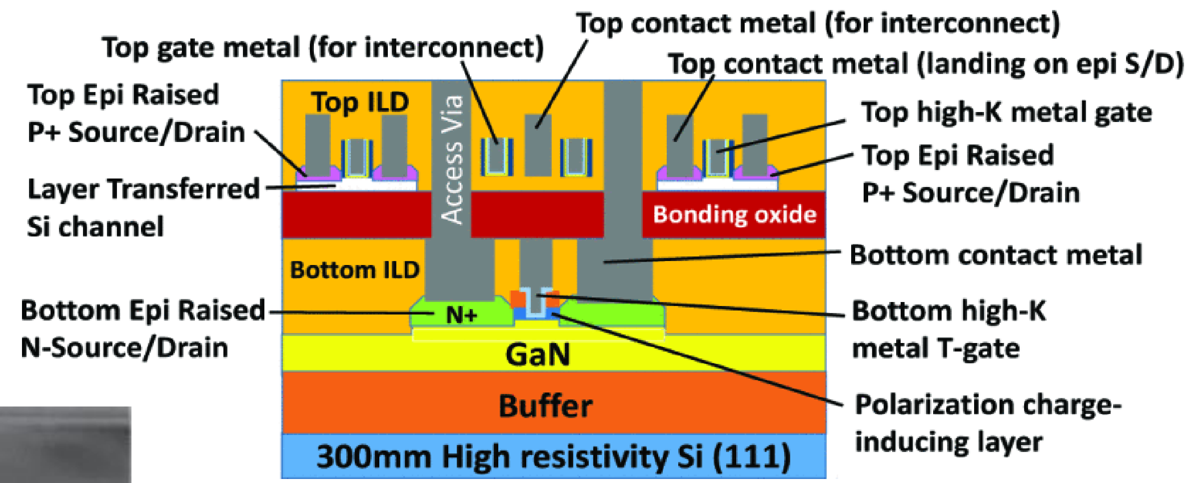
The road to AI?

At least for inference

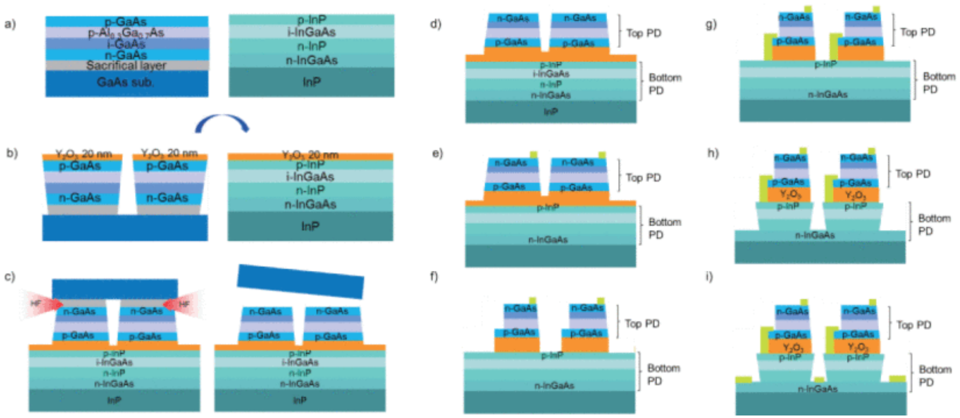
W2W HYBRID BONDING: OTHER EXAMPLES

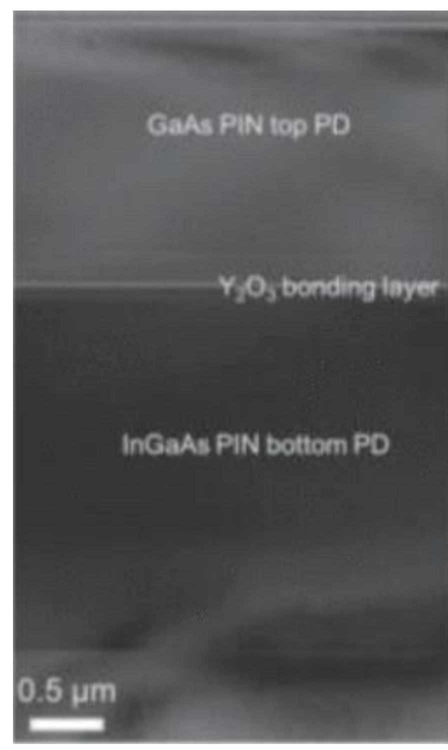


NAND memory on CMOS



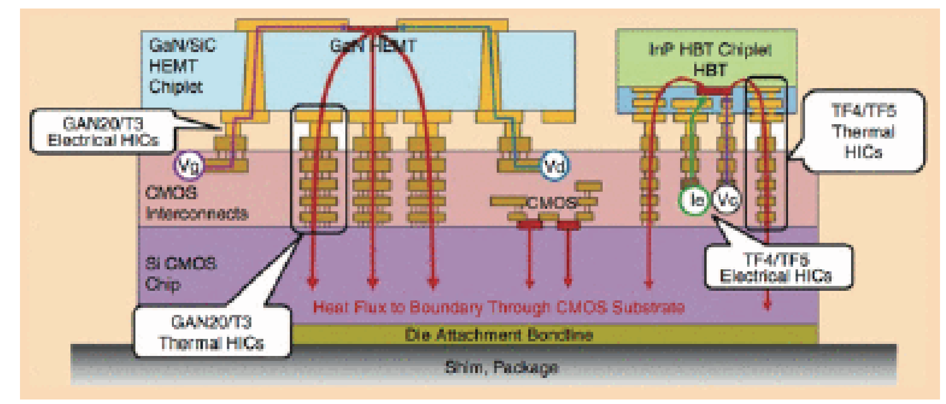
GaN/Si (111) on CMOS/Si (100)





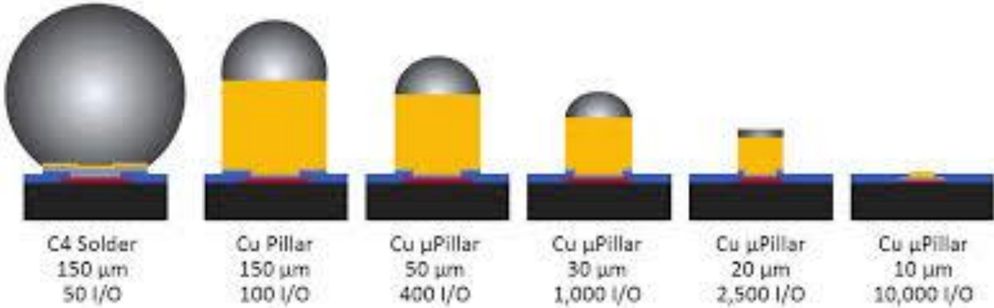
GaAs on InGaAs thru Y_2O_3

Multi-color detection Geum, 2019

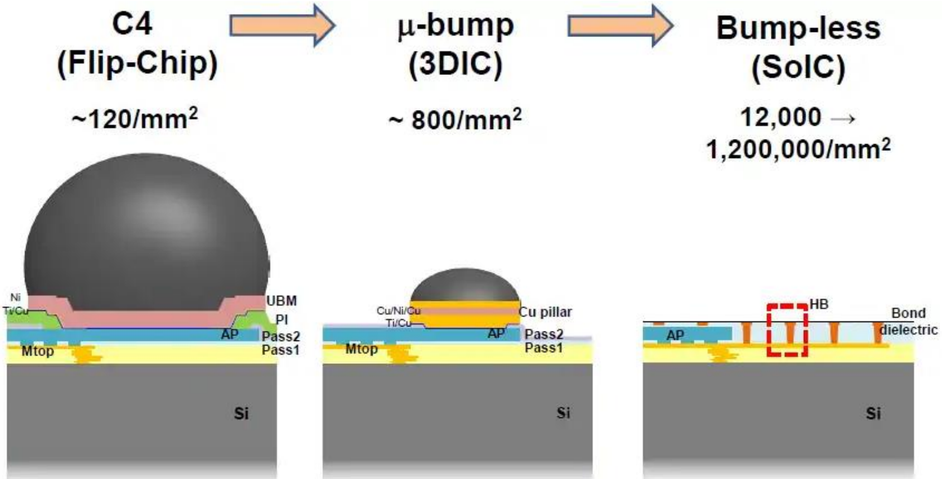


GaN & InP on CMOS for RF applications

CU PILLARS FOR INCREASING THE CONNECTION DENSITY AND DECREASING L



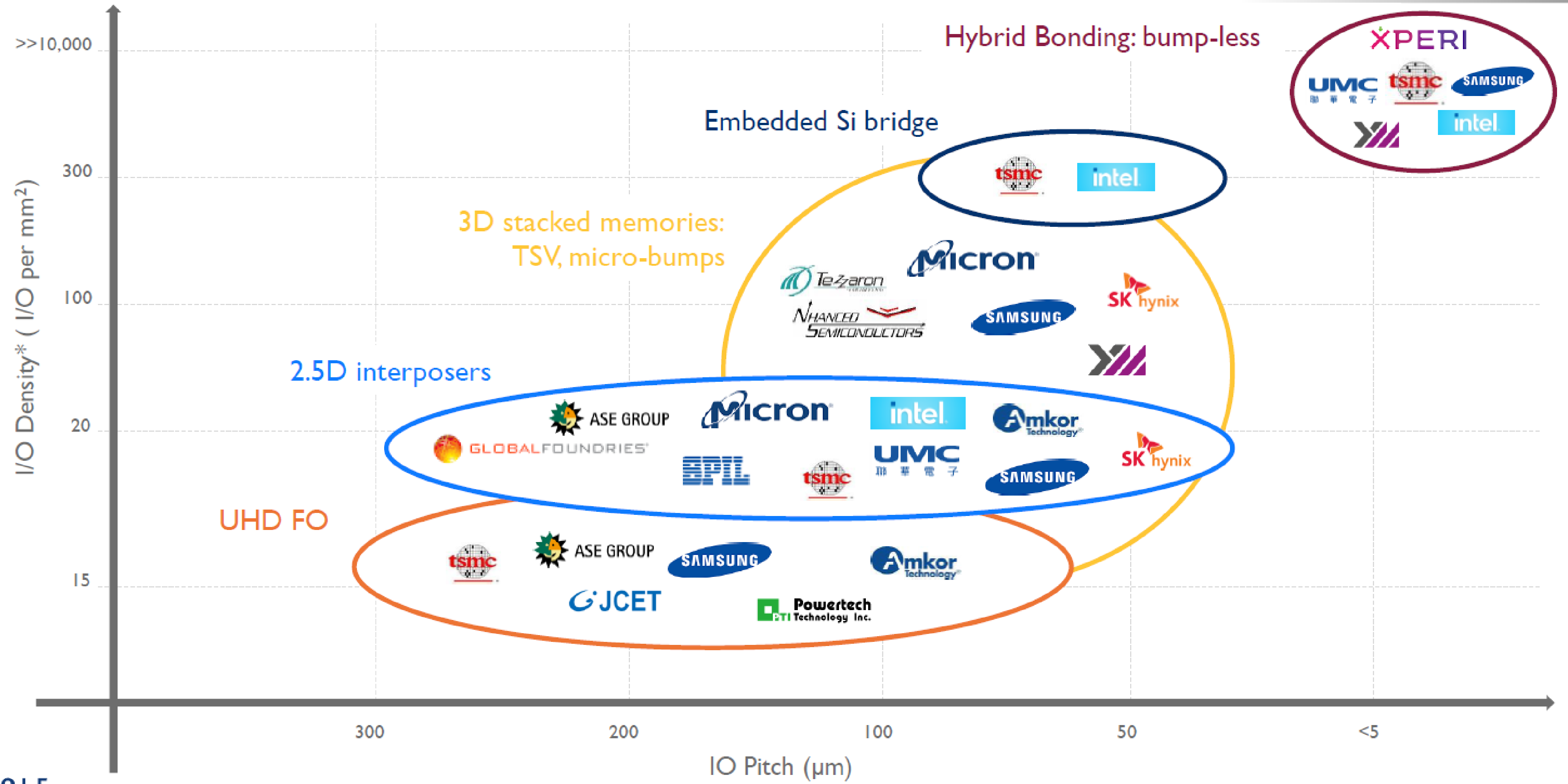
Decrease in the thermal resistance of interconnections



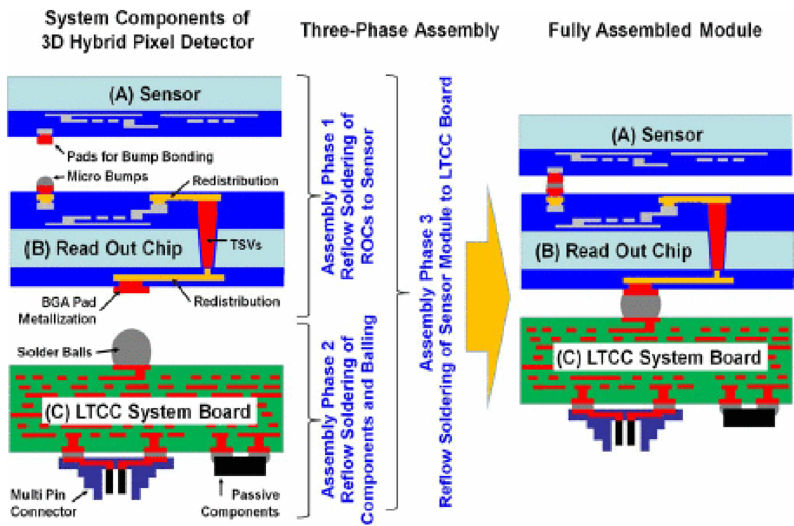
Technology	2.5D	3D-IC	SoIC
Structure cross-section	SoC1 SoC2 µbump BEOL Interposer	SoC1 µbump SoC2	SoC1 SoIC Bond SoC2
Interconnect	µbump + BEOL	µbump	SoIC bond
Bump Density	1.0X	1.0X	16.0X
Speed	0.01X	1.0X	11.9X
Bandwidth Density	0.01X	1.0X	191.0X
Power Efficiency (Energy/bit)	22.9X	1.0X	0.05X

TSMC

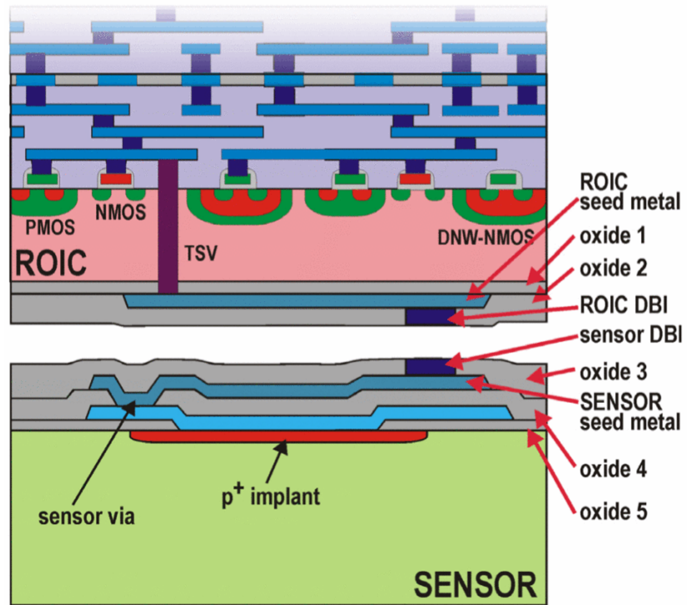
ADVANCED 3D INTEGRATION TECHNOLOGIES ARE AVAILABLE



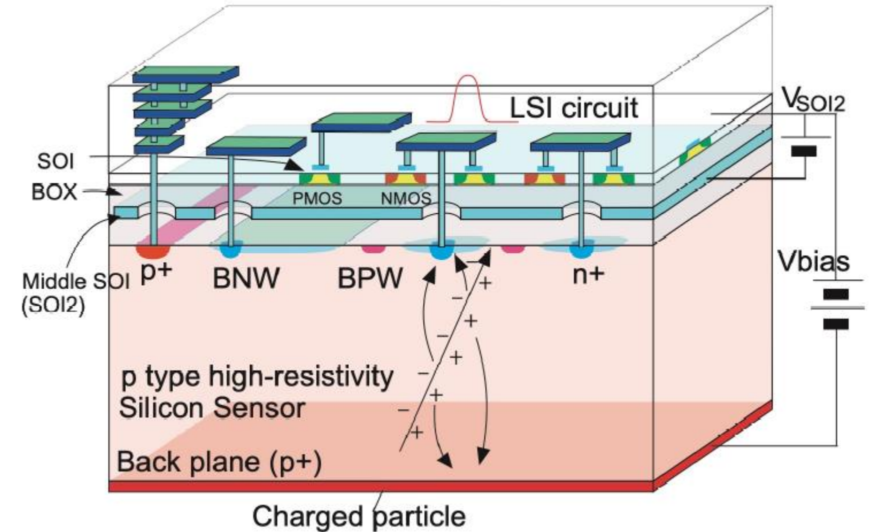
3D INTEGRATION: X-RAY AND PARTICLE DETECTORS

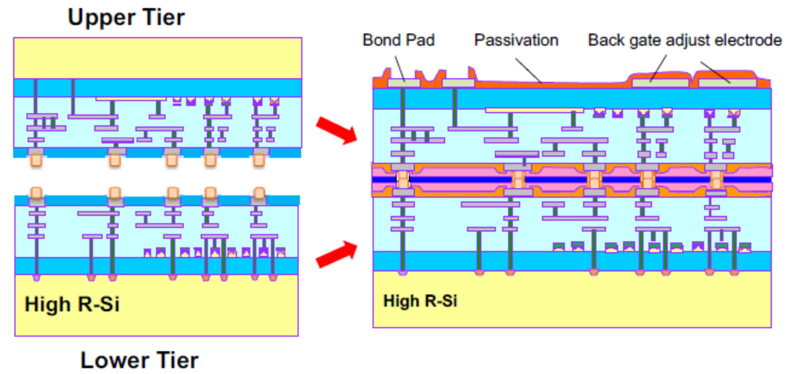


Zoschke, 2017



Deptuch, 2016





Yamada, 2019

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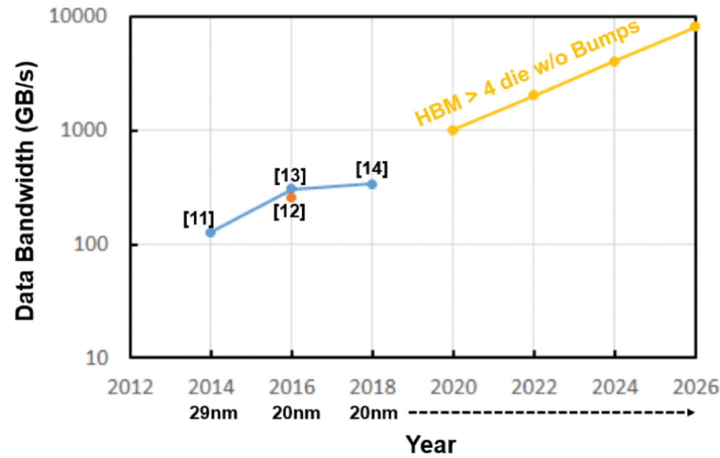
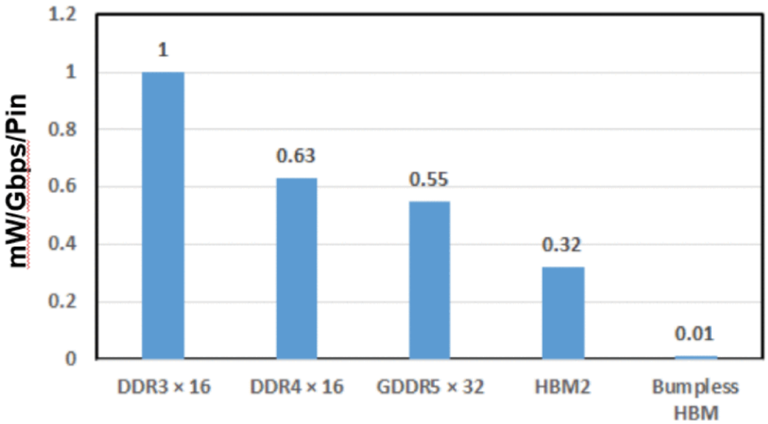
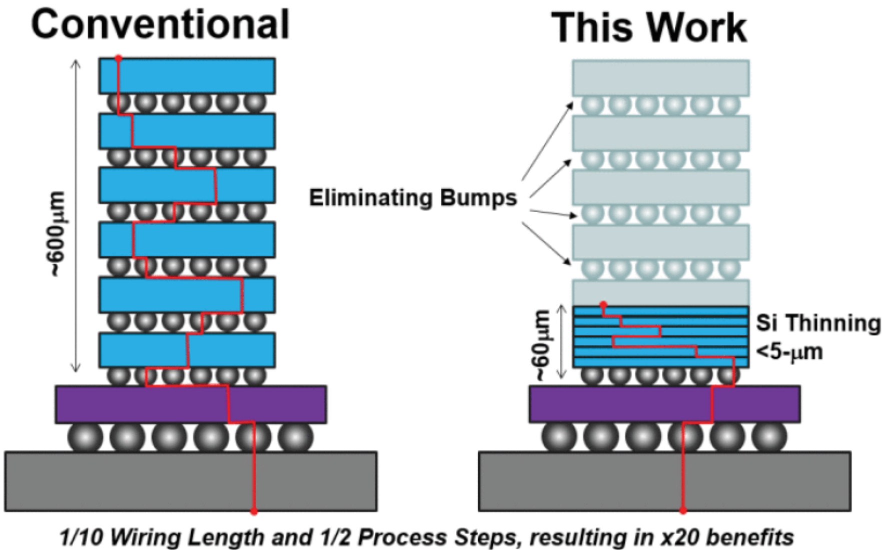
WHAT'S NEXT: INCREASE IN INTERCONNECT DENSITY

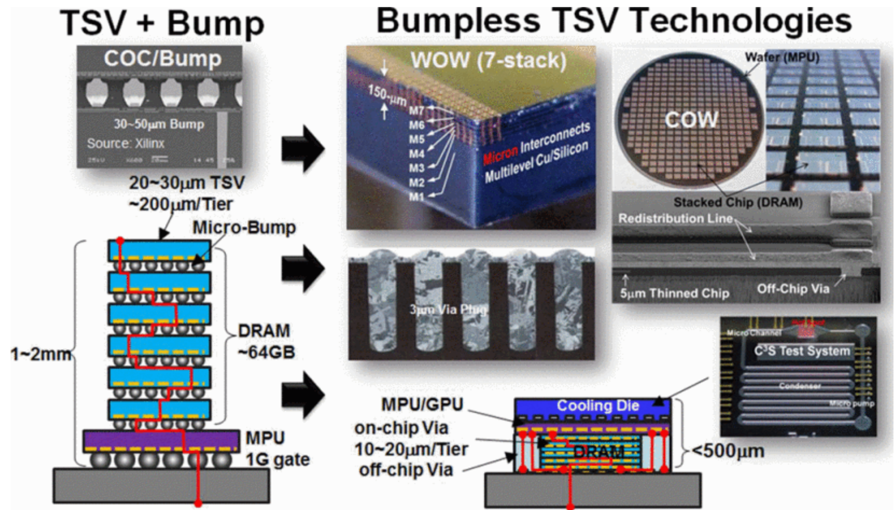
Development of:

- **Bumpless technology**
- **Wafer thinning**
  - Si down to 4-5µm (=> 0.5µm)
    - Glass down to 50µm
  - Reduce L and Aspect Ratio for TSV



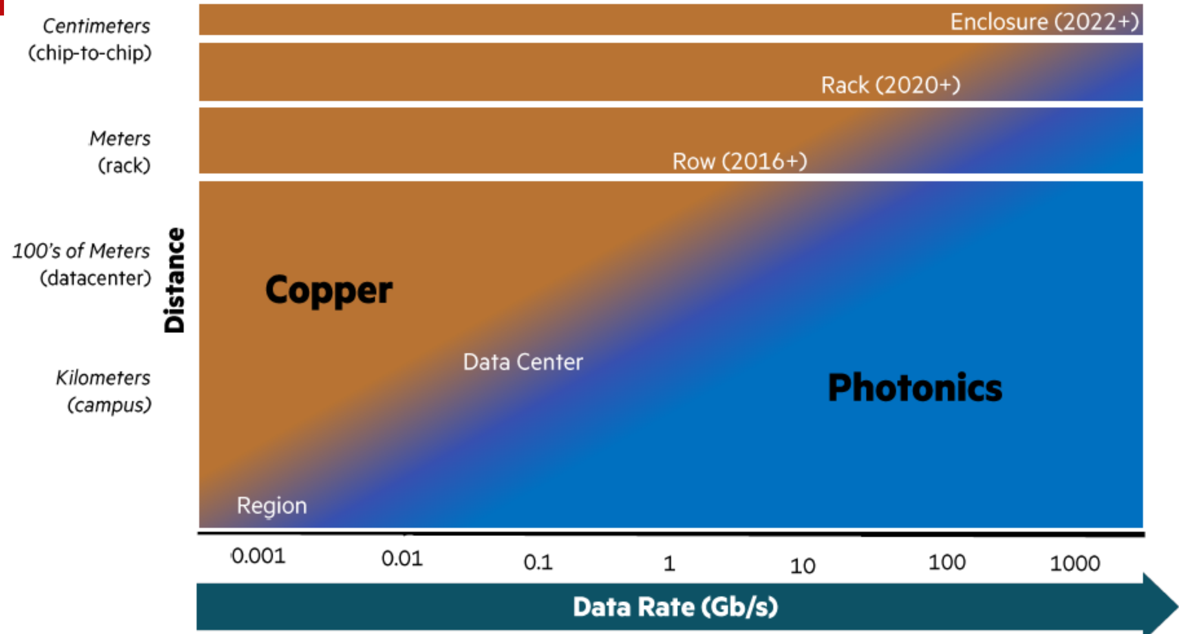


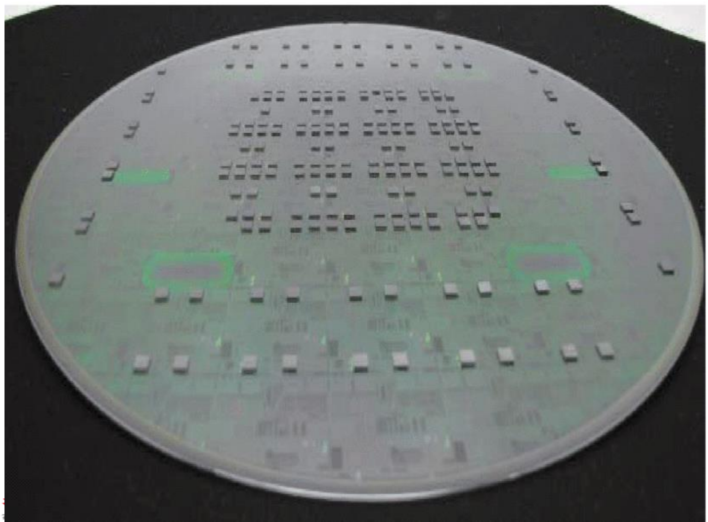


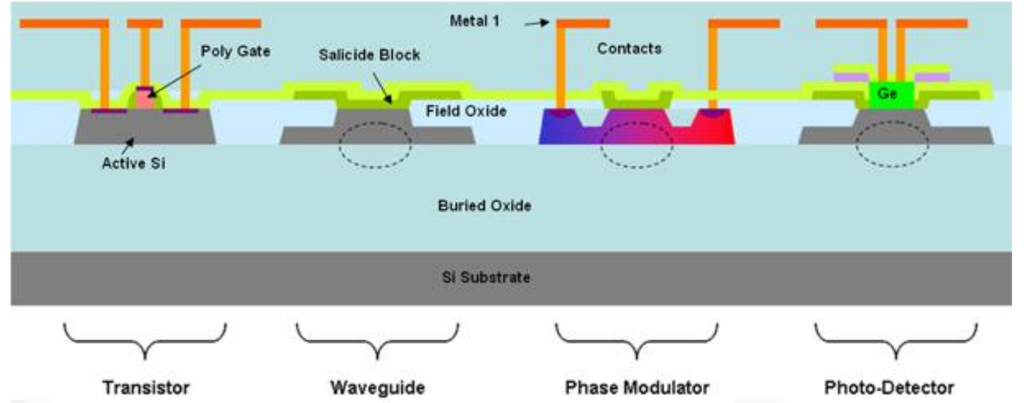


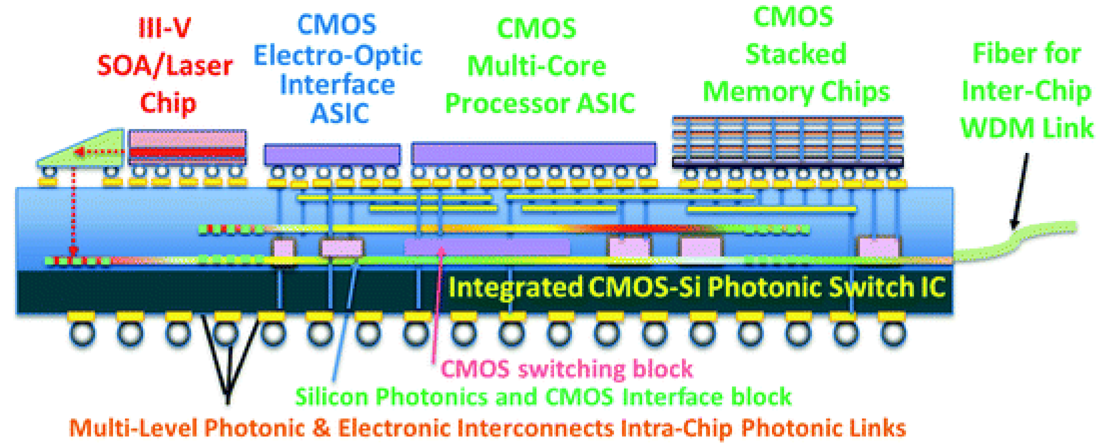
Sakui, 2019

WHAT'S NEXT: SI PHOTONICS



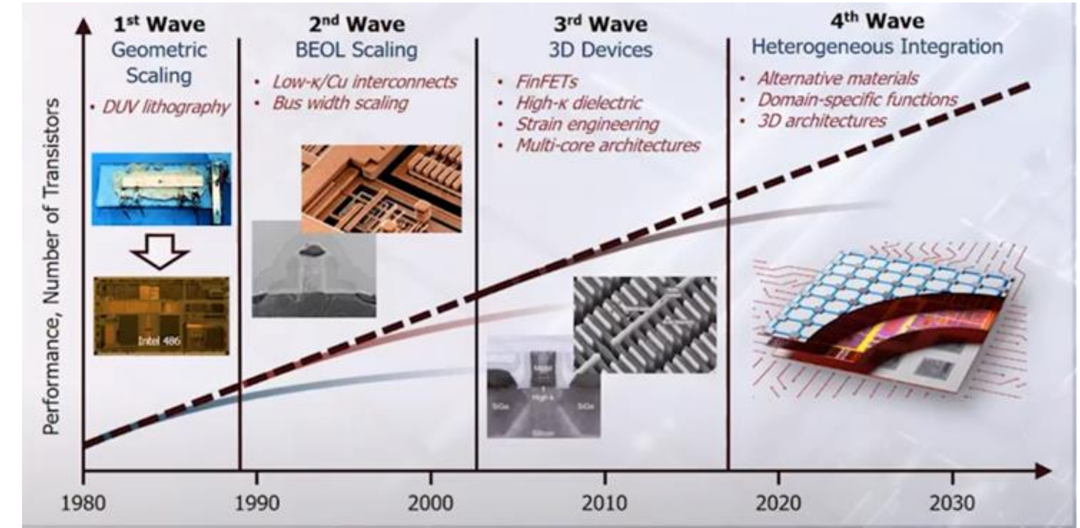


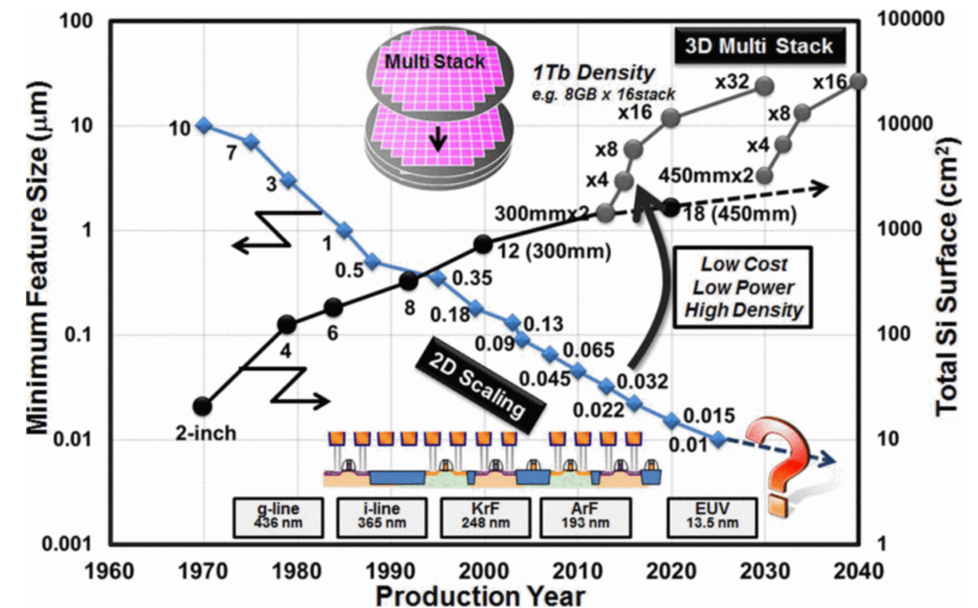




TAKEAWAYS

- **A wide technology tool box is available for achieving reliable and robust 3D integration**
  - One can almost stack anything on anything
  - Next phase of Moore’s law
- **Main technology drivers for 3D integration:**
  - Cost, performance, power consumption
- **Some issues remain**
  - DTCO: design/technology coordination
  - Thermal, thermo-mechanical stresses, EM
  - Cost
- **What’ next?**
  - Increase in interconnection density
  - Wafer thinning => reduce L and AR for TSV
  - Si photonics





Thank for your attention

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