SHIP: FE ELECTRONICS

SHIP JOINT PHYSICS AND DETECTOR MEETING: VACUUM VESSEL WORKSHOP

12.02.2021 I D.ARUTINOV

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GENERAL INFORMATION

- **core element of FE electronics is an mutli-channel ASIC w/ analog and digital functionality**

- **single FE unit per single or several adjacent LS-BOXes (2 WOMs a Box)**

- **sensor H-Voltage supply, housekeeping, cooling → separate from ASIC control electronics**

- **general powering → possible options: serial powering / POE / …**

- **intermediate concentrator not touched yet (will be explained briefly later)**

- **mechanical design not touched yet but has been discussed with other FZJ institute - ZEA-1**
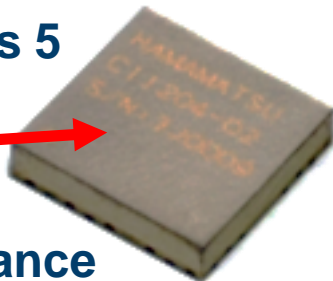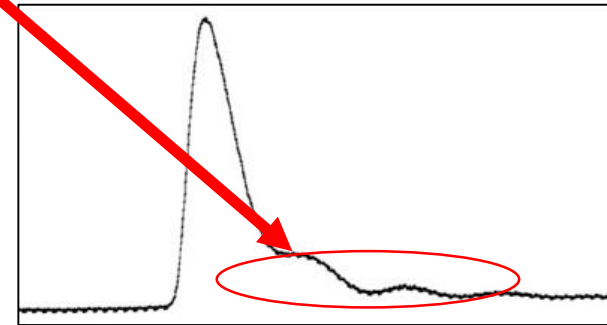
FE CONCEPT

SiPM PCB

WOM
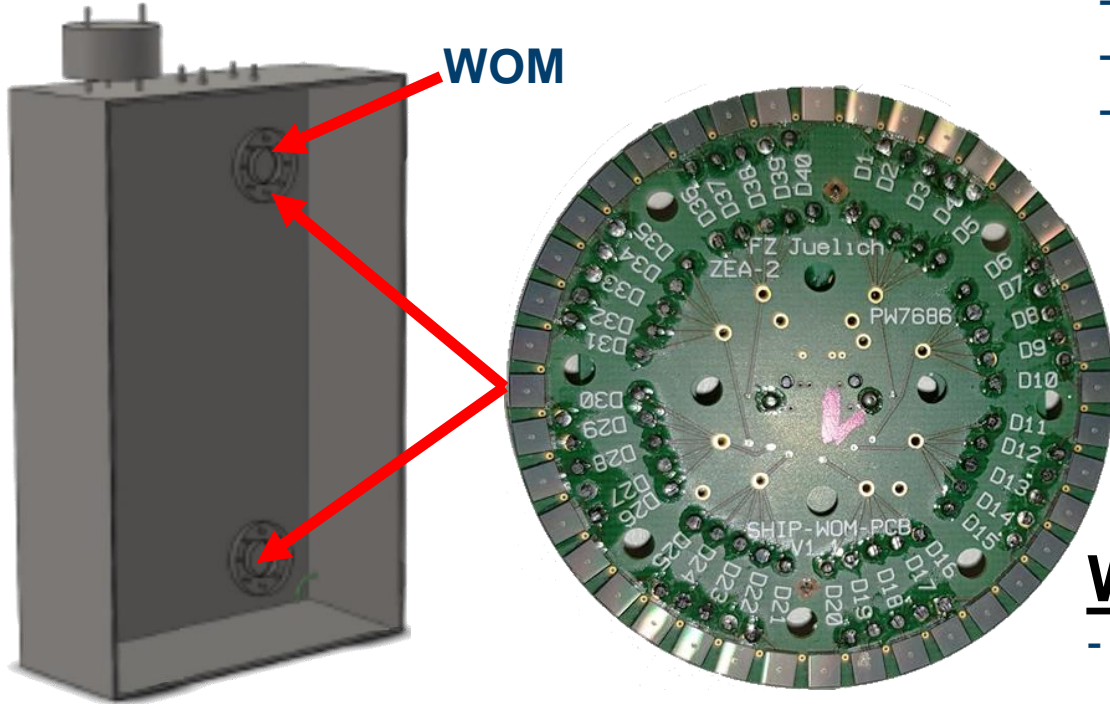
LS-BOX
- 2 WOMs = 2 PCBs

WOM PCB (current version)

- 40 SiPMs grouped (in parallel) in 8 channels 5 SiPM each
- SiPM: Hamamatsu 14160 (3×3mm)
- a switch to select number of SiPMs / group
- footprints for components to adjust impedance

WOM PCB (next version)

- will include temperature control & HV Chip (to test concept)
- adjusted impedance matching
- test components might be removed
- different connector for readout

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FE CONCEPT

Signal Receiver Chain

12 - 16 ADC in one ASIC, variable to combine for higher clock or ENOB

Programable Input Impedance 10 – 100Ohm

Programable Bias Built in Self Test

Internal Clock Generation

Receiver ASIC

GEneral **R**ead **O**ut **L**ow Power **D**evice

(GEROLD)

→ high performance
→ low energy consumption
→ small footprint

- Interface to ext. Processor
- slow I/Os
LVDS Interface to link up with other ASIC

Data ordered by timestamp and zerosuppression

Highspeed Interface to optical converter for up to 100m Data upload

Built in SRAM Memory to lower Bandwidth requirment to average

LVDS Interface to link up with other ASIC

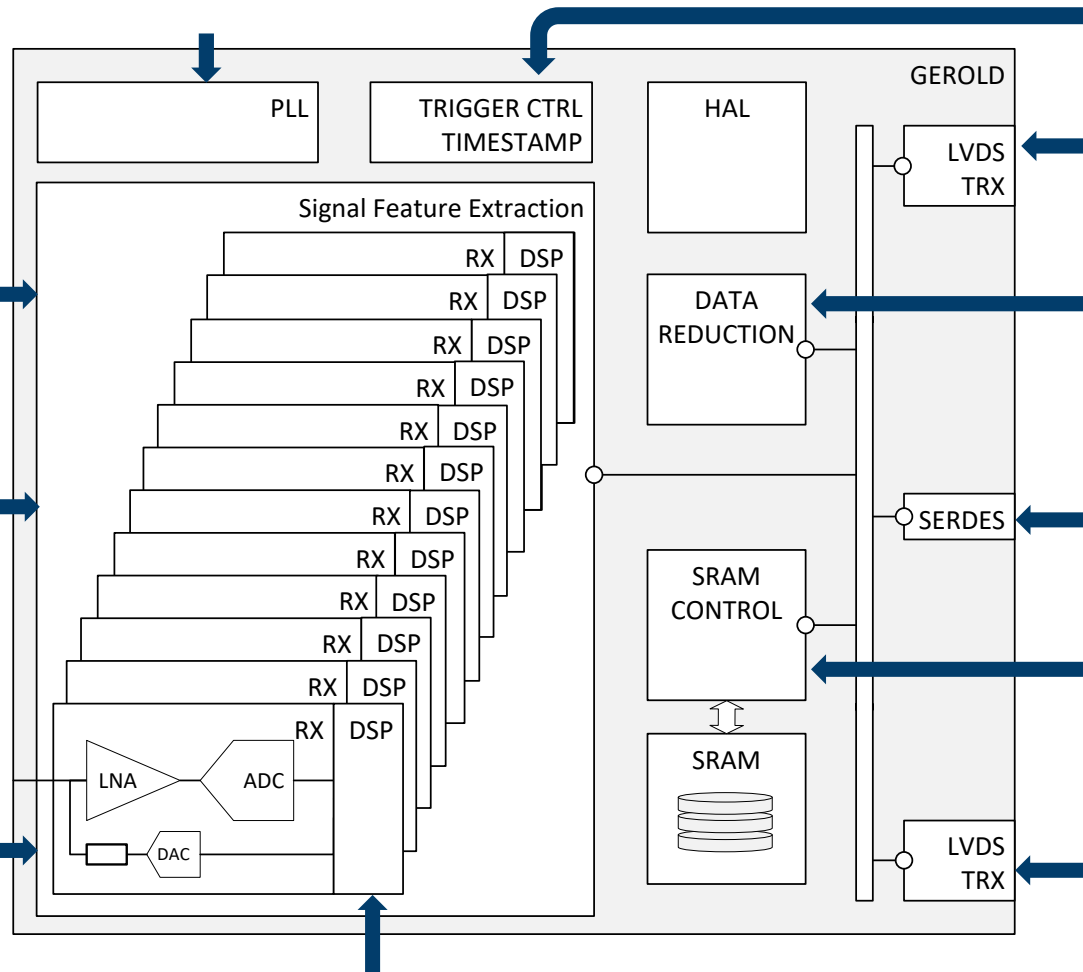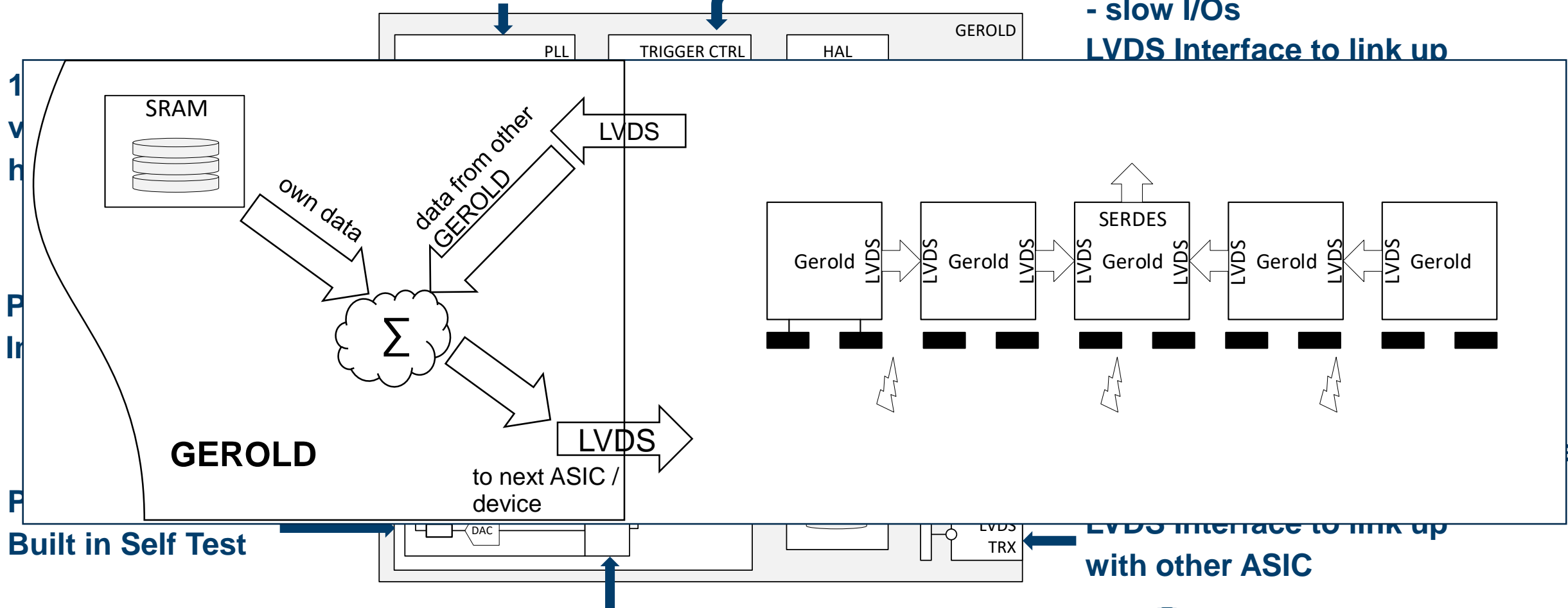**Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…**

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FE CONCEPT

Signal Receiver Chain

Internal Clock Generation

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- slow I/Os
LVDS Interface to link up
with other ASIC

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FE CONCEPT

Signal Receiver Chain

Internal Clock Generation

- Interface to ext. Processor

- slow I/Os

LVDS Interface to link up

GEROLD

PLL

TRIGGER CTRL

HAL

SRAM

own data

data from other GEROLD

LVDS

Σ

GEROLD

LVDS

to next ASIC / device

SERDES

Gerold | LVDS | LVDS | Gerold | LVDS | LVDS | Gerold | LVDS | LVDS | Gerold | LVDS | LVDS | Gerold

DAC

LVDS TRX

Built in Self Test

LVDS interface to link up with other ASIC

Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…

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FE CONCEPT

FE PCB

- FE resides directly on LS-BOX
- FE interconnection topology of a cluster TBD
- hit data / housekeeping / slow control →
  SERDES/LVDS either optics or cooper
- number of concentrators depends on data rate
- concentrators KIS: most functionality → GEROLD
- concentrator protocol can be adjusted to any std.
- still a lot to do

CURENT ACTIVITY

- **implementation of GEROLD functionality in FPGA soon**

- **implementation of transceivers (LVDS / SERDES) soon (LVDS already ongoing)**

- **first engineering sample of ADC (28nm) taped out, being tested, second engineering run expected end 2021**

- **currently submitting 3 DFG proposals to support development**

- **define data protocol and hit rates**

- **SiPM PCB is being tested in Berlin**
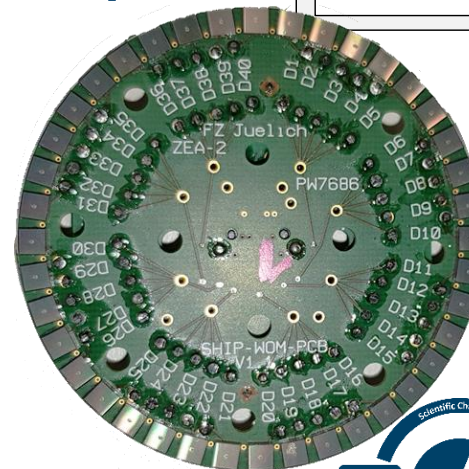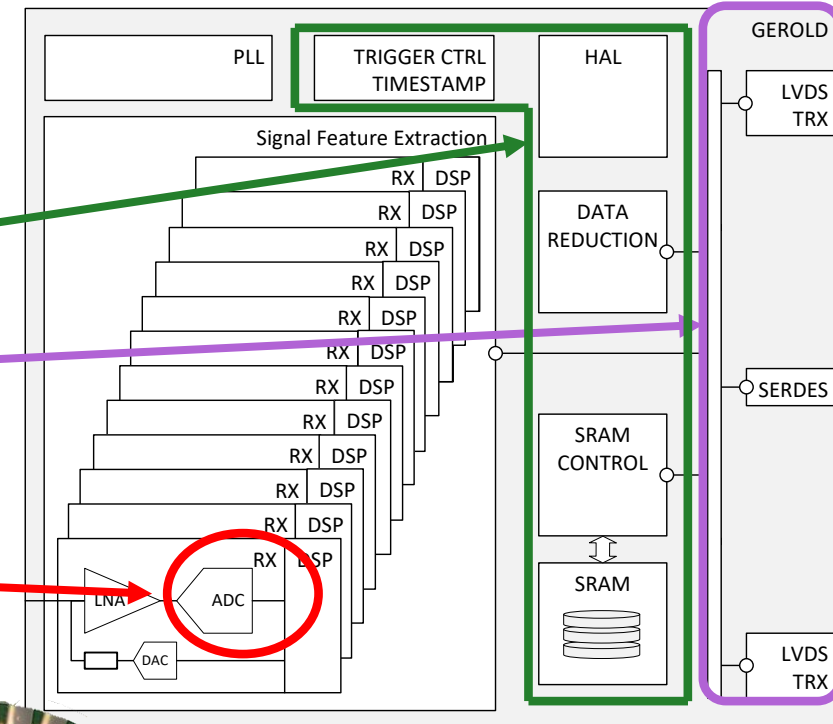
CURRENT GOAL

First "version" of GEROLD won't be an ASIC but a combination of

- **a PCB based test-bench with analog part containing 28nm ADC and other analog parts**

- **and FPGA board programmed to mimic desired digital functionality of GEROLD**

- **should be tuned towards test-beam requirements and be tested under realistic conditions**