ebg MedAustron

cosylab
CONTROL SYSTEM LABORATORY

Power Converter Controller Overview

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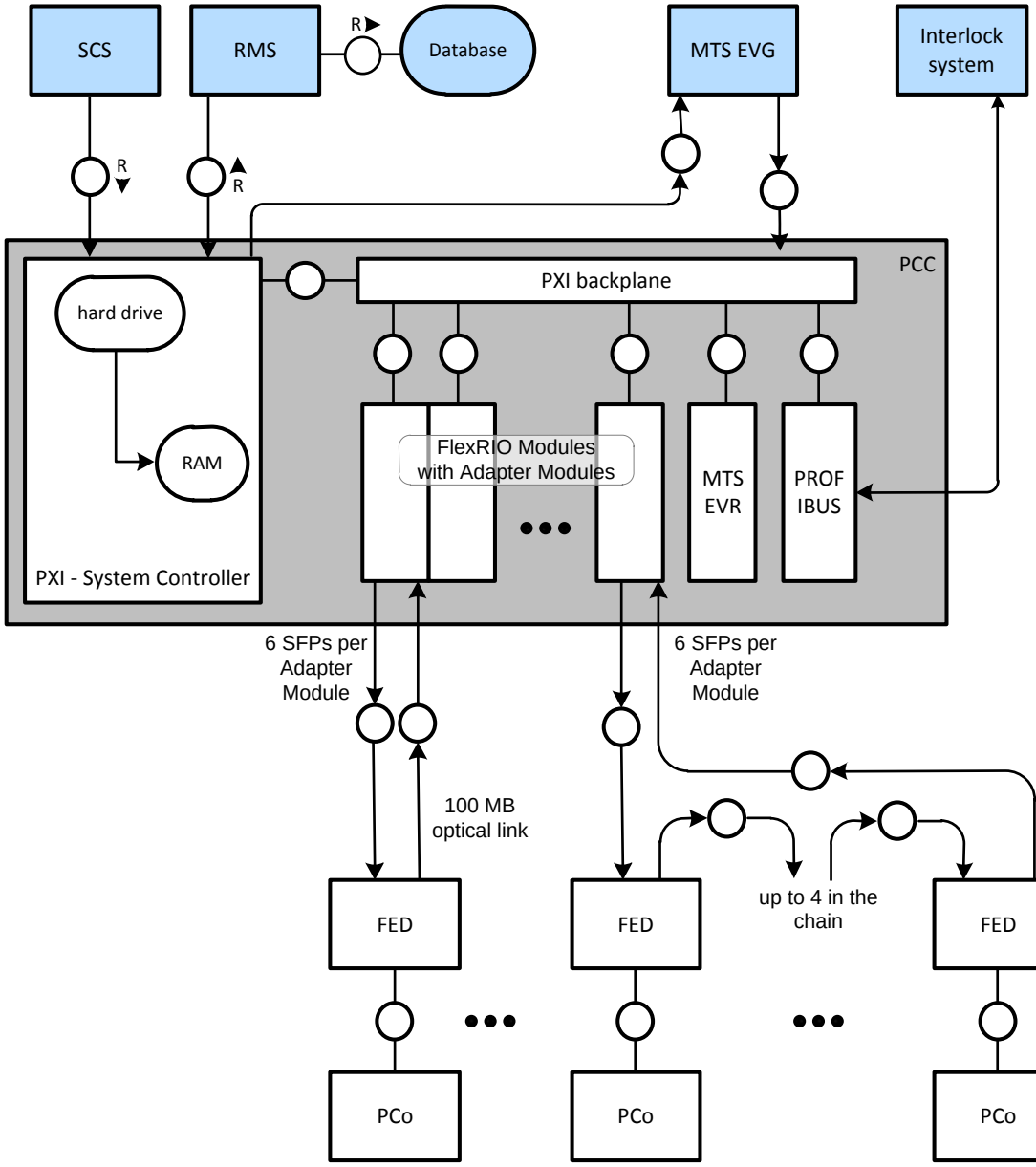
Outline

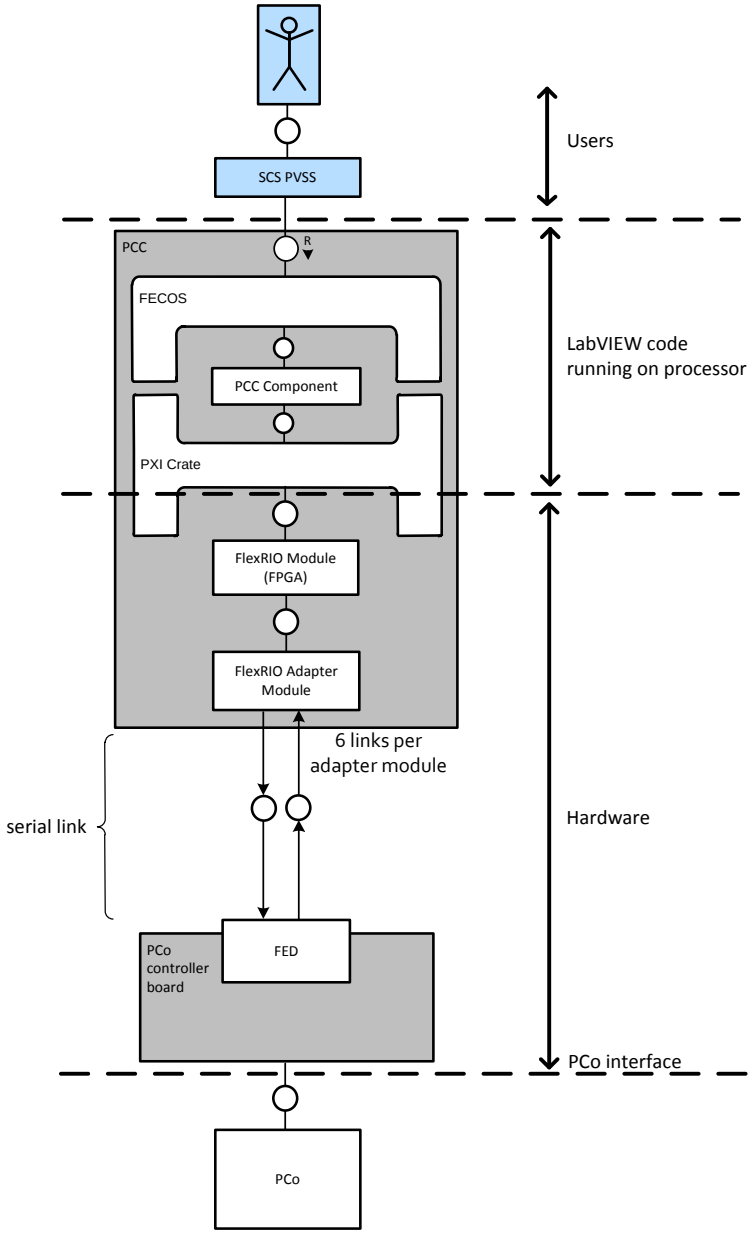
- CWO-2
- Power Converter Controller (PCC)
  - Quick overview
- Architecture design / implementation
  - PCC = PXI crate + FlexRIO Modules + Adapters
  - Fiber link
  - Front End Device
  - Power Converter interfaces
- Demo setup
- CWO-3

PCC activities in CWO-2

- added a few additional requirements
- designed detailed architecture
- moved architecture into EA model – traceability
- designing and manufacturing FlexRIO Adapter and FED prototypes
- implementing functionality for demo
- defining tasks for future CWOs

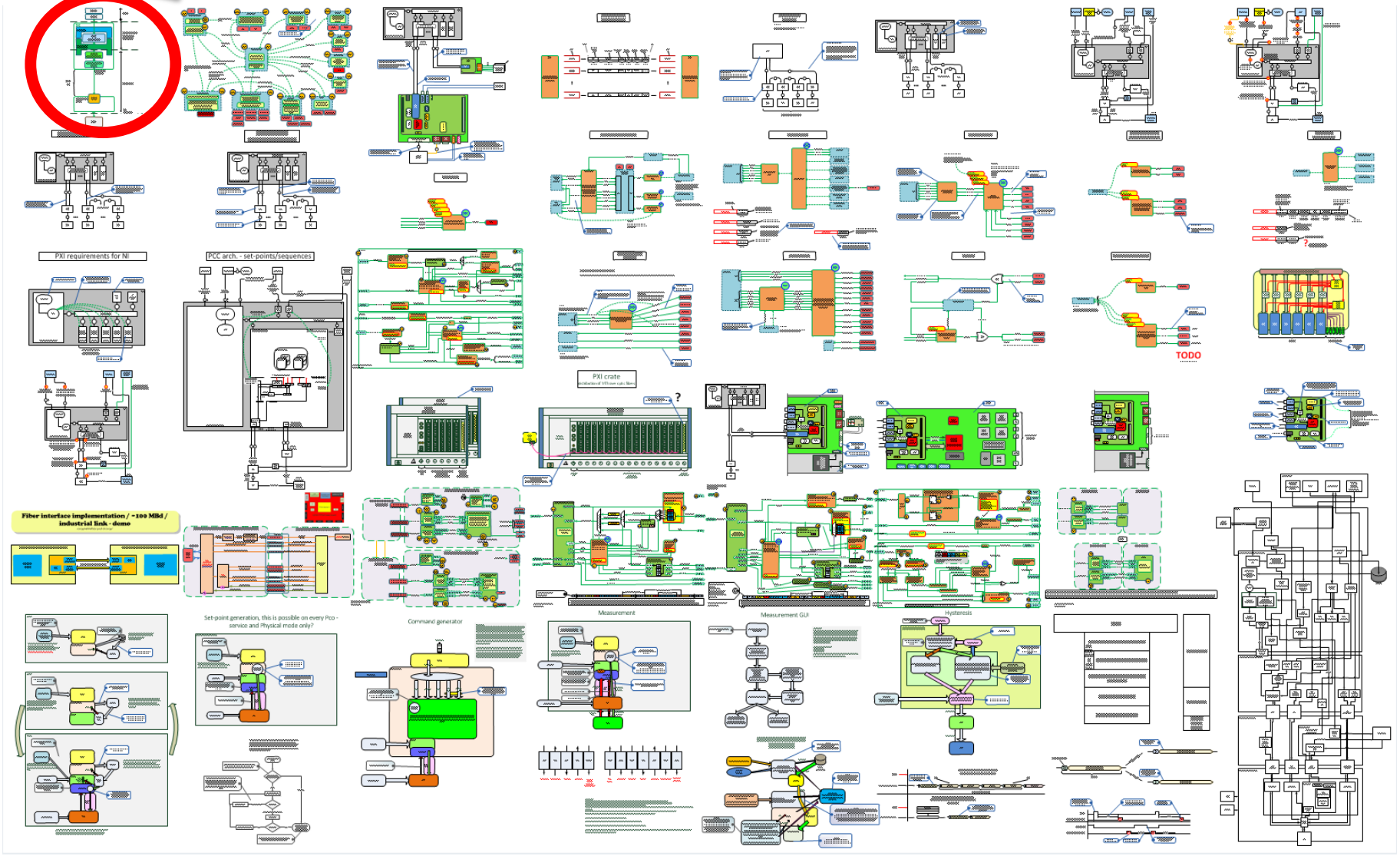
PCC – quick overview





PCC – detailed architecture

You are here

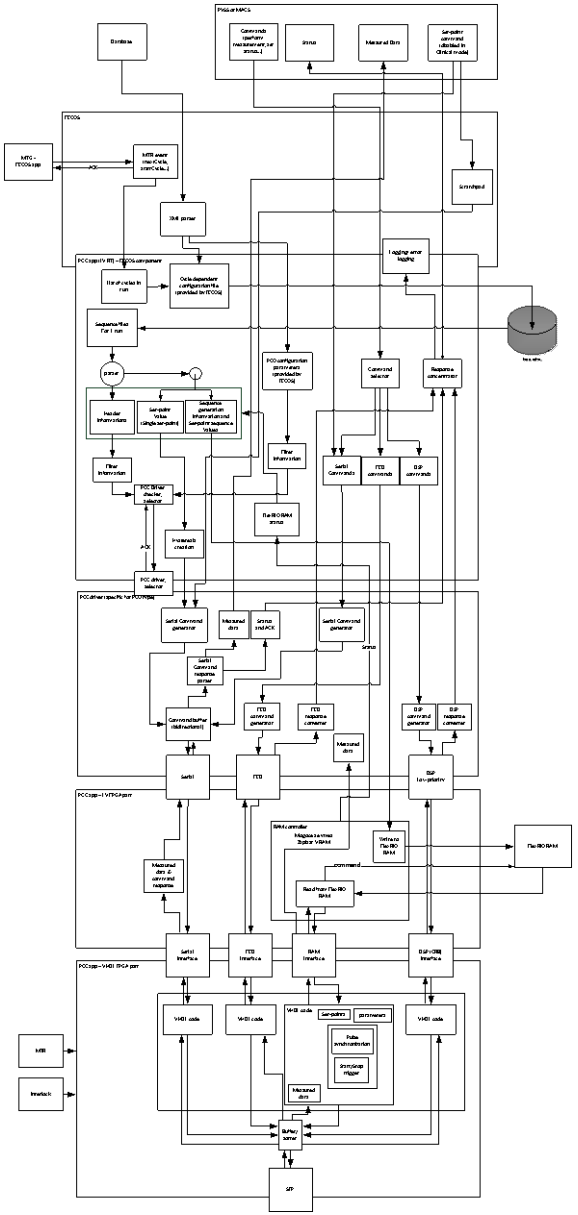


PCC – basic tasks

- Downstream (towards PCOs)
  - single set-point generation
  - sequence generation
  - transmission of commands
- Upstream (from PCOs)
  - reception of command responses
  - reception of measurements results
- How is it done?

PCC – how it's done?

That's how:



PCC – LabVIEW code

PVSS or MACS

Database

Commands (take measurement, set status...)

Status

Measured Data

Set-point command (disabled in clinical mode)

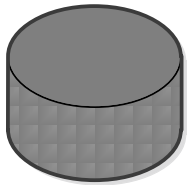
MTG - FECOS app

FECOS

- "everything comes from here, everything goes back to here"
- FECOS provides the PCC application with universal access to different types of interfaces (SCS, RMS, MTS...)

PCC app (LV RT) – FECOS component

- handles configuration and sequence files
- passes set-points and command requests to device drivers
- sends received data (responses, measurements) up to FECOS



hard drive

PCC driver (specific for PCO type)

- converts universal commands into appropriate format (depending on the PCO type)
- converts command responses back to the universal format

PCC – FPGA logic

PCC app – LV FPGA part

- prepares data for the VHDL logic (sequences into RAM, parameters through "memory interface")

FlexRIO RAM

PCC app – VHDL FPGA part

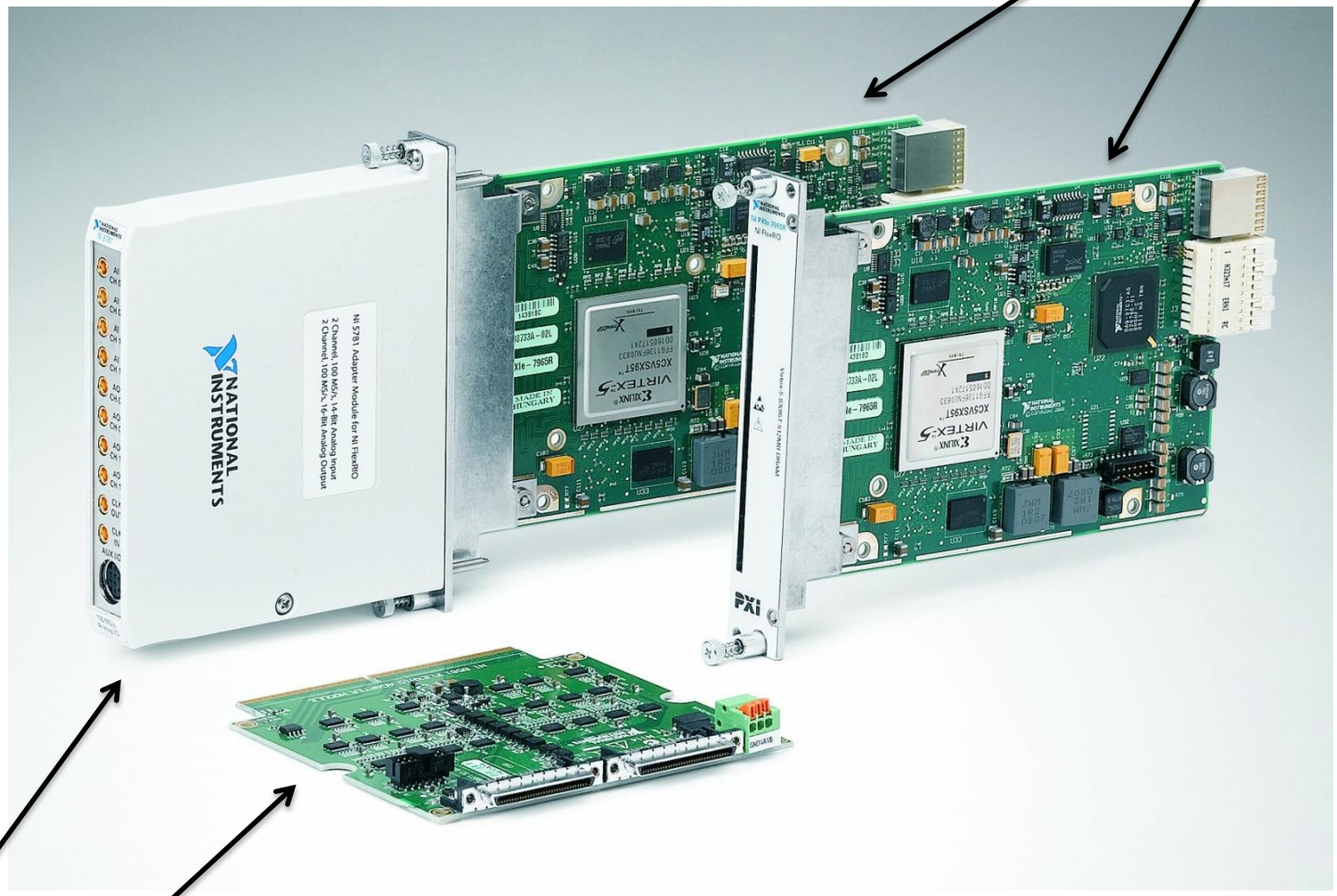
- generates single set-points, sequences (waits for events, adds delay, generates with frequency...) and transmits commands over the fiber optic link
- receives commands responses and measurement results

MTR

Interlock

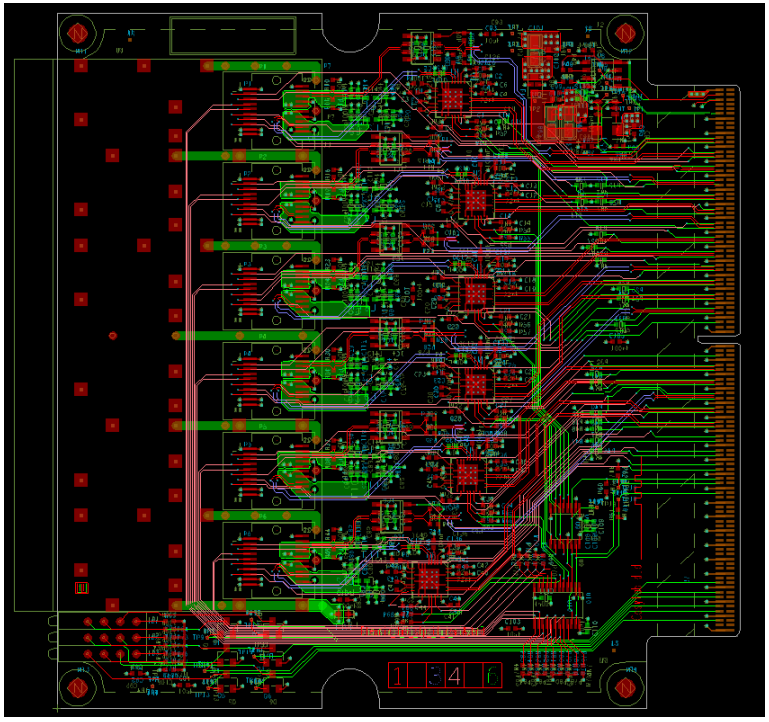
optical SFP

Flex..... what?


FlexRIO FPGA Modules
FlexRIO Adapter Modules
NATIONAL INSTRUMENTS
NI 5781 Adapter Module for NI FlexRIO
2 Channel, 100 MS/s, 14-Bit Analog Input
2 Channel, 100 MS/s, 16-Bit Analog Output
PXI

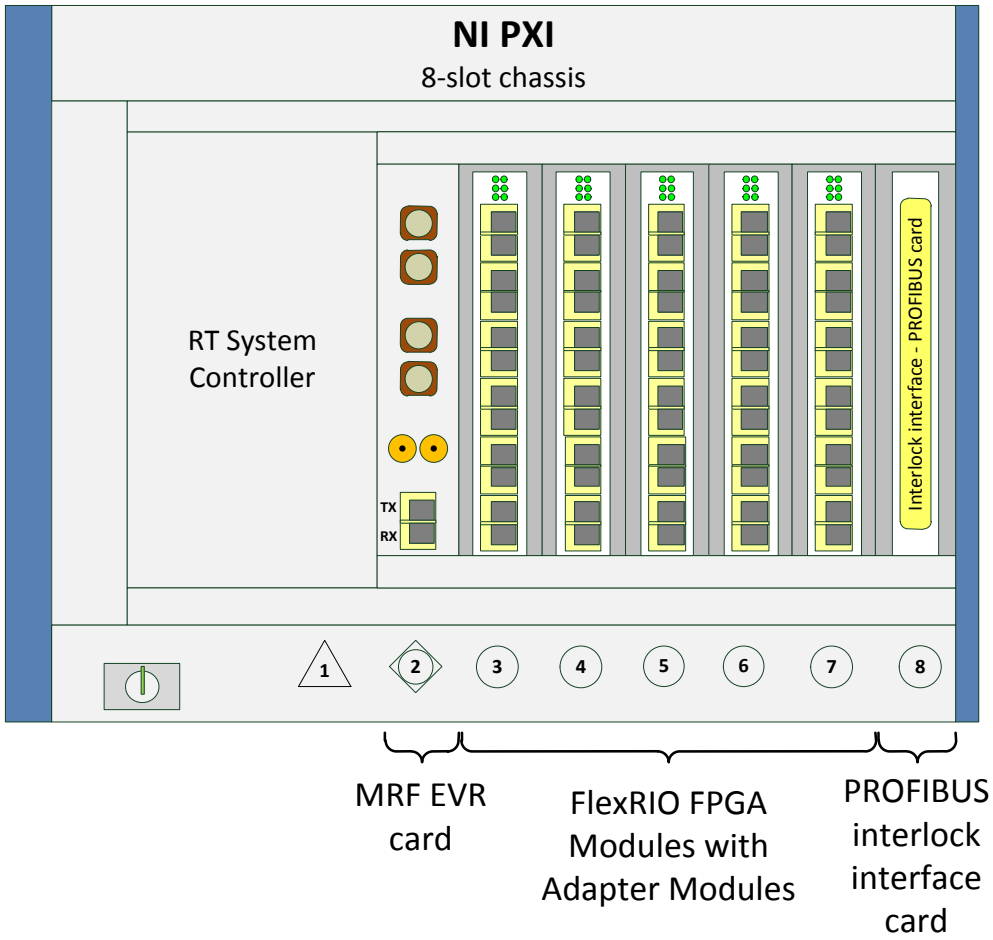
Our FlexRIO Adapter Module

- 6 optical connectors
- utilizing standard FPGA Input/Output pins
  - full control over these pins
- prototypes in production



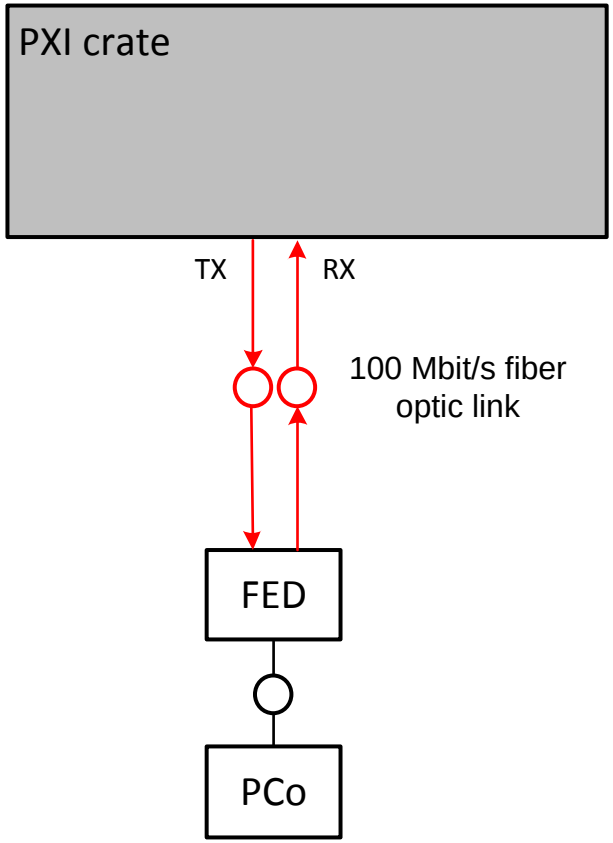
PXI crates

- total of 10 crates in the system
- up to 5 FlexRIO FPGA Modules per crate
- MTS EVR card
- interlock card



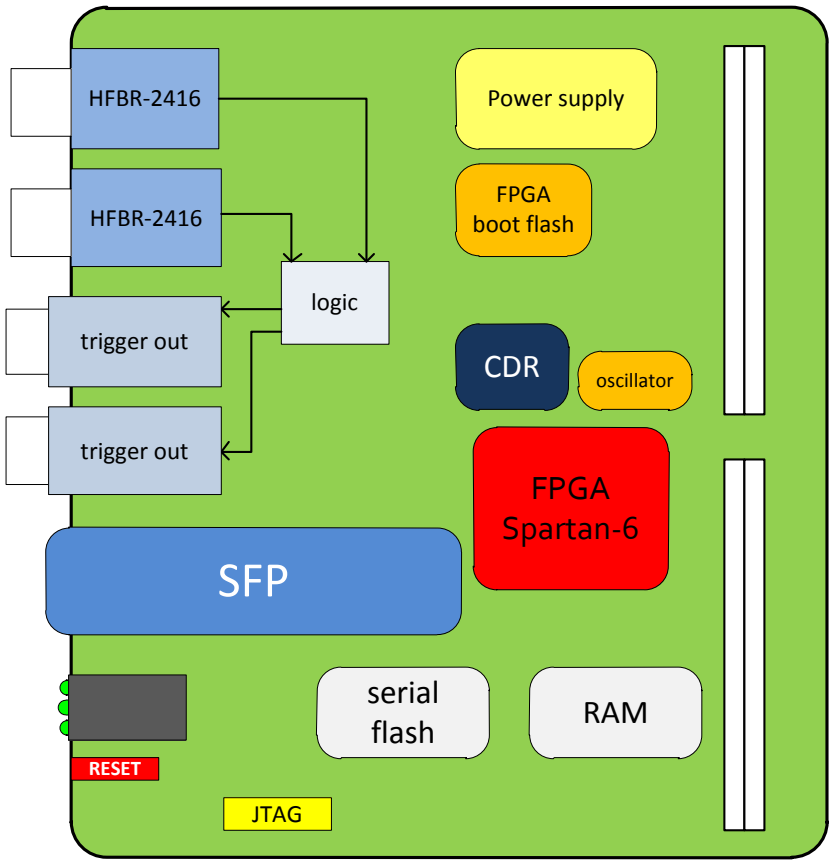
Serial link

- custom developed protocol
- 100 Mbit/s transfer rate
- high-priority data
  - low latency, **deterministic delay**
  - downstream: set-points
  - upstream: measurement results
- low-priority data
  - non-deterministic delay
  - downstream: commands
  - upstream: command responses



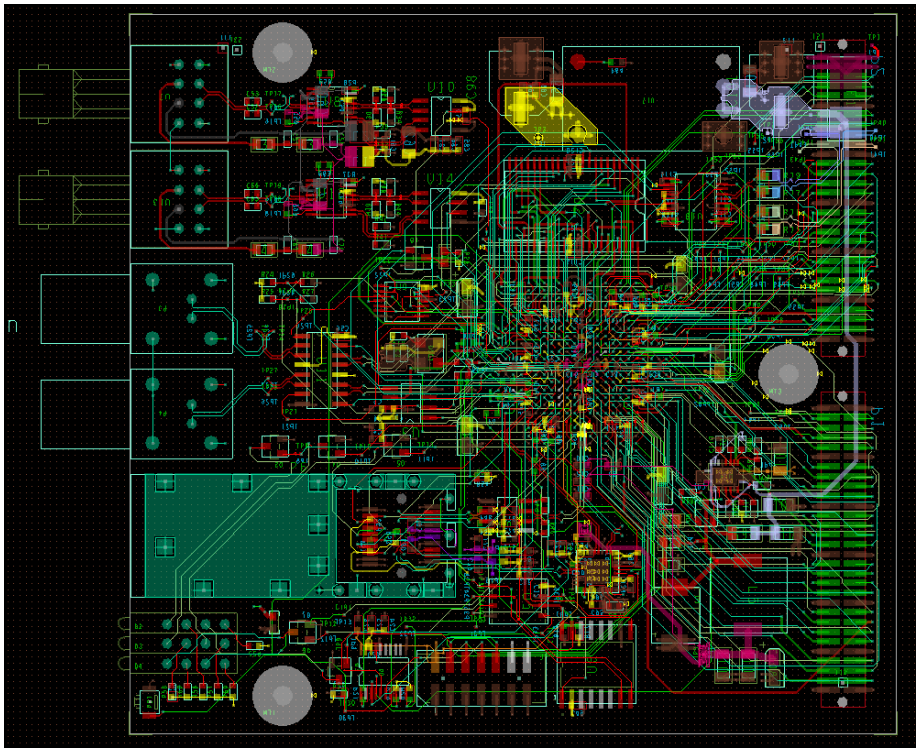
Front End Device (FED)

- based on Spartan-6 FPGA
- fiber interface towards the PCC
- trigger in/out
- expansion connectors
  - 32-bit UHPI
  - parallel interface
  - serial interface
  - interlock
  - GPIOs
  - control/status signals...
- has to be connected to a baseboard



FED – continued

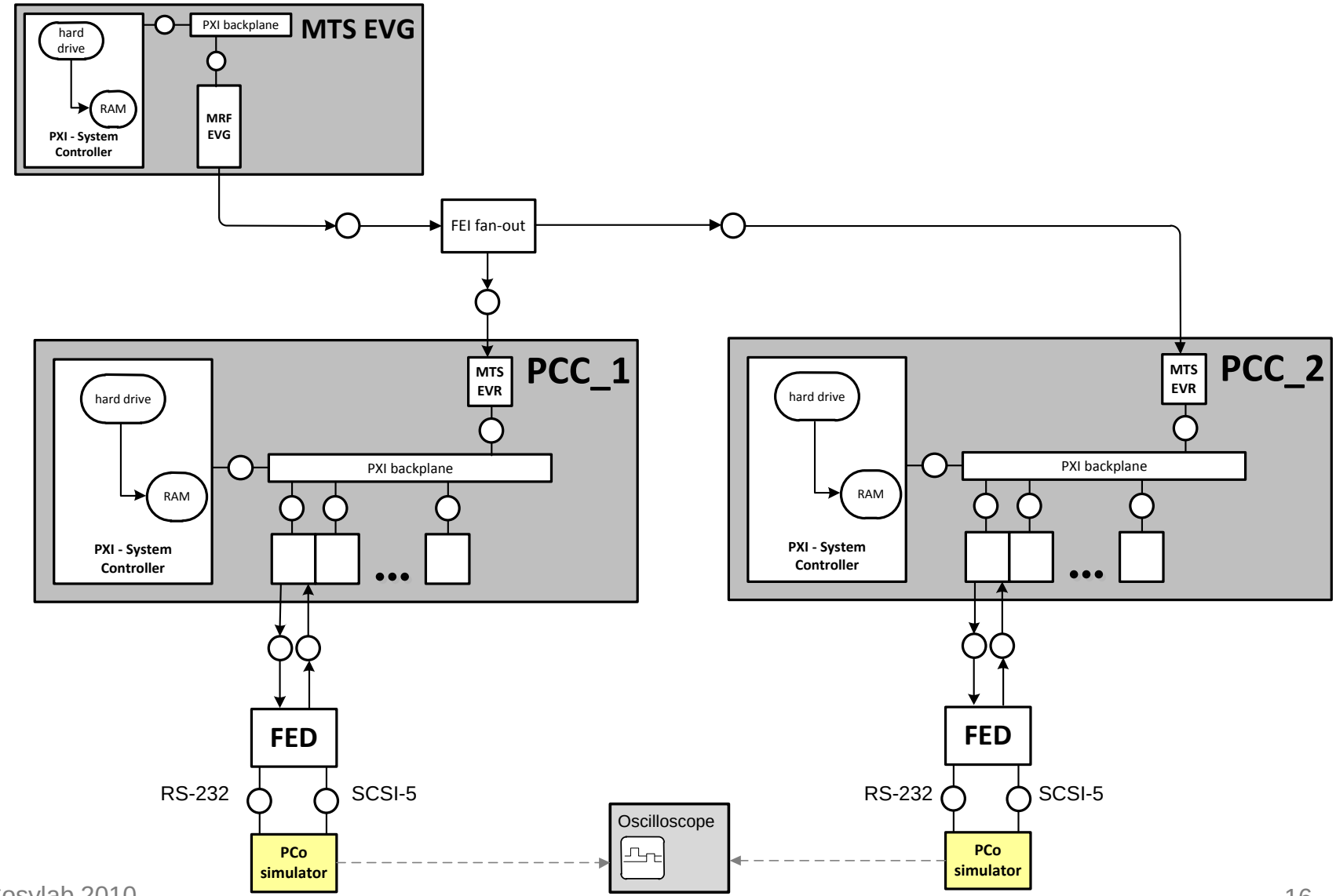
- first protoypes are currently being manufactured



Can you spot the FED inside the owen?

Demo

- sorry, no demo for today... available in December



CWO-3

- PCC – implement the remaining features
  - full featured sequences
  - full features measurements
  - complete command set for all PCO types
  - sequence (de)compression
  - driver support for CRB
  - pulse synchronization
  - GUIs
  - ...
- FED – implement the remaining features
  - CRB interface
  - set-point correction
  - FPGA bitstream update, multiboot
  - FED status and configuration (interlock)
  - ...

That’s all