

Computing System Trends and Performance Portability

Bálint Joó – OLCF, Oak Ridge National Laboratory

Lattice 2021 Virtual Meeting (MIT)

July 30, 2021

Contents

- Machine Trends
- Node Programming Models
- Porting Stories

Introduction – a brief history

- I recall at Lattice 2006 in Tuscon, first hearing about the idea of LQCD calculations on GPUs in a talk by Daniel Nogradi.
 - Programming was done using OpenGL.
 - I thought: “This looks fun, but it will never catch on!”
- I had to eat my words as I gave a talk about GPU accelerated computing in Squaw Valley at Lattice 2011 – 10 years ago.
- 2012-2018 was an era of ‘friendly competition’ between NVIDIA GPUs and Intel Knights
 - The Knights fought well, but were discontinued
 - Remaining fighting Knights are getting close to retirement
- OLCF Summit exceeded 1.88 ExaOps (in 32 and 16-bit precisions) on a Genomics Machine Learning Application in 2018, kicking off the Exascale era

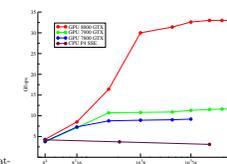
Lattice QCD as a video game

Gyöző L. Egri^a, Zoltán Fodor^{abc}, Christian Hoelbling^b,
Sándor D. Katz^{ab}, Dániel Nögrádi^b and Kálmán K. Szabó^b

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^cDepartment of Physics, University of California, San Diego, USA

Abstract

The speed, bandwidth and cost characteristics of today's PC graphics cards make them an at-



[Egri et. al. "Lattice QCD as a video game" Comput. Phys. Commun. 177:631-639,2007 arXiv:hep-lat/0611022](#)



JLab 9g cluster (2009)



JLab 10g cluster (2010)



OLCF Titan (2012)



JLab 12k/m cluster (2012)



NERSC Cori KNL (2016)



JLab 16p and 18p KNL Cluster (2016-...)

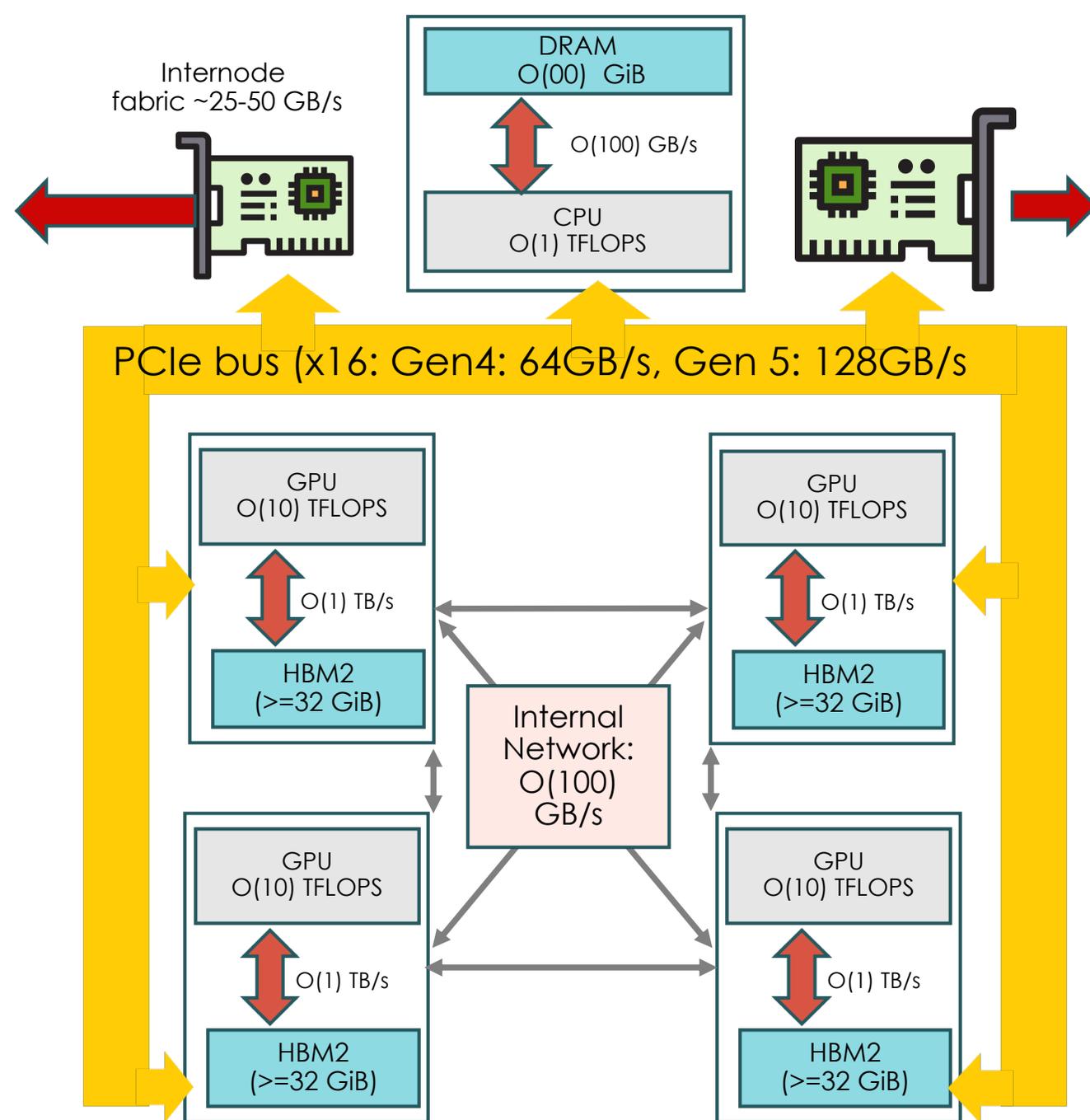


OLCF Summit 2017

Hardware

Typical Pre-Exascale Node

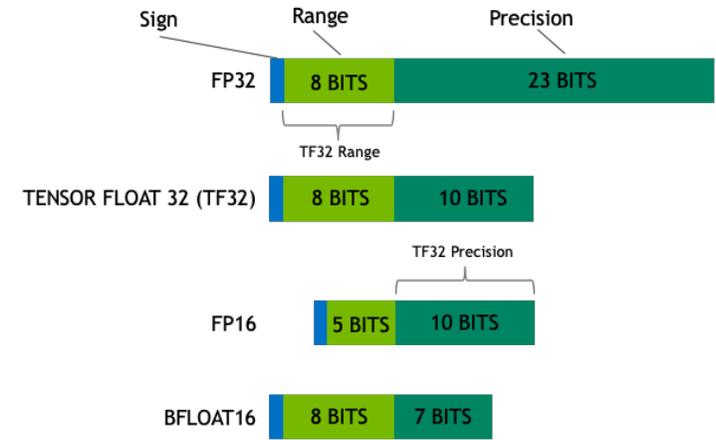
- Schematically not much has changed from Summit
 - Internal network
 - NVLink; 50GB/s per link, A100: up to 12 links=>600 GB/s
 - Infinity Fabric: 92 GB/s link, MI100: up 3 links=> 276 GB/sec
 - External Network
 - Cray/HPE Slingshot (Slingshot **10**: 12.5 + 12.5 = 25 GB/s)
 - Infiniband: (NDR: 50 GB/sec)
 - GPU compute ~ ~10x CPU compute
 - GPU mem-bandwidth ~10x CPU bandwidth
- GPUs have fast low precision matrix-matrix multiply capability
 - NVIDIA Tensor Cores (V100, A100)
 - AMD CDNA (MI100)
- In these accelerated nodes GPUs provide majority of performance
 - I will **blissfully ignore CPU details from here on in**
- Most (not all) LQCD stencils are memory bandwidth bound
 - 1EFLOPS peak => 100 PB/sec peak bandwidth
 - F/B ratio ~0.5-1 for Wilson like fermions in 64 Bit



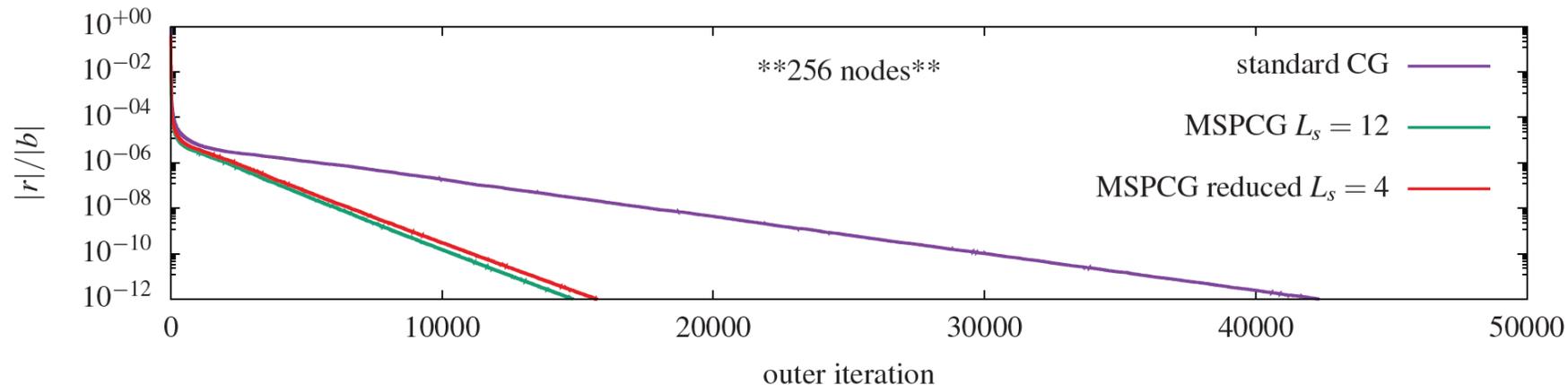
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QUDA and tensor core

- Speed up compute intensive kernels in QUDA with tensor cores that accelerate MMA operations on NVIDIA GPUs [poster D9]
 - [WIP] Multi-BLAS
 - m5inv in MSPCG/additive Schwarz: **1.5x** time-to-solution speed up [arXiv:2104.05615, J. Tu's parallel 07/28 14:30]
 - Multi-grid setup: as high as **13x** speed up for `computeUV` on Volta
- [WIP] MMA support for all four precisions: double (fp64), single (fp32), half (16-bit fixed-point), quarter (8-bit fixed-point)
 - $(hi + lo) * (hi + lo) = hi * hi + hi * lo + lo * hi + lo * lo$
 - Use 3xTFLOAT32 for single, and 3xBFLOAT16 for half



Stage	V100 TFLOPS	V100 speed up	A100 TFLOPS	A100 speed up
UV	22.7	13.0	48.4	12.1
$V^T UV$	6.5	1.5	11.4	2.0
$X^{-1} Y$	42.0	9.2	70.6	11.6

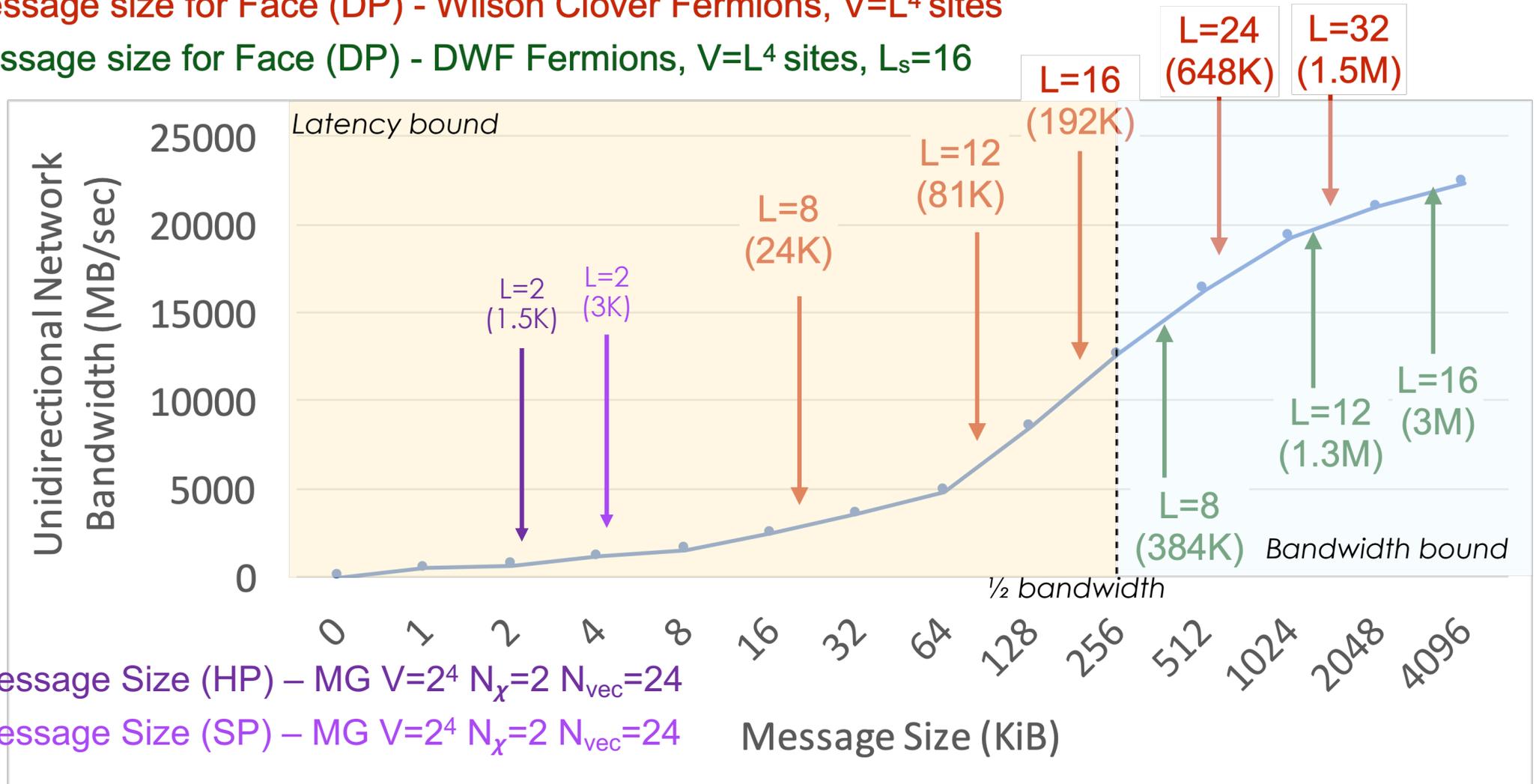


- ← 577.6 seconds
- ← 458.3 seconds
- ← 381.5 seconds

Latency Or Bandwidth? Both Please...

→ Message size for Face (DP) - Wilson Clover Fermions, $V=L^4$ sites

→ Message size for Face (DP) - DWF Fermions, $V=L^4$ sites, $L_s=16$



→ Message Size (HP) – MG $V=2^4$ $N_x=2$ $N_{vec}=24$

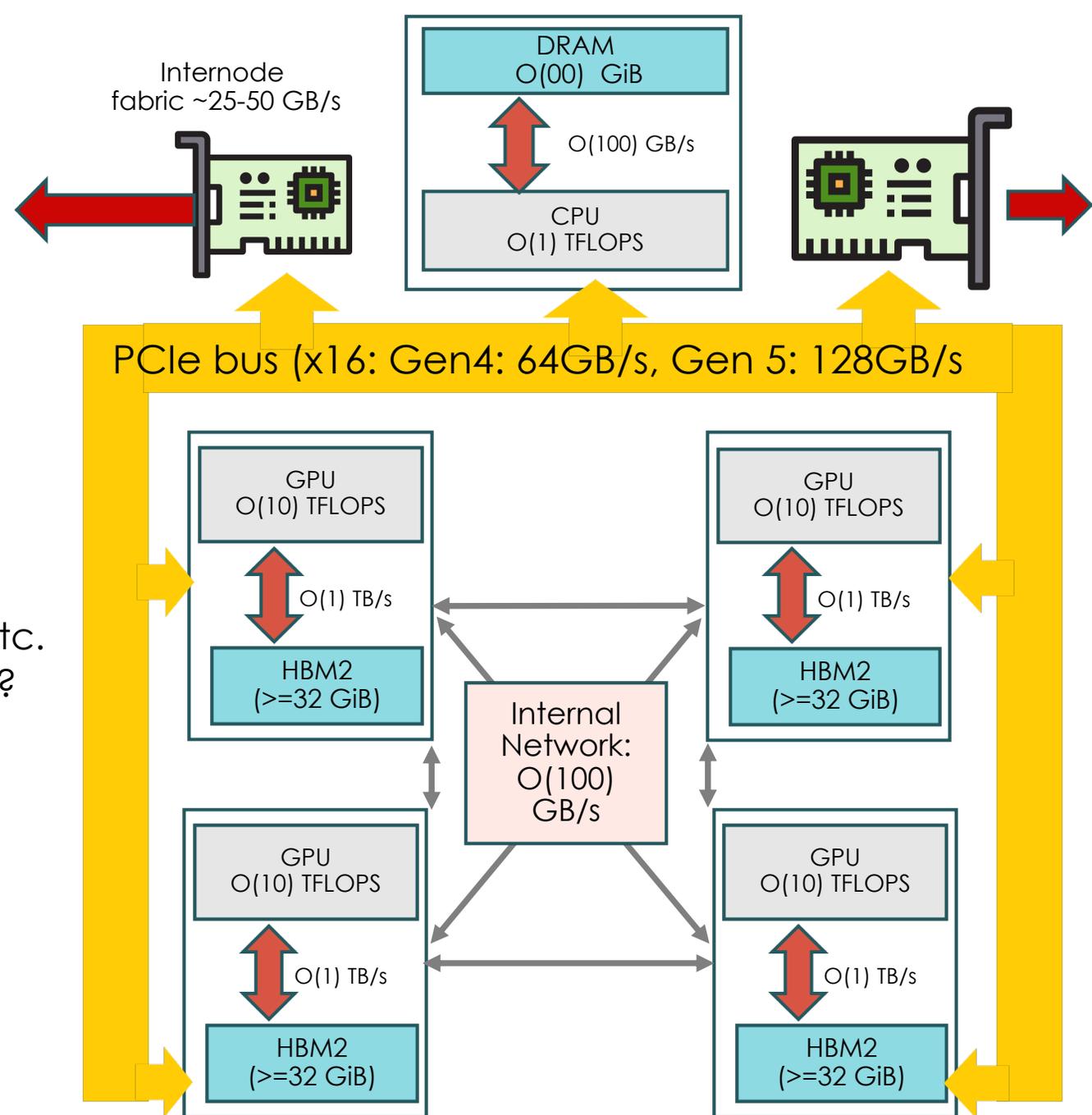
→ Message Size (SP) – MG $V=2^4$ $N_x=2$ $N_{vec}=24$

Message Size (KiB)

Data for Summit from SummitWorkshop-SummitNodePerformane-WJ talk by W. Joubert

And so, nuances matter

- Hardware capability
 - Direct path from GPUs to NIC?
 - Can GPUs initiate communications?
 - Number of hops in internode networks
 - Amount of GPU memory & H2D2H transfers
 - Unified/Managed Memory Capability?
- Programming model & implementation
 - Kernel launch latency
 - GPU aware MPI, Interfaces for P2P, SHMEM etc.
 - Persistent kernels, synchronizing with atomics?
 - Access to Unified/Managed Memories
- Algorithmic Pushes
 - MG & Reduced precision -> latency
 - Multi-RHS/Split Grid algorithms -> B/W
 - DD algorithms -> device locality



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Latencies affect strong scaling

QUDA NVSHMEM WILSON-DSLASH SCALING

Global Volume $64^3 \times 128$, NVIDIA Selene

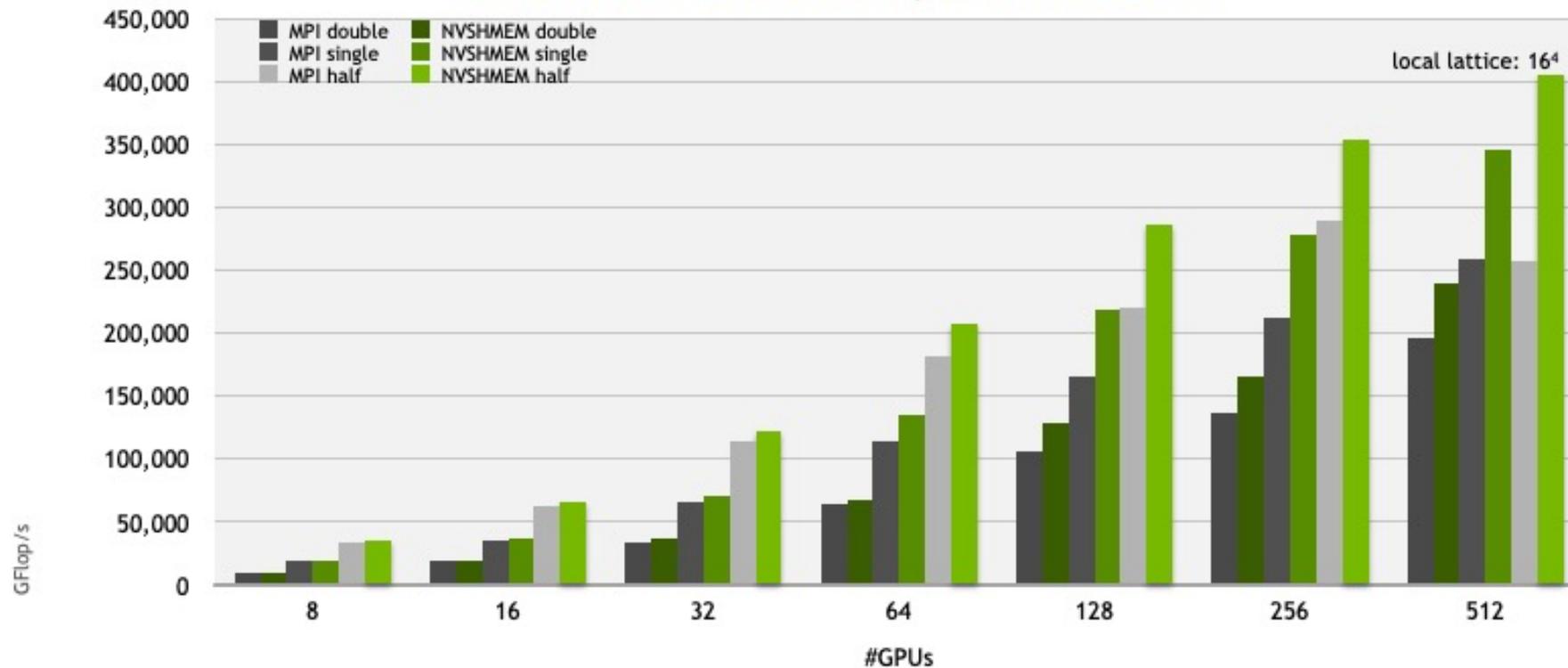
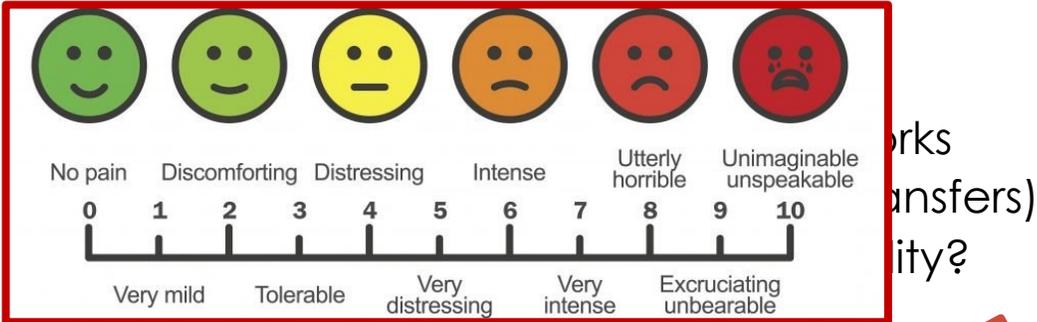


Figure Courtesy of M. Wagner, NVIDIA (Talk on Wednesday afternoon in Machines and Software session in this conference)



And so, Nuances matter

- Hardware capability

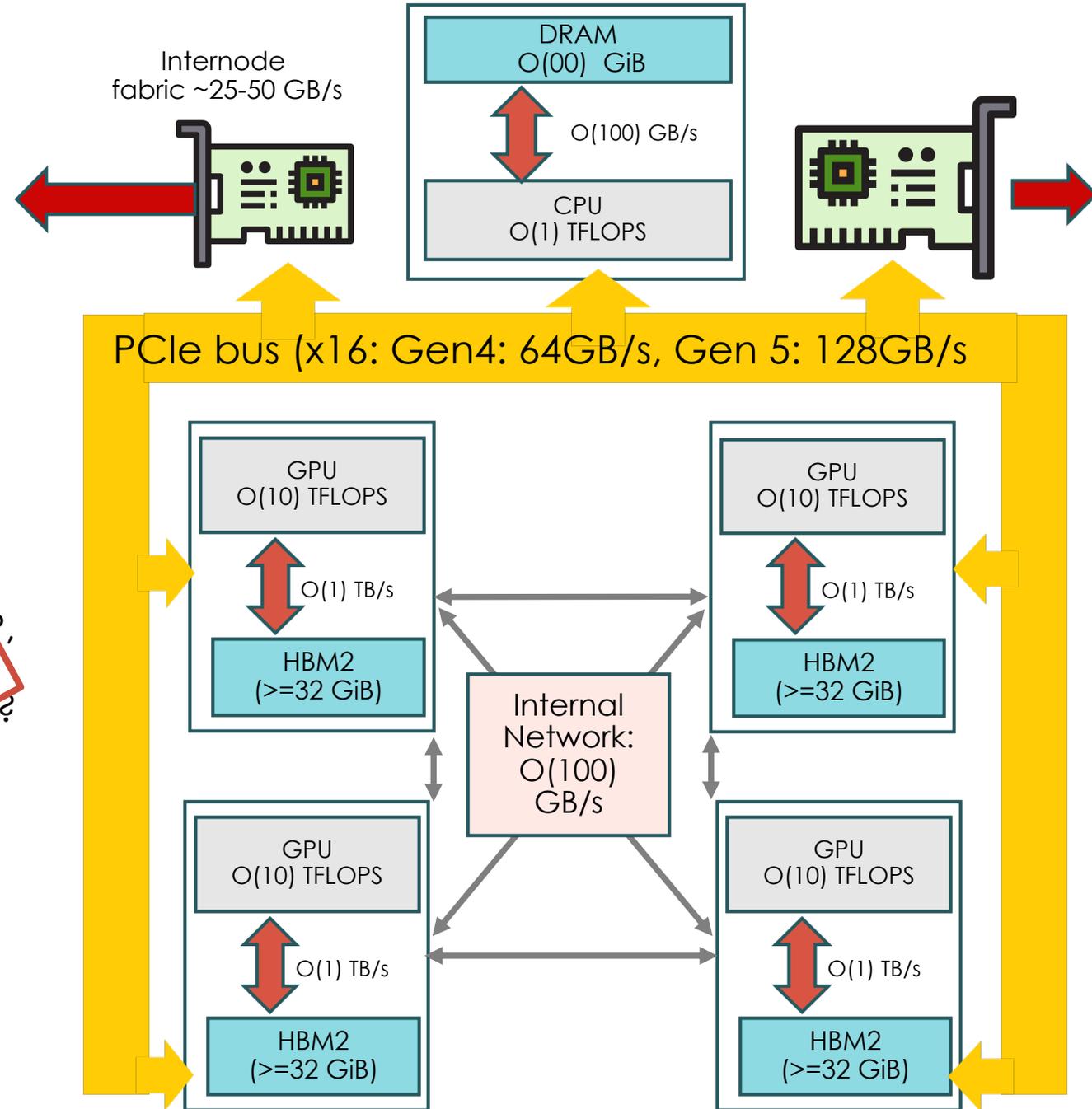


- Programming model & implementation

- Kernel launch latency
- User access to Hardware (e.g. SHMEM etc)
- Persistent kernels, state
- Access to Unified memory

- Algorithmic
- Memory access patterns -> latency
- Algorithmic complexity -> B/W
- Data access patterns -> device locality

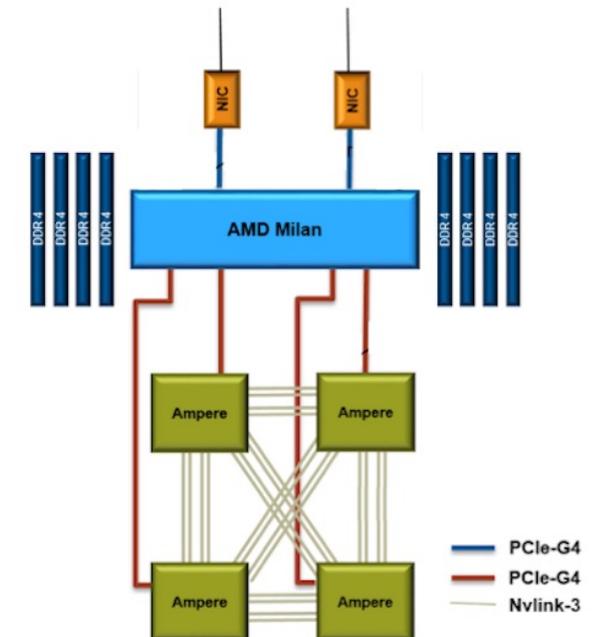
YOUR LEVEL OF PAIN MAY VARY !!!



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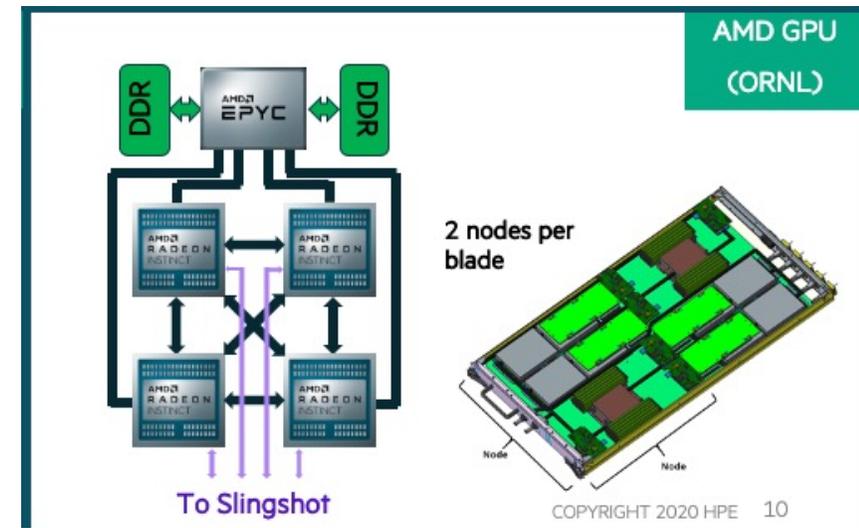
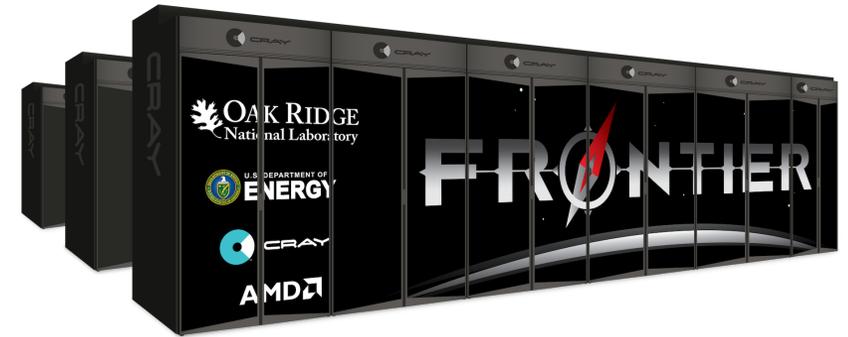
US Exascale and Pre-Exascale Systems: NERSC Perlmutter

- Perlmutter is the New HPE/Cray “Shasta” system recently arrived at NERSC
 - #5 on Top 500 List: 89.8 PF (Rpeak), 64.5 PF (Rmax)
- Accelerators are NVIDIA A100 (Ampere) GPUs
 - Memory B/w: 1555.2 GB/sec
 - FLOPs:
 - 19.5 TF (FP32) 9.7 TF (FP64)
 - Tensor ops: 311.9 (FP16), 155.9 (TF32), 19.5 (FP64)
- NVLink 3
 - 4 GPUs on node have all-to-all connection
 - 100 GB/s/direction between a pair of GPUs
 - 600 GB/sec total into/out-of a GPU
- HPE/Cray Slingshot-10 Interconnect
- System is expected to open to users soon
- Programming Models
 - MPI + CUDA, OpenMP-5 offload, NVSHMEM
- <https://www.nersc.gov/systems/perlmutter/>



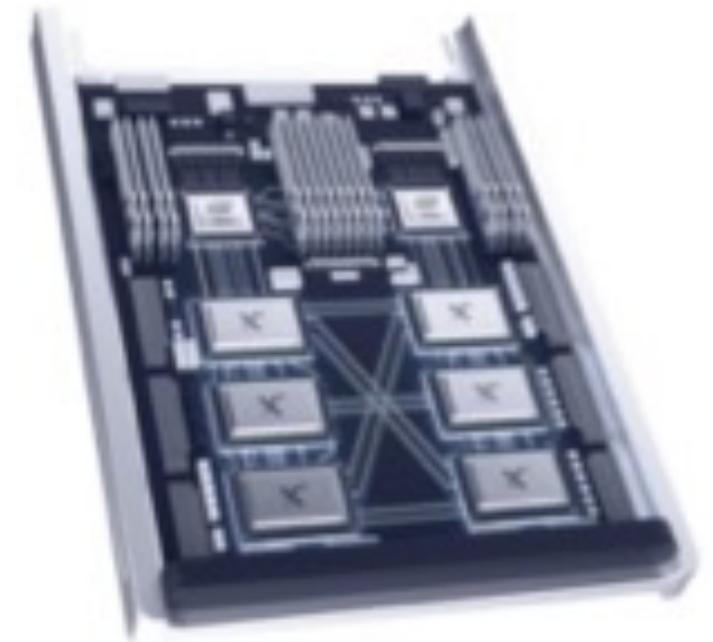
US Exascale and Pre-Exascale Systems: OLCF Frontier

- Frontier will be the New HPE/Cray “Shasta” system at Oak Ridge Leadership Computing Facility
 - >1.5 Exaflops peak performance
- Accelerators will be AMD Radeon Instinct GPUs
- AMD Infinity Fabric
 - 4 GPUs on node to have all-to-all connection
- HPE/Cray Slingshot
 - “Multiple Slingshot NICs providing 100GB/sec network bandwidth”
 - GPUs will have direct connection to Slingshot
- Programming Models
 - MPI, AMD HIP, OpenMP-5-offload, ...
- <https://www.olcf.ornl.gov/frontier>



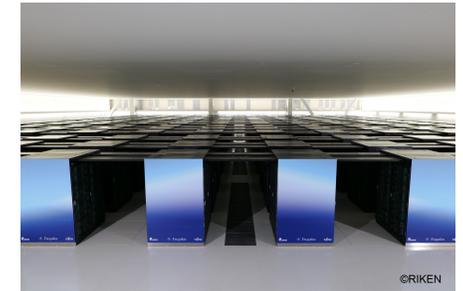
US Exascale and Pre-Exascale Systems: ALCF Aurora

- Aurora will be the New HPE/Cray “Shasta” system at Argonne Leadership Computing Facility
 - >1 Exaflop peak (DP) performance
- Accelerators will be Intel Xe architecture based “Ponte Vecchio” GPUs
- Unified Memory Architecture
 - Across GPU and CPU
- Low Latency, High Bandwidth all-to-all connectivity within Node
- HPE/Cray Slingshot interconnect
 - 8 fabric endpoints per node
- Programming Models
 - MPI, Intel oneAPI DPC++ (based on SYCL), OpenMP-5-offload, ...
- <https://alcf.anl.gov/aurora>



Other Noteworthy Systems for LQCD

- Supercomputer Fugaku, RIKEN CCS Japan
 - #1 Top 500 list: 537PF (Rpeak), 442 PF (Rmax)
 - Please see talk by Yoshifumi Nakamura!
- Summit at OLCF, U.S.A
 - #2 Top 500 list: 200PF (Rpeak), 148.6 PF (RMax)
- Sunway TaihuLight, National Supercomputing Center, Wuxi, China
 - #4 on on Top 500 list: 125.4 PF(Rpeak) 93PF(Rmax)
- Tianhe-2A, National Super Computer Center, Guangzhou, China
 - #7 on the Top 500 list; 100.6 PF (Rpeak) 61PF (Rmax)
- JUWELS Booster, Forschungszentrum Jülich, Germany
 - #8 on Top500 List: 71PF (Rpeak), 44 PF (Rmax)
 - 4 NVIDIA A100 GPUs, switched directly to HCAs
 - Infiniband Network in DragonFly+ configuration.



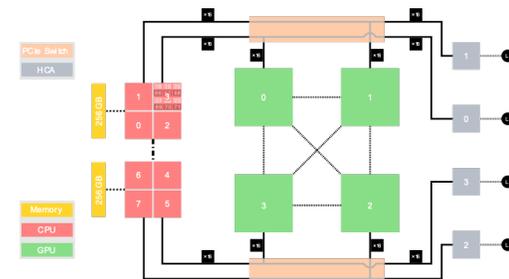
Supercomputer Fugaku



OLCF Summit



TaihuLight



JUWELS Booster Node Architecture

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Custom QCD Systems?

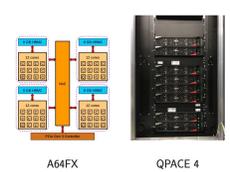
- QPACE 4: 177/354 TFlop/s peak
 - Please see poster by the Regensburg group: N. Meyer, P. Georg, S. Solbrig & T. Wettig
- A64FX CPUs - Fugaku like
 - 48 cores/CPU 1.8 GHz
 - 512-bit Arm SVE SIMD: 2.76 TF/cpu
 - 32 GB HBM2 memory per CPU
- InfiniBand EDR interconnect
- Open-source software stack
 - no assistant cores like Fugaku
 - lots of kernel tuning to reduce O/S noise.

Grid on QPACE 4
 Nils Meyer, Peter Georg, Stefan Solbrig, Tilo Wettig
 Department of Physics, University of Regensburg, Germany



QPACE 4

- ▶ Latest member of QCD Parallel Compute Engine (QPACE) series
 - ▷ Fujitsu PRIMEHPC FX700 series
 - ▷ Deployed June 2020 at Regensburg University
- ▶ 64 Fujitsu A64FX CPUs (48 cores each, 1.8 GHz)
 - ▷ 512-bit Arm Scalable Vector Extension (SVE)
 - ▷ 177/354 TFlop/s peak in double/single precision (DP/SP)
 - ▷ 2048 GB HBM2 memory total
 - ▷ InfiniBand EDR interconnect (100 Gbit/s)
- ▶ Open-source software stack
 - ▷ CentOS Stream 8, GCC 10.1, OpenMPI 4.0
 - ▷ GlusterFS parallel filesystem
 - ▷ Grid Lattice QCD framework [1]
 - ▷ Grid Python Toolkit (GPT) [2]



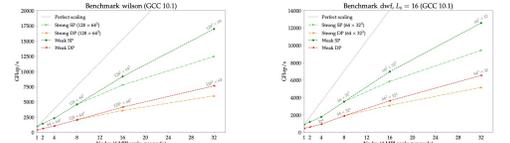
Wilson Dslash and Domain Wall kernels

▶ Performance-relevant part of Domain Wall Dirac operator, same source code as Wilson Dslash ($L_5 = 1$)

$$\psi'(n, s)_{\text{DW}} = (D\psi)'(n, s)_{\text{DW}} = \sum_{\mu=1}^4 \sum_{\nu=1}^4 \sum_{\rho=1}^4 \{ U'_{\nu}(n)_{\mu}(1 + \gamma_{\nu})_{\mu\nu} \psi(n + \hat{\mu}, s)_{\rho} + U'_{\nu}(n - \hat{\mu})_{\mu}(1 - \gamma_{\nu})_{\mu\nu} \psi(n - \hat{\mu}, s)_{\rho} \}$$

▶ Specialization for A64FX (---dslash-asm): manual instruction scheduling and software prefetching using ACLE

▶ GCC 10.1 and 10.2 achieve best performance, outperforming other compilers (incl. clang/LLVM 12.0 and GCC 11.1)



Stream benchmark

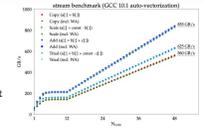
▶ Standard benchmark for memory throughput evaluation

▶ $N_{\text{max}} > 12$: data throughput scales with number of cores in use

▶ Benchmark data throughput: up to 625 GB/s

▶ Caches implement write-back policy

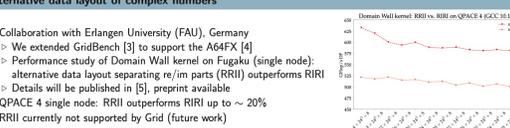
- ▷ Write Allocation (WA): cache block load from memory on write miss
- ▷ WA causes extra traffic and thus reduces effective memory throughput
- ▷ Including WA traffic, data throughput is up to 835 GB/s



Alternative data layout of complex numbers

▶ Collaboration with Erlangen University (FAU), Germany

- ▷ We extended GridBench [3] to support the A64FX [4]
- ▷ Performance study of Domain Wall kernel on Fugaku (single node): alternative data layout separating re/im parts (RRII) outperforms RIRI
- ▷ Details will be published in [5], preprint available
- ▶ QPACE 4 single node: RRII outperforms RIRI up to ~20%
- ▶ RRII currently not supported by Grid (future work)



Grid port to A64FX (512-bit SVE)

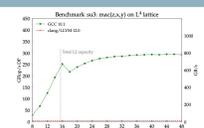
- ▶ Arm C Language Extensions (ACLE) provide access to SVE vector types and SVE instructions in C/C++
- ▶ We use ACLE to implement Grid's lower-level functions
 - ▷ Alternating re/im parts layout (RRII)
 - ▷ Hardware support for processing complex numbers
- ▶ Hand-optimized Wilson Dslash and Domain Wall kernels using ACLE and RRII layout
- ▶ Available in upstream Grid develop branch (`configure --enable=simd=A64FX`)

Grid benchmark: SU(3) matrix multiplication

▶ Independent SU(3) matrix multiplication $z = x \times y$ on each lattice site

▶ Well suited for compiler testing

- ▷ GCC 10.1: up to ~300 GFlop/s DP (800 GB/s)
- ▷ GCC 10.2 and 11.1: achieve same performance
- ▷ clang/LLVM compilers underperform (incl. clang/LLVM 12.0)



Summary and outlook

- ▶ Fujitsu A64FX achieves outstanding performance for Lattice QCD applications
- ▶ GCC 10.1 and 10.2 achieve best overall performance
- ▶ Other compilers underperform (incl. clang/LLVM 12.0 and GCC 11.1)
- ▶ Alternative layout of complex numbers is beneficial on A64FX, but yet to be integrated into Grid (future work)

References

[1] P. Boyle et al., Proceedings of LATTICE 15 (2016) 023 [arXiv:1512.03487]
 [2] C. Leheer et al., "Grid Python Toolkit (GPT)", <https://github.com/leheer/gpt>
 [3] P. Boyle et al., "GridBench - Single CPU benchmarks cutting down Grid", <https://github.com/paboyle/GridBench>
 [4] N. Meyer et al., "GridBench - AVX512 and A64FX extensions", <https://github.com/meyer-ur/gridbench-17-avx512-17-a64fx>
 [5] C. Alappatt et al., Concurrence and Computation: Practice and Experience (PAMIS special edition) (2021) [arXiv:2103.03013]

Supported by the German Research Foundation (DFG) in the framework of SFB/TRR-55

Software

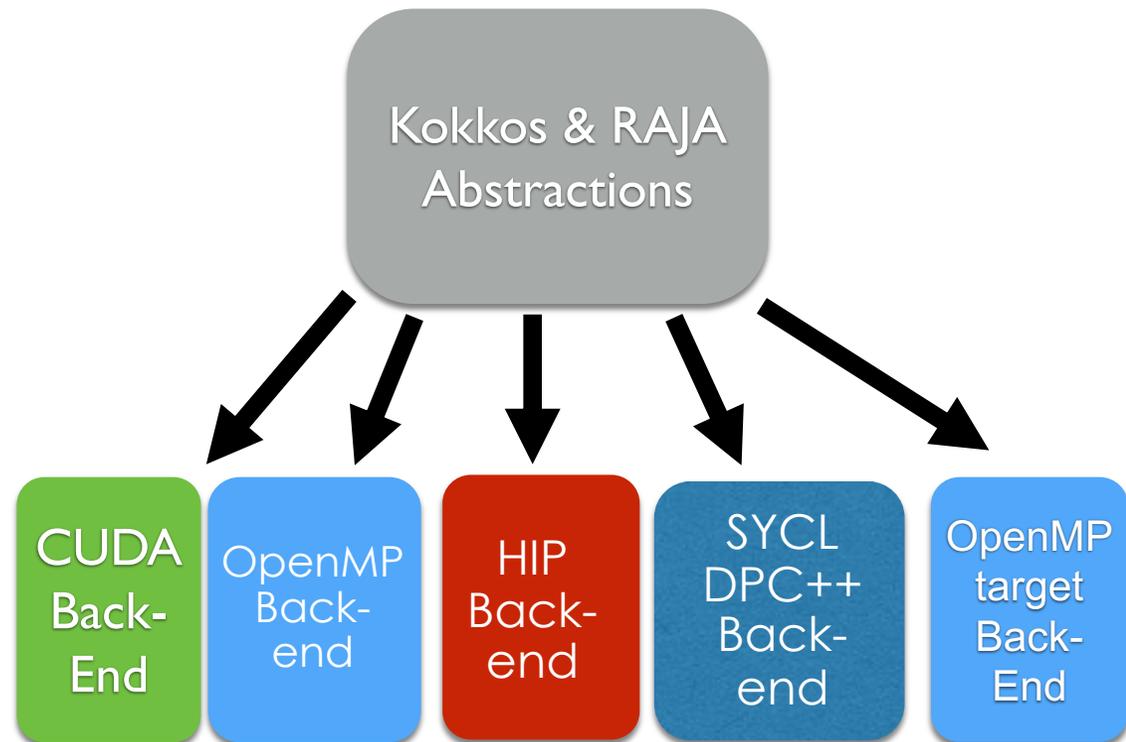
Node Programming Models: Pick your standard

- Vendor options
 - NVIDIA CUDA: the CUDA you know, evolved..
 - Support for Tensor cores in cuBLAS, cuDNN and CUDA (wmma:: namespace)
 - ecosystem support: cuBLAS, cuFFT, cuRAND etc.
 - C++ Standard Library (cuda::std::)
 - Strong push to implement **ISO C++ standard** features in full.
 - **AMD HIP**
 - very similar to NVIDIA's CUDA core library (replace 'cuda' with 'hip')
 - **open source implementations for ROCm, also for CPUs** (HIP CPU)'
 - LLVM/Clang based compiler
 - ecosystem support: hipBLAS, hipFFT/rocFFT, hipRAND/rocRAND, etc
 - access to CDNA features through compiler
 - Intel oneAPI
 - based on **SYCL Standard from the Khronos Group, with OpenCL heritage**
 - Compiler in oneAPI SDK and in Intel's contributions to LLVM
 - ecosystem support: oneMKL, oneDNN, ...
 - oneAPI Tutorial at this conference by P. Steinbrecher
- Directive based approaches: **OpenMP-offload and OpenACC**
 - OpenMP: `#pragma omp teams distribute parallel for simd`
 - all vendors committed to supporting OpenMP-5.0 offload
 - OpenACC supported in NVIDIA HPC-SDK and GCC (work by Mentor Graphics)
 - OpenMP is likely the best option for Fortran (although nvfortran can offload DO CONCURRENT)
- **OpenCL** is available through all vendors as well
 - but beware vendor specificity in the implementations...



Performance Portability via Kokkos and RAJA

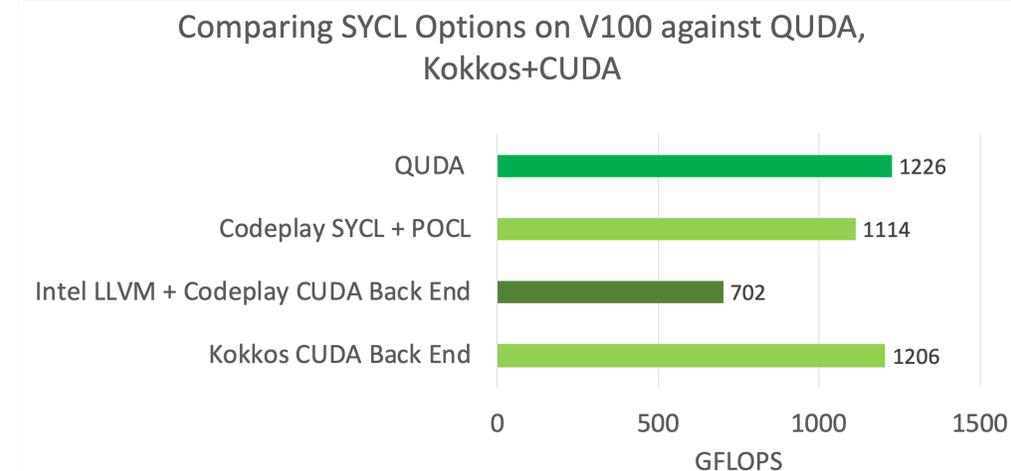
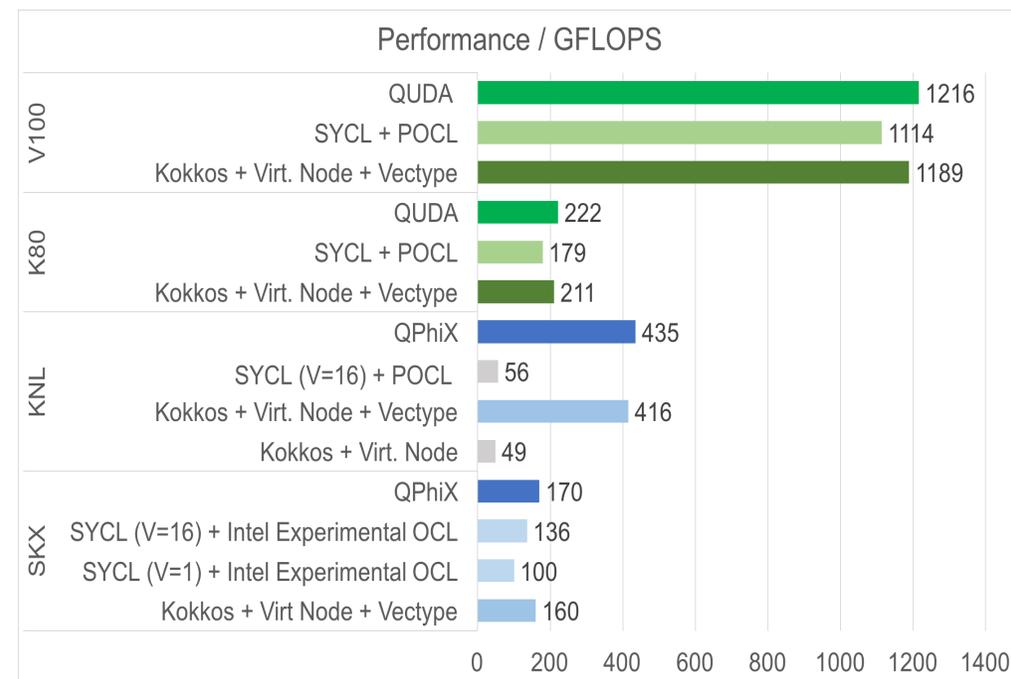
- Kokkos and RAJA provide portability to C++ programs via 'back ends'
 - Kokkos now has a Fortran interface project
- Both prog. models provide basic parallel patterns
 - forall, reduction, scan
- Kokkos provides 'View' datatype
 - multi-dimensional array, a precursor to `std::mdspan`
 - RAJA uses other packages (e.g. Umpire) for memory management
- Views and execution patterns are bound to memory and execution spaces via policies.
 - Policies have default values, which can be set in some architecture specific header.



```
Kokkos::View<float[1000]> y("y"), x("x");  
// Fill x and y somehow – not shown  
  
float alpha=0.5;  
Kokkos::parallel_for(1000,  
                    KOKKOS_LAMBDA(int i) {  
                        y(i) += alpha * x(i);  
                    });
```

Portability of the programming Models

- Directive based approaches: should target all main systems
 - require strong compiler support, and vendors to agree on interpretation of the standard
- Intel Data Parallel C++: main target: Intel GPUs/CPUs/FPGAs etc.
 - Aurora Proxies: Linux laptops with Intel Graphics (Gen 9 or later), Intel Dev Cloud, JLSE Early access systems
 - NVIDIA GPUs: Intel LLVM compiler has CUDA back end from Codeplay
 - AMD GPU: hipSYCL Project, a pilot AMD Back End for Intel LLVM is being developed by Codeplay
- HIP: main target AMD GPUs
 - Frontier Proxies: NVIDIA GPUs systems (Summit), Early Access Systems (Spock)
 - NVIDIA GPUs: Native support up to a certain CUDA level (substitutions: 'hip'→'cuda')
 - Intel GPUs: ECP HIP-LZ (HIP on Level Zero) project
 - nascent HIP-CPU project to support CPUs (as a development aid)
- CUDA: main target NVIDIA GPUs
 - Perlmutter Proxies: Summit, JUWELS-Booster, Desktop GPU systems,
 - AMD: HIP includes 'hipify' conversion tool for 'developer assisted' conversion to HIP.
 - Intel GPUs: Intel provides 'developer assisted' conversion to Data Parallel C++
- Kokkos & RAJA: pick most performant back end (most likely the native one)



figures from B. Joo P3HPC Forum 2020 virtual meeting. Courtesy of B. Joo and collaborators.

Code porting/development efforts: QUDA

- QUDA is a software library for QCD components
 - Advanced Optimized solvers (e.g. Aggregation based MG preconditioner)
 - Key optimized routines: GaugeForce (MILC), Gauge Fixing,
 - Multiple precision use since Day-1
 - Built in Autotuning
 - adjusting grid, block and shared memory sizes,
 - choosing communications policy e.g. P2P, GDR, MPI
- See "Towards QUDA 2.0" talk by K. Clark (Wed, 1pm) for refactoring details
 - plus several other QUDA related talks at this conference (M. Wagner, E. Weinberg, J. Tu, ...)
- QUDA grew a 'performance portability' subgroup of developers:
 - K. Clark (NVIDIA) QUDA Lead developer, C++, std::par, pSTL, NVC++
 - B. Joo (OLCF) HIP Backend
 - D. Howarth (LLNL) HIP Backend
 - J. Osborn (ALCF) DPC++ Backend
 - X-Y. Jin (ALCF) OpenMP-offload Backend
 - A. Strelchenko (FNAL) – Intel CUDA-Conversion tool exploration
 - D. McDougall, C. Robeck (AMD) – HIP consultation
 - P. Steinbrecher (Intel) – Intel compiler consultation (DPC++ and OpenMP)
 - weekly meetings + notes of varying level of depth in our Slack #portability channel

Refactoring for Perf Portability (led by K. Clark)

- Launch Abstractions
 - Kernel1D, Kernel2D, Kernel3D, Reduction, TransformReduce,
 - most portability frameworks do something like this: Kokkos, Raja, and also Grid
- API Elements
 - memory allocation/copy (`quda_malloc()`)
 - Streams (fixed number and use index as 'stream')
 - Shared memory: `sharedMemory` manager class
 - Constant memory – for large list of arguments (e.g. small matrices)
 - API functions error check internally (architecture dependent status codes are isolated/contained)
- Device constraints & Macro Reduction/Localization
 - `constexpr` functions
 - `SFINAE`, and template-template classes.
- Libraries
 - CUB/hipCUB, => namespace `QudaCub` aliases
 - `cu/hipRand`, `cu/hipFFT` => wrapped into 'shim headers'
 - certain math functions (`sincos` and `rsqrt` and half prec implementations) implemented on host/device
 - straightforward for HIP, since many libraries corresponding to CUDA exist, may be trickier for e.g. Intel
- Miscellany
 - vector types (e.g. `float4`, `int4`) – HIP returned proxy objects / accessors to some structure elements
 - IPC for Peer2Peer seems easy to port between CUDA and HIP

CONSTEXPR



[CppCon17 talk by Ben Deane and Jason Turner](#)

CONSTEXPR



[Also "Don't constexpr all the things" – David Sankel, CppNow 2021](#)

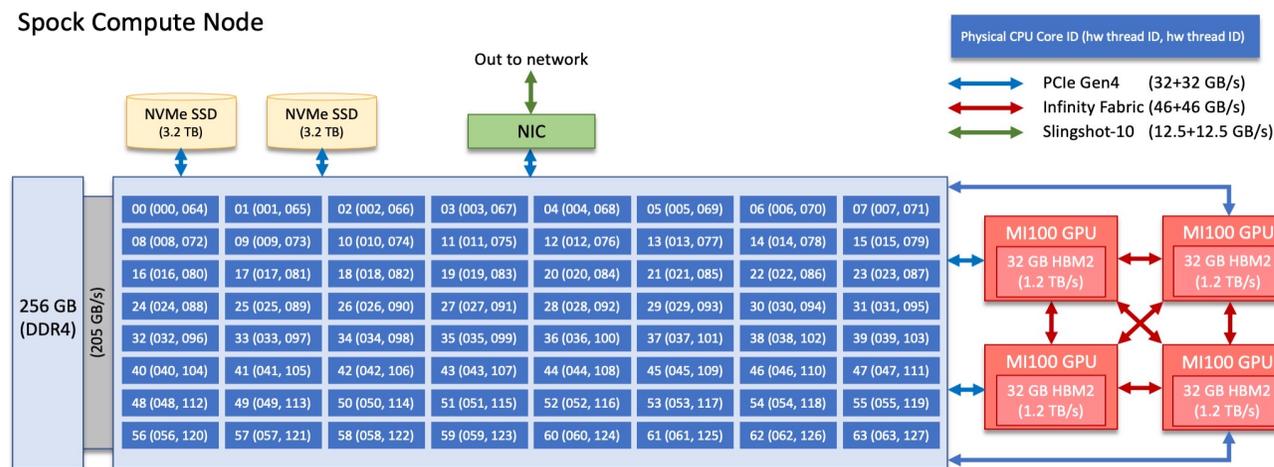
(actually this talk is about Circle)

Spock: OLCF's Frontier Early Access System (EAS)

- 3 Cabinets w. 12 nodes/cabinet => 36 nodes, 144 GPUs total
- Each node has
 - 1x 64 core AMD EPYC 7662 "Rome" CPU (4 NUMA domains) + 256 GB DDR4 memory (205 GB/s)
 - 4x AMD Radeon Instinct MI100 GPUs (gfx908), 32 GB HBM2 @ (1.2 TB/sec)
 - GPU-GPU: All-to-all Infinity Fabric Interconnect, Host-GPU: PCIe Gen4: 32+32 GB/sec
 - 2 x NVMe SSDs (3.2 TB each): 6800 MB/sec read, 4200 MB.sec write
- Slingshot 10 Interconnect: 12.5 + 12.5 GB/sec
- Spock Training Workshop materials: <https://www.olcf.ornl.gov/spock-training>
- Documentation: https://docs.olcf.ornl.gov/systems/spock_quick_start_guide.html



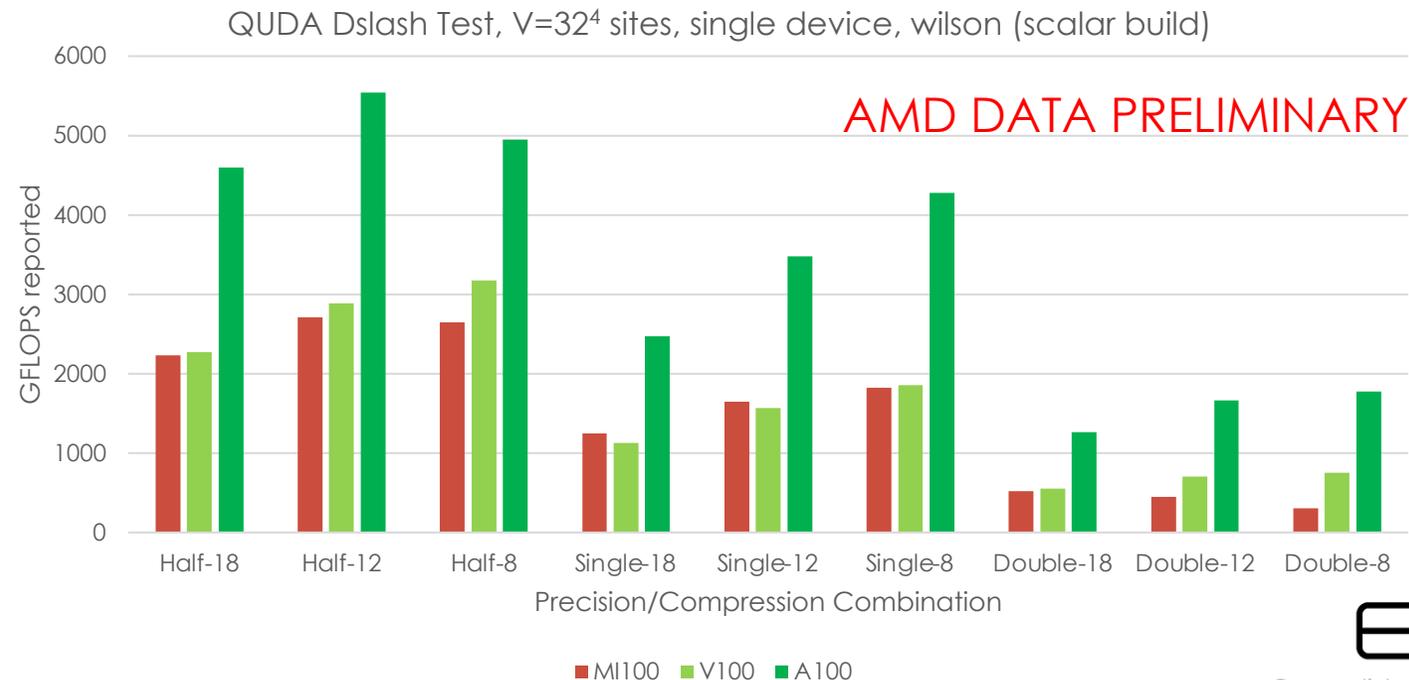
Original Spock Compute Node



QUDA Porting Status

- (All of) the library builds with ROCm 4.2
 - feature/hip-compile-fixes branch
 - P2P & MPI Comms built. Currently undergoing testing and debugging
- All 'Ctest' pass on single AMD GPU
- Intel GPU porting in progress
 - James Osborn is still developing and testing the SYCL port and Xioyong-Jin is working on OpenMP-offload
 - focus is on making sure the refactorings which we discussed allow efficient porting to both programming models (access to shared memories, reductions, etc)

- *A100 data courtesy of E. Weinberg, NVIDIA. Data from **A100 80 GB** part*
 - *~2.0TB/s peak mem. B/W*
 - *Perlmutter has 1.56 TB/sec, 40GB parts*
- *V100 data from Summit*
 - *~900 GB/sec peak mem B/W*
- *MI100 data from Spock*
 - *~1.2TB/sec peak mem B/W*



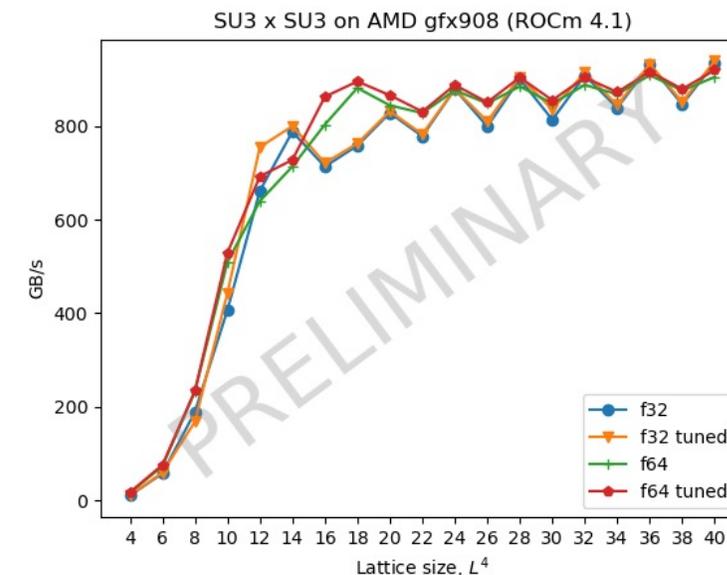
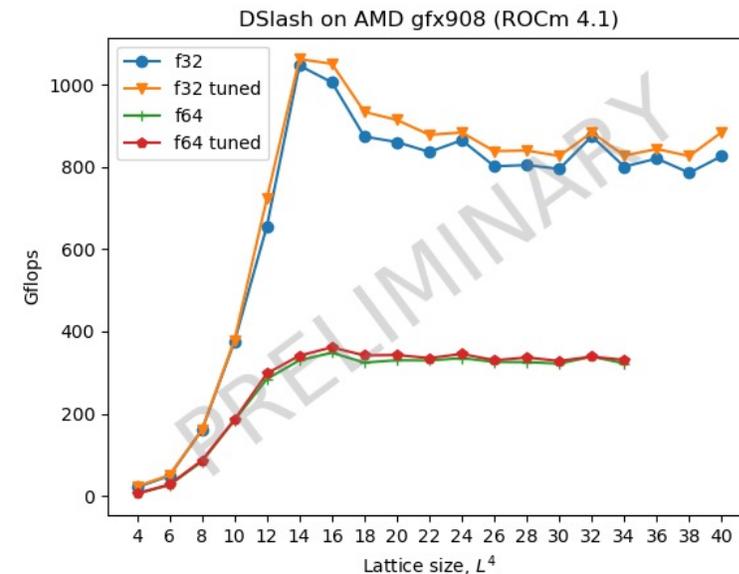
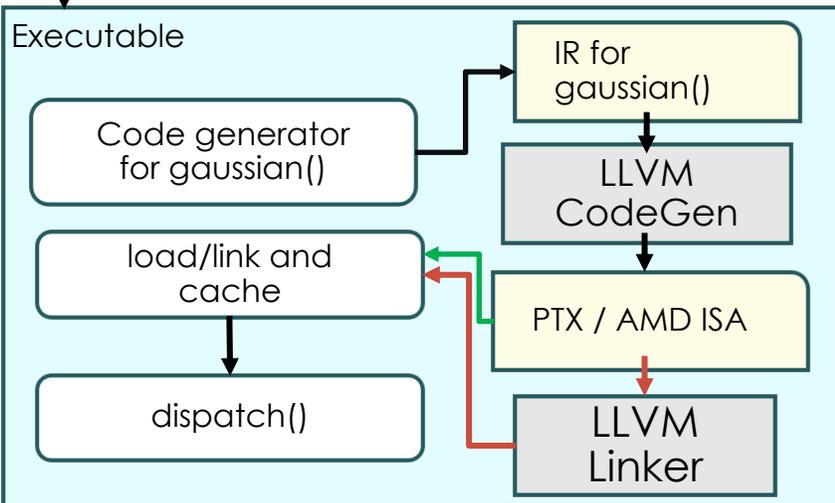
Progress with QDP-JIT

- Frank Winter ported QDP-JIT to AMD GPUs: Presented this conference Wed 7/28
- QDP-JIT can run a full Chroma HMC trajectory on AMD GPU
 - 800+ GFLOPS from Native QDP-JIT Dslash implementation, 800+ GB/sec on SU(3)xSU(3) kernels
 - MI100 has ~1200 GB/sec maximum HBM bandwidth
- AMDGPU backend for LLVM generates ISA rather than an intermediate form like PTX
 - Needs additional linking step
- Intel GPUs next...

C++ Source code

```
LatticeFermion x;
gaussian(x);
```

Compile time Expression Template Magic



Preliminary MI100 results from the ECP All Hands Meeting poster by F. Winter. Courtesy of Frank Winter.

Open slide master to edit

Julia For LQCD

- Interesting work from Akio Tomiya -- poster at this conference.
- Julia uses JIT compilation via LLVM.
- “Very high level” with good C/C++/Python interoperability – ML friendly
- Support for Wilson-Clover & Staggered Fermions, Stout Smearing, RHMC, Heat-Bath, Self Learning Monte Carlo,
- Similar performance to Fortran code
- Related:
 - work by A. Strelchenko (2019 [USQCD All Hands Meeting](#)) for algorithmic exploration

LatticeQCD.jl

: Lattice QCD code with Julia

Akio Tomiya (International professional university of technology in Osaka, Assistant Professor) akio@yukawa.kyoto-u.ac.jp
Yuki Nagai (Japan Atomic Energy Agency, Senior Scientist)

1. Introduction

- Lattice QCD = Multi-dimensional integral over SU(3)

$$S[U, \psi, \bar{\psi}] = \sum_n \left[-\frac{1}{g^2} \text{Re} \text{tr} U_{\mu\nu} + \bar{\psi} (D + m) \psi \right]$$

$$\langle \mathcal{O} \rangle = \frac{1}{Z} \int \mathcal{D}U \mathcal{D}\bar{\psi} \mathcal{D}\psi e^{-S[U, \psi, \bar{\psi}]} \mathcal{O}[U, \psi, \bar{\psi}]$$

$$\mathcal{D}U = \prod_{n \in (Z/L)^4} \prod_{\mu=1}^4 dU_{\mu}(n) \quad >1000 \text{ dimension.}$$
- This integral gives non-perturbative information of QCD
- Monte-Carlo is used to calculate (Numerical error independent to the dimensionality)
- C++/Fortran have been used for simulations since it costs a lot! Supercomputers are needed for large scale calculations
- We make an open source code for lattice QCD with **Julia language!**

2. Julia?

- Programming language for science (Ref. 1) since 2012. Free, open
- Fast as C/Fortran (Fig1), productive as Python (Fig2)

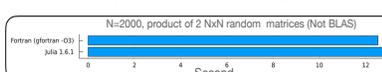
Fig1. 

Fig2.

```
for i in [1,2,3]
  println("Hello world ", i)
end
```

- 33.9k star on Github. NASA uses Julia [2]. Runnable on Supercomputers!
- Easy start: Binary available for Win, macOS and Linux, run everywhere
- Good package control system unlike python environment.
- Just-in-compiling, dynamic type. We can use **Python/Fortran/C** libraries. **Machine learning friendly!**

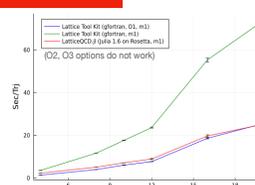
3. Why we make?

- To examine capability of Julia
- Ease of install/compiling
- Machine learning friendly lattice QCD code is needed
- Educational purpose/ Ease of modification

5. Features

- General gauge action (plaq+rect+chair +...) for SU(N) is supported
- Dynamical clover-Wilson (Nf=2), staggered fermions (Nf = 2-8). Both can be run with/without stout.
- (R)HMC, Heatbath (for quenched), self-learning Monte-Carlo, etc are supported
- Measurements: Plaquette, Polyakov loop, Chiral condensate, Pion correlator, topological charge
- Gradient flow with general gauge action
- ILDG I/O support
- Work on Google colab/ batch job / REPL (Julia prompt)
 - (parallelization is in progress)
 - **Parameter wizard**

6. Benchmark



Machine:
 m1 mac mini
 - Julia 1.6.1 + Rosetta2
 - gfortran11 (with/wo O1)

L=4^3 x Lt
 Lt = 4, 8, 10, 12, 16, 20
 kappa = 0.141139
 beta = 5.5
 Nmd = 10, e=0.1
 CG eps = 10-8
 (Default of Lattice tool kit [3])

- We compare with Lattice Tool kit (Fortran) , (same algorithm)
- Ls=4, Lt=4-20, beta = 5.5, kappa = 0.141139, full HMC
- Performance is good so far on single thread/core

7. Summary

- Julia is fast as Fortran/C, productive as Python (easy to write)
- LatticeQCD.jl works well, fast as a fortran code
- Future work: Overlap, domain-wall, parallelization
- (Modified version of) this code used for arXiv 2010.11900 and arXiv 2103.11965. Talk in session 27th, 13:00-, Algorithms

4. USAGE

Only 4 steps! See our Github webpage in details

1. Download Julia binary from the official webpage
2. Add lattice QCD using built-in package control system
3. (optional) Make parameter file with the wizard (type `run_wizard()`)
4. Execute! (type `run_LQCD("my_parameters.jl")`)

We also provide **Google Colab notebook [4]**!

Reference

1. Julia: <https://julialang.org>
2. LTK: <https://mio-mon.rise.hiroshima-u.ac.jp/LTK/>
3. NASA: <https://modelingquora.nasa.gov/docs/DOC-2783>
4. Google Colab <https://bit.ly/3yYtQIG>

LATTICE2021@MIT (Virtual)

Start Lattice calculation in 5 min <https://github.com/akio-tomiya/LatticeQCD.jl>

Abstract: <https://indico.cern.ch/event/1006302/contributions/437850/>

Grid

- Grid is an LQCD framework headed up by P. Boyle and team
 - several Grid related talks/posters at this conference
 - Poster by P. Boyle, A. Yamaguchi, GPT Python bindings tutorial by C. Lehner, etc....
- C++ expression template based LQCD software system
- Portability to several “back-ends”
 - OpenMP
 - HIP
 - CUDA
 - SYCL
- coalescedRead()/Write() – abstraction
- accelerator_for() – abstraction (macro?)
 - wraps actual kernel launch via HIP/SYCL/CUDA
- for more details please contact the Authors
- excellent performance, including near wire-speed saturation of networks reported



Grid: OneCode and FourAPIs

www.github.com/paboyle/Grid



Azusa Yamaguchi (University of Edinburgh)
Peter Boyle (Brookhaven National Laboratory)

Background:

Grid is a C++11 high level library for lattice Gauge theory [1,2]
It aims to be performance portable across all modern architectures
A number of LQCD software efforts make use of Grid for actions, algorithms (solvers, multigrid, HMC, contraction primitives) [3].
Portability in across the Exascale roadmap requires support for AMD (HIP), Intel (SYCL) and Nvidia (CUDA) GPUs in addition to vectorising multicore architectures. Grid is a single source and targets all of these APIs portably.



* CPU computing is also not going away

Covariant programming:

SIMD and SIMT differ semantically in whether local variables are vectors or scalars

Naively poses a barrier to writing single source kernels which vectorise on CPUs and read coalesce on GPUs.

C++ automatic type inference lets you avoid naming the types (vector or scalar) so you can deduce the type according to the architecture following simply programming idioms.

Combined with `accelerator_for` abstraction capturing and offloading loop bodies in `device lambda functions` we can write high performance kernel code that runs on all four API's.

FourAPIs and OneCode

```

Portability 101 – abstract the interfaces
// CUDA specific
accelerator_inline int accelerator2DFT(int Nside) {
    return hipThreadIdx_z;
}
// HIP specific
accelerator_inline int accelerator2DFT(int Nside) {
    return __sycl_get_device_id();
}
// SYCL specific
accelerator_for2D(Iter1, num1, iter2, num2, nside, ...) {
    // ...
}
// OpenMP specific
accelerator_for2D(Iter1, num1, iter2, num2, nside, ...) {
    // ...
}
    
```

Similar ideas to RAJA and Kokkos – use device lambda capture;
lean internal interface to offload – HIP and OpenMP similar

HIP and OpenMP targets

```

// HIP specific
accelerator_for2D(Iter1, num1, iter2, num2, nside, ...) {
    // ...
}
// OpenMP specific
accelerator_for2D(Iter1, num1, iter2, num2, nside, ...) {
    // ...
}
    
```

Wilson dslash kernel (sketch)

Same optimised kernel transforms covariantly between GPU and CPU

Return type of `coalescedRead` dictates whether SOA or scalar structs are processed in each logical thread

Thread interleaving happens naturally on GPU with memory resident data stored in SOA.

CPU processes loop as SOA data with good vectorisation.

Nvidia performance:

Excellent performance on ATOS sequana A100 x 4 nodes with 4x HDR infiniband (e.g. Juelich Booster + Edinburgh Tursa systems) – communication is key 6TF/s per node in multi-node operation.

```

template<class T>
void WilsonDslashKernel(
    double* d, double* d2, double* d3, double* d4, double* d5, double* d6, double* d7, double* d8, double* d9, double* d10, double* d11, double* d12, double* d13, double* d14, double* d15, double* d16, double* d17, double* d18, double* d19, double* d20, double* d21, double* d22, double* d23, double* d24, double* d25, double* d26, double* d27, double* d28, double* d29, double* d30, double* d31, double* d32, double* d33, double* d34, double* d35, double* d36, double* d37, double* d38, double* d39, double* d40, double* d41, double* d42, double* d43, double* d44, double* d45, double* d46, double* d47, double* d48, double* d49, double* d50, double* d51, double* d52, double* d53, double* d54, double* d55, double* d56, double* d57, double* d58, double* d59, double* d60, double* d61, double* d62, double* d63, double* d64, double* d65, double* d66, double* d67, double* d68, double* d69, double* d70, double* d71, double* d72, double* d73, double* d74, double* d75, double* d76, double* d77, double* d78, double* d79, double* d80, double* d81, double* d82, double* d83, double* d84, double* d85, double* d86, double* d87, double* d88, double* d89, double* d90, double* d91, double* d92, double* d93, double* d94, double* d95, double* d96, double* d97, double* d98, double* d99, double* d100, double* d101, double* d102, double* d103, double* d104, double* d105, double* d106, double* d107, double* d108, double* d109, double* d110, double* d111, double* d112, double* d113, double* d114, double* d115, double* d116, double* d117, double* d118, double* d119, double* d120, double* d121, double* d122, double* d123, double* d124, double* d125, double* d126, double* d127, double* d128, double* d129, double* d130, double* d131, double* d132, double* d133, double* d134, double* d135, double* d136, double* d137, double* d138, double* d139, double* d140, double* d141, double* d142, double* d143, double* d144, double* d145, double* d146, double* d147, double* d148, double* d149, double* d150, double* d151, double* d152, double* d153, double* d154, double* d155, double* d156, double* d157, double* d158, double* d159, double* d160, double* d161, double* d162, double* d163, double* d164, double* d165, double* d166, double* d167, double* d168, double* d169, double* d170, double* d171, double* d172, double* d173, double* d174, double* d175, double* d176, double* d177, double* d178, double* d179, double* d180, double* d181, double* d182, double* d183, double* d184, double* d185, double* d186, double* d187, double* d188, double* d189, double* d190, double* d191, double* d192, double* d193, double* d194, double* d195, double* d196, double* d197, double* d198, double* d199, double* d200, double* d201, double* d202, double* d203, double* d204, double* d205, double* d206, double* d207, double* d208, double* d209, double* d210, double* d211, double* d212, double* d213, double* d214, double* d215, double* d216, double* d217, double* d218, double* d219, double* d220, double* d221, double* d222, double* d223, double* d224, double* d225, double* d226, double* d227, double* d228, double* d229, double* d230, double* d231, double* d232, double* d233, double* d234, double* d235, double* d236, double* d237, double* d238, double* d239, double* d240, double* d241, double* d242, double* d243, double* d244, double* d245, double* d246, double* d247, double* d248, double* d249, double* d250, double* d251, double* d252, double* d253, double* d254, double* d255, double* d256, double* d257, double* d258, double* d259, double* d260, double* d261, double* d262, double* d263, double* d264, double* d265, double* d266, double* d267, double* d268, double* d269, double* d270, double* d271, double* d272, double* d273, double* d274, double* d275, double* d276, double* d277, double* d278, double* d279, double* d280, double* d281, double* d282, double* d283, double* d284, double* d285, double* d286, double* d287, double* d288, double* d289, double* d290, double* d291, double* d292, double* d293, double* d294, double* d295, double* d296, double* d297, double* d298, double* d299, double* d300, double* d301, double* d302, double* d303, double* d304, double* d305, double* d306, double* d307, double* d308, double* d309, double* d310, double* d311, double* d312, double* d313, double* d314, double* d315, double* d316, double* d317, double* d318, double* d319, double* d320, double* d321, double* d322, double* d323, double* d324, double* d325, double* d326, double* d327, double* d328, double* d329, double* d330, double* d331, double* d332, double* d333, double* d334, double* d335, double* d336, double* d337, double* d338, double* d339, double* d340, double* d341, double* d342, double* d343, double* d344, double* d345, double* d346, double* d347, double* d348, double* d349, double* d350, double* d351, double* d352, double* d353, double* d354, double* d355, double* d356, double* d357, double* d358, double* d359, double* d360, double* d361, double* d362, double* d363, double* d364, double* d365, double* d366, double* d367, double* d368, double* d369, double* d370, double* d371, double* d372, double* d373, double* d374, double* d375, double* d376, double* d377, double* d378, double* d379, double* d380, double* d381, double* d382, double* d383, double* d384, double* d385, double* d386, double* d387, double* d388, double* d389, double* d390, double* d391, double* d392, double* d393, double* d394, double* d395, double* d396, double* d397, double* d398, double* d399, double* d400, double* d401, double* d402, double* d403, double* d404, double* d405, double* d406, double* d407, double* d408, double* d409, double* d410, double* d411, double* d412, double* d413, double* d414, double* d415, double* d416, double* d417, double* d418, double* d419, double* d420, double* d421, double* d422, double* d423, double* d424, double* d425, double* d426, double* d427, double* d428, double* d429, double* d430, double* d431, double* d432, double* d433, double* d434, double* d435, double* d436, double* d437, double* d438, double* d439, double* d440, double* d441, double* d442, double* d443, double* d444, double* d445, double* d446, double* d447, double* d448, double* d449, double* d450, double* d451, double* d452, double* d453, double* d454, double* d455, double* d456, double* d457, double* d458, double* d459, double* d460, double* d461, double* d462, double* d463, double* d464, double* d465, double* d466, double* d467, double* d468, double* d469, double* d470, double* d471, double* d472, double* d473, double* d474, double* d475, double* d476, double* d477, double* d478, double* d479, double* d480, double* d481, double* d482, double* d483, double* d484, double* d485, double* d486, double* d487, double* d488, double* d489, double* d490, double* d491, double* d492, double* d493, double* d494, double* d495, double* d496, double* d497, double* d498, double* d499, double* d500, double* d501, double* d502, double* d503, double* d504, double* d505, double* d506, double* d507, double* d508, double* d509, double* d510, double* d511, double* d512, double* d513, double* d514, double* d515, double* d516, double* d517, double* d518, double* d519, double* d520, double* d521, double* d522, double* d523, double* d524, double* d525, double* d526, double* d527, double* d528, double* d529, double* d530, double* d531, double* d532, double* d533, double* d534, double* d535, double* d536, double* d537, double* d538, double* d539, double* d540, double* d541, double* d542, double* d543, double* d544, double* d545, double* d546, double* d547, double* d548, double* d549, double* d550, double* d551, double* d552, double* d553, double* d554, double* d555, double* d556, double* d557, double* d558, double* d559, double* d560, double* d561, double* d562, double* d563, double* d564, double* d565, double* d566, double* d567, double* d568, double* d569, double* d570, double* d571, double* d572, double* d573, double* d574, double* d575, double* d576, double* d577, double* d578, double* d579, double* d580, double* d581, double* d582, double* d583, double* d584, double* d585, double* d586, double* d587, double* d588, double* d589, double* d590, double* d591, double* d592, double* d593, double* d594, double* d595, double* d596, double* d597, double* d598, double* d599, double* d600, double* d601, double* d602, double* d603, double* d604, double* d605, double* d606, double* d607, double* d608, double* d609, double* d610, double* d611, double* d612, double* d613, double* d614, double* d615, double* d616, double* d617, double* d618, double* d619, double* d620, double* d621, double* d622, double* d623, double* d624, double* d625, double* d626, double* d627, double* d628, double* d629, double* d630, double* d631, double* d632, double* d633, double* d634, double* d635, double* d636, double* d637, double* d638, double* d639, double* d640, double* d641, double* d642, double* d643, double* d644, double* d645, double* d646, double* d647, double* d648, double* d649, double* d650, double* d651, double* d652, double* d653, double* d654, double* d655, double* d656, double* d657, double* d658, double* d659, double* d660, double* d661, double* d662, double* d663, double* d664, double* d665, double* d666, double* d667, double* d668, double* d669, double* d670, double* d671, double* d672, double* d673, double* d674, double* d675, double* d676, double* d677, double* d678, double* d679, double* d680, double* d681, double* d682, double* d683, double* d684, double* d685, double* d686, double* d687, double* d688, double* d689, double* d690, double* d691, double* d692, double* d693, double* d694, double* d695, double* d696, double* d697, double* d698, double* d699, double* d700, double* d701, double* d702, double* d703, double* d704, double* d705, double* d706, double* d707, double* d708, double* d709, double* d710, double* d711, double* d712, double* d713, double* d714, double* d715, double* d716, double* d717, double* d718, double* d719, double* d720, double* d721, double* d722, double* d723, double* d724, double* d725, double* d726, double* d727, double* d728, double* d729, double* d730, double* d731, double* d732, double* d733, double* d734, double* d735, double* d736, double* d737, double* d738, double* d739, double* d740, double* d741, double* d742, double* d743, double* d744, double* d745, double* d746, double* d747, double* d748, double* d749, double* d750, double* d751, double* d752, double* d753, double* d754, double* d755, double* d756, double* d757, double* d758, double* d759, double* d760, double* d761, double* d762, double* d763, double* d764, double* d765, double* d766, double* d767, double* d768, double* d769, double* d770, double* d771, double* d772, double* d773, double* d774, double* d775, double* d776, double* d777, double* d778, double* d779, double* d780, double* d781, double* d782, double* d783, double* d784, double* d785, double* d786, double* d787, double* d788, double* d789, double* d790, double* d791, double* d792, double* d793, double* d794, double* d795, double* d796, double* d797, double* d798, double* d799, double* d800, double* d801, double* d802, double* d803, double* d804, double* d805, double* d806, double* d807, double* d808, double* d809, double* d810, double* d811, double* d812, double* d813, double* d814, double* d815, double* d816, double* d817, double* d818, double* d819, double* d820, double* d821, double* d822, double* d823, double* d824, double* d825, double* d826, double* d827, double* d828, double* d829, double* d830, double* d831, double* d832, double* d833, double* d834, double* d835, double* d836, double* d837, double* d838, double* d839, double* d840, double* d841, double* d842, double* d843, double* d844, double* d845, double* d846, double* d847, double* d848, double* d849, double* d850, double* d851, double* d852, double* d853, double* d854, double* d855, double* d856, double* d857, double* d858, double* d859, double* d860, double* d861, double* d862, double* d863, double* d864, double* d865, double* d866, double* d867, double* d868, double* d869, double* d870, double* d871, double* d872, double* d873, double* d874, double* d875, double* d876, double* d877, double* d878, double* d879, double* d880, double* d881, double* d882, double* d883, double* d884, double* d885, double* d886, double* d887, double* d888, double* d889, double* d890, double* d891, double* d892, double* d893, double* d894, double* d895, double* d896, double* d897, double* d898, double* d899, double* d900, double* d901, double* d902, double* d903, double* d904, double* d905, double* d906, double* d907, double* d908, double* d909, double* d910, double* d911, double* d912, double* d913, double* d914, double* d915, double* d916, double* d917, double* d918, double* d919, double* d920, double* d921, double* d922, double* d923, double* d924, double* d925, double* d926, double* d927, double* d928, double* d929, double* d930, double* d931, double* d932, double* d933, double* d934, double* d935, double* d936, double* d937, double* d938, double* d939, double* d940, double* d941, double* d942, double* d943, double* d944, double* d945, double* d946, double* d947, double* d948, double* d949, double* d950, double* d951, double* d952, double* d953, double* d954, double* d955, double* d956, double* d957, double* d958, double* d959, double* d960, double* d961, double* d962, double* d963, double* d964, double* d965, double* d966, double* d967, double* d968, double* d969, double* d970, double* d971, double* d972, double* d973, double* d974, double* d975, double* d976, double* d977, double* d978, double* d979, double* d980, double* d981, double* d982, double* d983, double* d984, double* d985, double* d986, double* d987, double* d988, double* d989, double* d990, double* d991, double* d992, double* d993, double* d994, double* d995, double* d996, double* d997, double* d998, double* d999, double* d1000, double* d1001, double* d1002, double* d1003, double* d1004, double* d1005, double* d1006, double* d1007, double* d1008, double* d1009, double* d1010, double* d1011, double* d1012, double* d1013, double* d1014, double* d1015, double* d1016, double* d1017, double* d1018, double* d1019, double* d1020, double* d1021, double* d1022, double* d1023, double* d1024, double* d1025, double* d1026, double* d1027, double* d1028, double* d1029, double* d1030, double* d1031, double* d1032, double* d1033, double* d1034, double* d1035, double* d1036, double* d1037, double* d1038, double* d1039, double* d1040, double* d1041, double* d1042, double* d1043, double* d1044, double* d1045, double* d1046, double* d1047, double* d1048, double* d1049, double* d1050, double* d1051, double* d1052, double* d1053, double* d1054, double* d1055, double* d1056, double* d1057, double* d1058, double* d1059, double* d1060, double* d1061, double* d1062, double* d1063, double* d1064, double* d1065, double* d1066, double* d1067, double* d1068, double* d1069, double* d1070, double* d1071, double* d1072, double* d1073, double* d1074, double* d1075, double* d1076, double* d1077, double* d1078, double* d1079, double* d1080, double* d1081, double* d1082, double* d1083, double* d1084, double* d1085, double* d1086, double* d1087, double* d1088, double* d1089, double* d1090, double* d1091, double* d1092, double* d1093, double* d1094, double* d1095, double* d1096, double* d1097, double* d1098, double* d1099, double* d1100, double* d1101, double* d1102, double* d1103, double* d1104, double* d1105, double* d1106, double* d1107, double* d1108, double* d1109, double* d1110, double* d1111, double* d1112, double* d1113, double* d1114, double* d1115, double* d1116, double* d1117, double* d1118, double* d1119, double* d1120, double* d1121, double* d1122, double* d1123, double* d1124, double* d1125, double* d1126, double* d1127, double* d1128, double* d1129, double* d1130, double* d1131, double* d1132, double* d1133, double* d1134, double* d1135, double* d1136, double* d1137, double* d1138, double* d1139, double* d1140, double* d1141, double* d1142, double* d1143, double* d1144, double* d1145, double* d1146, double* d1147, double* d1148, double* d1149, double* d1150, double* d1151, double* d1152, double* d1153, double* d1154, double* d1155, double* d1156, double* d1157, double* d1158, double* d1159, double* d1160, double* d1161, double* d1162, double* d1163, double* d1164, double* d1165, double* d1166, double* d1167, double* d1168, double* d1169, double* d1170, double* d1171, double* d1172, double* d1173, double* d1174, double* d1175, double* d1176, double* d1177, double* d1178, double* d1179, double* d1180, double* d1181, double* d1182, double* d1183, double* d1184, double* d1185, double* d1186, double* d1187, double* d1188, double* d1189, double* d1190, double* d1191, double* d1192, double* d1193, double* d1194, double* d1195, double* d1196, double* d1197, double* d1198, double* d1199, double* d1200, double* d1201, double* d1202, double* d1203, double* d1204, double* d1205, double* d1206, double* d1207, double* d1208, double* d1209, double* d1210, double* d1211, double* d1212, double* d1213, double* d1214, double* d1215, double* d1216, double* d1217, double* d1218, double* d1219, double* d1220, double* d1221, double* d1222, double* d1223, double* d1224, double* d1225, double* d1226, double* d1227, double* d1228, double* d1229, double* d1230, double* d1231, double* d1232, double* d1233, double* d1234, double* d1235, double* d1236, double* d1237, double* d1238, double* d1239, double* d1240, double* d1241, double* d1242, double* d1243, double* d1244, double* d1245, double* d1246, double* d1247, double* d1248, double* d1249, double* d1250, double* d1251, double* d1252, double* d1253, double* d1254, double* d1255, double* d1256, double* d1257, double* d1258, double* d1259, double* d1260, double* d1261, double* d1262, double* d1263, double* d1264, double* d1265, double* d1266, double* d1267, double* d1268, double* d1269, double* d1270, double* d1271, double* d1272, double* d1273, double* d1274, double* d1275, double* d1276, double* d1277, double* d1278, double* d1279, double* d1280, double* d1281, double* d1282, double* d1283, double* d1284, double* d1285, double* d1286, double* d1287, double* d1288, double* d1289, double* d1290, double* d1291, double* d1292, double* d1293, double* d1294, double* d1295, double* d1296, double* d1297, double* d1298, double* d1299, double* d1300, double* d1301, double* d1302, double* d1303, double* d1304, double* d1305, double* d1306, double* d1307, double* d1308, double* d1309, double* d1310, double* d1311, double* d1312, double* d1313, double* d1314, double* d1315, double* d1316, double* d1317, double* d1318, double* d1319, double* d1320, double* d1321, double* d1322, double* d1323, double* d1324, double* d1325, double* d1326, double* d1327, double* d1328, double* d1329, double* d1330, double* d1331, double* d1332, double* d1333, double* d1334, double* d1335, double* d1336, double* d1337, double* d1338, double* d1339, double* d1340, double* d1341, double* d1342, double* d1343, double* d1344, double* d1345, double* d1346, double* d1347, double* d1348, double* d1349, double* d1350, double* d1351, double* d1352, double* d1353, double* d1354, double* d1355, double* d1356, double* d1357, double* d1358, double* d1359, double* d1360, double* d1361, double* d1362, double* d1363, double* d1364, double* d1365, double* d1366, double* d1367, double* d1368, double* d1369, double* d1370, double* d1371, double* d1372, double* d1373, double* d1374, double* d1375, double* d1376, double* d1377, double* d1378, double* d1379, double* d1380, double* d1381, double* d1382, double* d1383, double* d1384, double* d1385, double* d1386, double* d1387, double* d1388, double* d1389, double* d1390, double* d1391, double* d1392, double* d1393, double* d1394, double* d1395, double* d1396, double* d1397, double* d1398, double* d1399, double* d1400, double* d1401, double* d1402, double* d1403, double* d1404, double* d1405, double* d1406, double* d1407, double* d1408, double* d1409, double* d1410, double* d1411, double* d1412, double* d1413, double* d1414, double* d1415, double* d1416, double* d1417, double* d1418, double* d1419, double* d1420, double* d1421, double* d1422, double* d1423, double* d14
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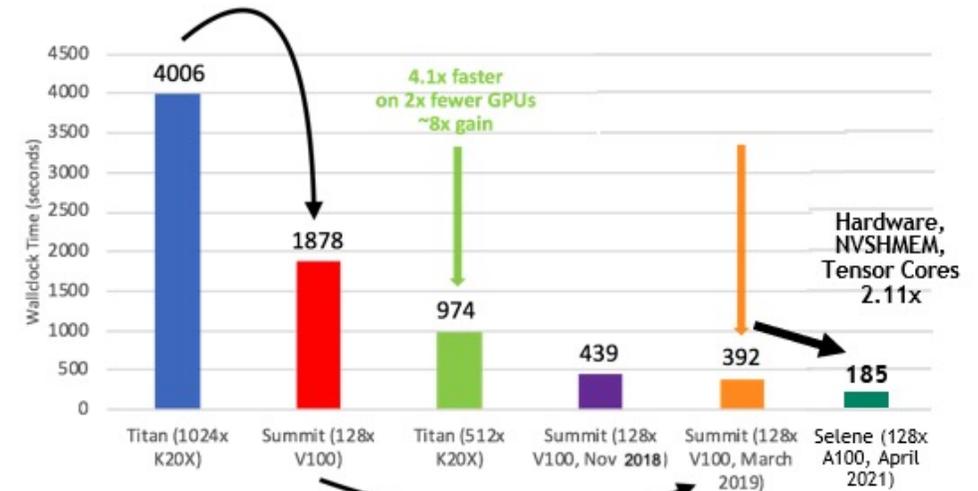
Summary

- Very exciting time as code porting work is coming to fruition
 - Perlmutter is here, we are looking forward to hopping on...
 - Frontier will be starting to arrive very soon
 - Slightly stressful: tooling is still maturing in some cases, bugs to iron out
- Some interesting new machines on the horizon
 - Aurora at ALCF
 - [Large A64FX based system by Atos with GENCI and CEA in France](#)
 - [A system based on the Grace CPU from NVIDIA at Los Alamos](#)
- With so many architectures it is important to have a good performance portability strategy
- Algorithms also advancing – sadly not enough time to cover in this talk
 - Multigrid algorithms advances (E. Weinberg, P. Boyle, ...)
 - Advances in Domain Wall algorithms: Multi-Grid and DDHMC (talk by Peter Boyle, Chulwoo Jung and others)
 - Algorithms to combat critical slowing down and adding machine learning to accelerate Monte-Carlo methods. (talks by Sam Foreman & Xiao-Yong Jin)
 - and many more...

Departing Plot

- In 2018 we measured a baseline of our HMC gauge generation algorithm on 1024 nodes of Titan at OLCF
 - No multigrid yet, but GPU accelerated – K20X GPUs
- On this figure we can track improvement of algorithms, software and algorithm tuning
- At the current time what took 4006 sec. on 1024 Titan nodes, takes only 185 sec. on the NVIDIA Selene System (#6 on Top500 system)
 - 21.6x speedup on 8x fewer devices
 - 173x “integrated improvement”
- Looking forward to adding some Frontier data on this plot soon
- Where will new advances take us next?

Hardware: 2.13x wall-time on 8x fewer GPUs = 17x



Algorithms, Software and Tuning: 4.79x

Chroma w/ QDP-JIT and QUDA, ECP FOM data,
V=64³x128 sites, $m_{\pi} \sim 172$ MeV, (QDP-JIT by F. Winter,
Jefferson Lab)

Original figure credit Balint Joo -2
years ago, new numbers from M.
Wagner



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