



# Re-commissioning of the Interlock Systems BIS, SMP, WIC, PIC and FMCM after LS2

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*TE-MPE-MI*

19<sup>th</sup> February 2021

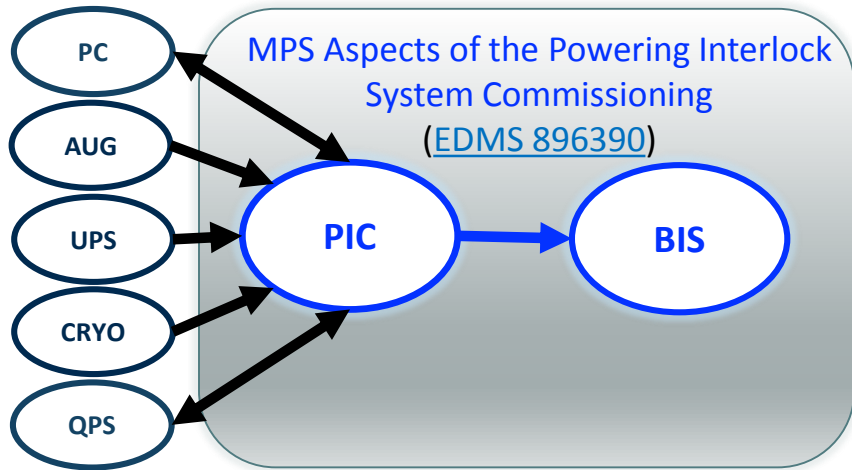
# Outline

- PIC : EDMS [896390 v.4.0](#)
- FMCM : EDMS [896393 v.3.2](#)
- WIC : EDMS [896395 v.3.0](#)
- SMP : EDMS [1112187 v.1.0](#)
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# PIC – MPS Commissioning



## On testbench:

- PLC & CPLD Software validation (Before HWC)

## On the 36 PIC systems:

- UPS & AUG tests done with EN-EL (~ 8 days)
- CRYO tests done with CCC-TI (~1h)
- QPS-PC tests with OP via Acctesting/pmea.
- PIC-BIC tests with OP via Acctesting

Sequence of test which validates the commissioning of the **PIC** for the **36** individual powering interlock controllers (PIC) installed in the LHC.

## Automated Masking of the Global Protection Mechanism (GPM) for [Low Circuit Energies \(EDMS 1360776\)](#)

- The **GPM** triggers a preventive discharge of magnet circuits in the vicinity of a main magnet that quenched.
- **ECR:** LHC-CIP-EC-0005 ([EDMS 2232247](#))
- The GPM activation is from now on **dependent on the current into the main circuits (arcs only)**.

$GPM\_AM = \text{PAR\_GPM\_AM} \cdot GPM\_AM\_ENB \cdot \text{EXP\_GPM\_M}$   
 $(\text{DISABLE}, GPM\_AM, \text{ENABLE}) \text{ OR } \text{EXP\_GPM\_M}$

$GPM\_AM(I_{mb}, I_{dq}, I_{fq})$  (ON, OFF, Other)

$0 \leq I_{mb} \leq Th_{mb} \text{ AND } 0 \leq I_{dq} \leq Th_{dq} \text{ AND } 0 \leq I_{fq} \leq Th_{fq}$

Where

- $I_{mb}$  = Main bend Current
- $I_{dq}$  = Main Defocusing Quadrupole Current
- $I_{fq}$  = Main focusing Quadrupole Current
- $Th_{mb}$  = Main Bend Current Threshold
- $Th_{dq}$  = Main Defocusing Quadrupole Current Threshold
- $Th_{fq}$  = Main focusing Quadrupole Current Threshold

GPM\_AM = GPM Automated Mask  
 PAR\_GPM\_AM = GPM Automated Mask Parameter  
 GPM\_AM\_ENB = GPM Automated Mask Enabling (chap. 3.5)  
 EXP\_GPM\_M = GPM Expert Mask (Manual and time limited) [3]

**GPM is disabled below a defined current threshold**

Sector	RB Current	RQD Current	RQF Current	Threshold	Calculated Auto Mask (FESA)	Auto Mask PLC	Auto Mask Enal.	Auto Mask Enable	Auto Mask Disable
S12	-0.1889330446	-0.0262001957	-0.0433969236	1000	TRUE	TRUE	TRUE	S12 Enable	S12 Disable
S23	-0.0330509915	-0.0563991516	-0.0965707153	1000	TRUE	TRUE	TRUE	S23 Enable	S23 Disable
S34	0.00916726980	-0.0445652902	-0.1023662760	1000	TRUE	TRUE	TRUE	S34 Enable	S34 Disable
S45	0.00030786357	-0.0925481393	-0.0756690651	1000	TRUE	TRUE	TRUE	S45 Enable	S45 Disable
S56	-0.0724490582	-0.0841585099	-0.0162087995	1000	TRUE	TRUE	TRUE	S56 Enable	S56 Disable
S67	-0.0243317298	-0.0775092691	-0.0687390416	1000	TRUE	TRUE	TRUE	S67 Enable	S67 Disable
S78	0.5973951816	-0.1080773770	-0.0261492228	1000	TRUE	TRUE	TRUE	S78 Enable	S78 Disable
S81	6.79862819158	-0.1173519119	-0.0570168085	1000	TRUE	TRUE	TRUE	S81 Enable	S81 Disable

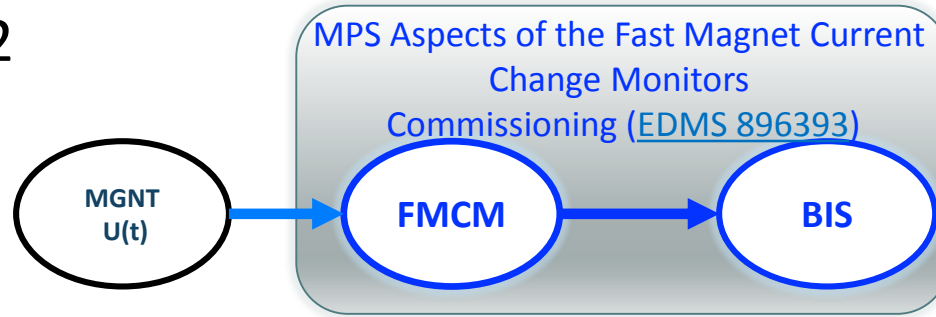
## Automated Masking of the GPM for Low Circuit Energies

- **IST** document ([EDMS 531823](#)) has been updated to add tests for the automated masking of the GPM function.
- The LS2 upgraded **PLC software** has been tested successfully on the PIC automated test bench (IST)
- **16 tests** (2 / arcs) added in the commissioning of the PIC **to be carried out manually by OP** to validate the new **Automated GPM function**:
  - Start at least one circuit (Power Permit)
  - Set an essential circuit to Fast Power Abort (FPA)
  - Start and Ramp the RB or RQD or RQF above the threshold (1kA)
  - Check all started circuits goes to FPA
- **PIC automated test**: Test configuration for maskable/unmaskable circuits towards the Beam Interlock system by provoking an FGC\_STATE failure in all power converters of the concerned PICs.
- **PIC commissioning procedures to be updated for the GPM and circulated.**

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## Changes in LS2



- **2x FMCM** devices protecting TT60 (MBS and MBB magnets) exchanged to get monitoring.
- **MPS tests: 1 or 2 days** duration for FMCM
- MPS tests **to be repeated** Jan 2022 ([EDMS 896393](#)) - normally performed by OP in parallel with low intensity beam commissioning:
  - For each FMCM, program a current step into the powering cycle (TL devices) or create an FGC\_STATE fault on the power converter (LHC) and validate the correct triggering of the FMCM with the BIS. Optimize threshold if required with increasing beam intensity/energy.
  - For each FMCM (or a selection in case of a short winter stop), program a current step into the powering cycle (or provoke an FGC\_STATE fault) and validate the correct triggering of the FMCM with the BIS; Determine the maximum beam excursion observed in the vacuum chambers of the TL/LHC and possible beam losses before the beam was dumped
  - For a selection of FMCMs (with a priority on RD1 and RD34), program a current step into the powering cycle (or provoke an FGC\_STATE fault) and validate the correct triggering of the FMCM with the BIS

**No change in the commissioning of the FMCM**



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# WIC Software changes

## All 8 WIC PLCs upgraded to the latest version of the generic code

- V3.12
- Changes in the matrices only for P1, P5 and P7

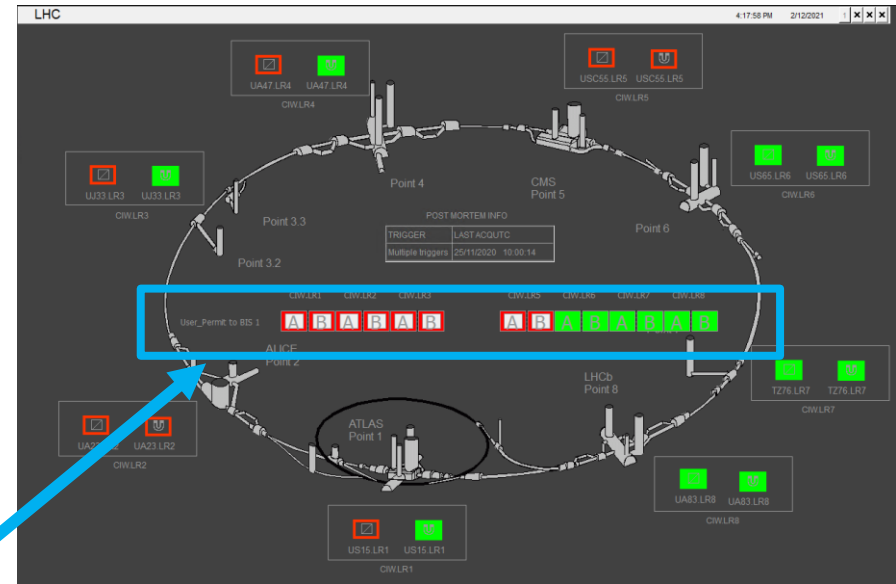
## WinCC\_OA supervision upgraded

- HMI
- New generic magnet & PC widgets

Status of redundant “User Permit” signals sent to the BIS are now shown on the main faceplate

- No connection in P4

In collaboration with BE-ICS



HMI for the LHC (Status on 12.02.2021)

# Beam Beam Compensation Wire

## In Point 1 and Point 5

The two WIC systems were modified to request a “Beam Dump” (to the BIS) in case of:

- **Over-heating of a BBCW**
- **Fault on a BBCW power converter**

ECR: [LHC-TC-EC-0019](#)

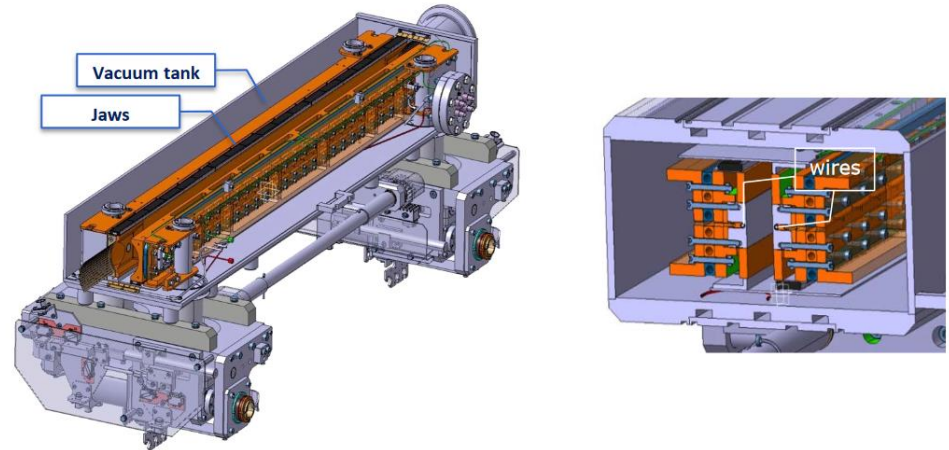


Figure 1 - 3D drawing of Wire-in-jaw collimator (courtesy of L. Gentini)

It has been agreed with BE-BI that, in case of failure on the BBCW side, that could not be repaired in a reasonable amount of time, **BE-BI would bridge the BBCW signal sent to the WIC** in order to resume operation with beam

→ **No modification needed on the WIC side (Best effort piquet service)**

The BBCW power converters are managed by SY-EPC as any other LHC power converters

# Replace 2 magnets by absorbers and reconfiguration of the MQWA and MQWB circuits

## Point 7:

- MQWA.E5L7 and MQWA.E5R7 magnet were removed and replaced by absorbers
- The respective MQWB magnets of the area (MQWB.5L7 and MQWB.5R7) were disconnected from their power supplies and included in the MQWA circuits.



The WIC matrix and connections were modified accordingly and tested successfully

ECR: [LHC-MW-EC-0002](#)

Old circuit	Old slots	New circuit	New slots
RQ5.LR7	MQWA.A5L7	RQ5.LR7	MQWA.A5L7
RQ5.LR7	MQWA.B5L7	RQ5.LR7	MQWA.B5L7
RQT5.L7	MQWB.5L7	RQ5.LR7	MQWA.F5L7
RQ5.LR7	MQWA.C5L7	RQ5.LR7	MQWA.C5L7
RQ5.LR7	MQWA.D5L7	RQ5.LR7	MQWA.D5L7
RQ5.LR7	MQWA.E5L7	removed	removed
RQ5.LR7	MQWA.A5R7	RQ5.LR7	MQWA.A5R7
RQ5.LR7	MQWA.B5R7	RQ5.LR7	MQWA.B5R7
RQT5.R7	MQWB.5R7	RQ5.LR7	MQWA.F5R7
RQ5.LR7	MQWA.C5R7	RQ5.LR7	MQWA.C5R7
RQ5.LR7	MQWA.D5R7	RQ5.LR7	MQWA.D5R7
RQ5.LR7	MQWA.E5R7	removed	removed

## MPS Aspects of the Warm Magnet Interlock System Commissioning - [LHC-OP-MPS-0010](#) (2016)

- The WIC IST tests are done in **3 steps**:
  1. Test the magnet connections to the WIC (Tunnel Access)
  2. Test the PC connections with EPC (Remotely)
  3. Test the WIC/BIS connections (Remotely)
- According to LHC-OP-MPS-0010 (EDMS 896395), nothing to be repeated after IST



**UP TO DATE**

GENERIC PROCEDURE

VALID FOR ALL WIC SYSTEMS

### Status today:

- **IST (Steps 1 and 2) almost finished**
  - Except P5. MBWMD.1L2 in Alice exp. area will be re-installed in May 21<sup>st</sup>
- **IST Step 3** to be done when all conditions are met.

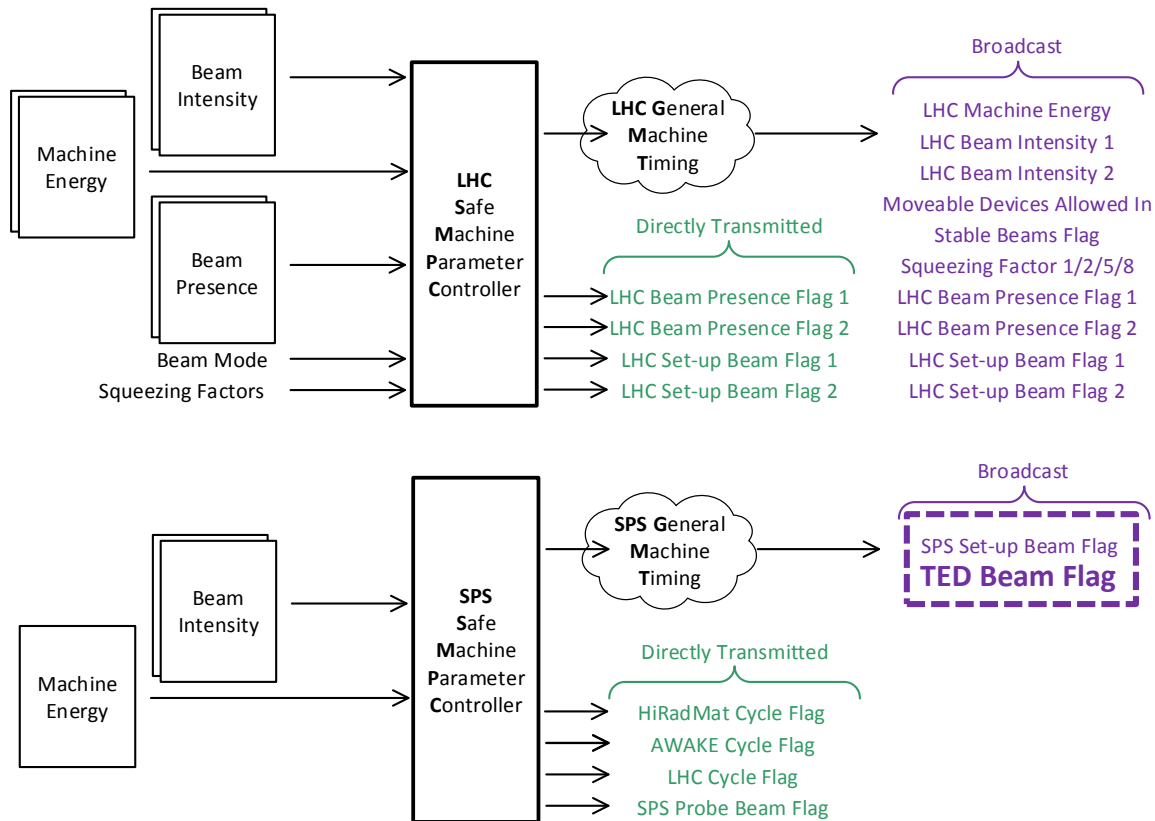
### We missed the occasion to test a first version of “AccTesting” for the WIC

- The overall readiness of the WIC is assured by a **heat run** (performed after the interlock tests)
- The magnets and PCs in point 4 won't be tested as they are **not used** during LHC operation

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# Safe Machine Parameter



# SMP-SPS – Frames for Extraction BIS

- **TED Intensity Limit**  $\leq 3.5 \times 10^{13}$  p

EDMS: [SPS-OTH-ES-0001](#)

- SMP-SPS:

- **Setup Beam Flag (SBF)**
- **TED Beam Flag (TBF)**
- **Probe Beam Flag (PBF)**

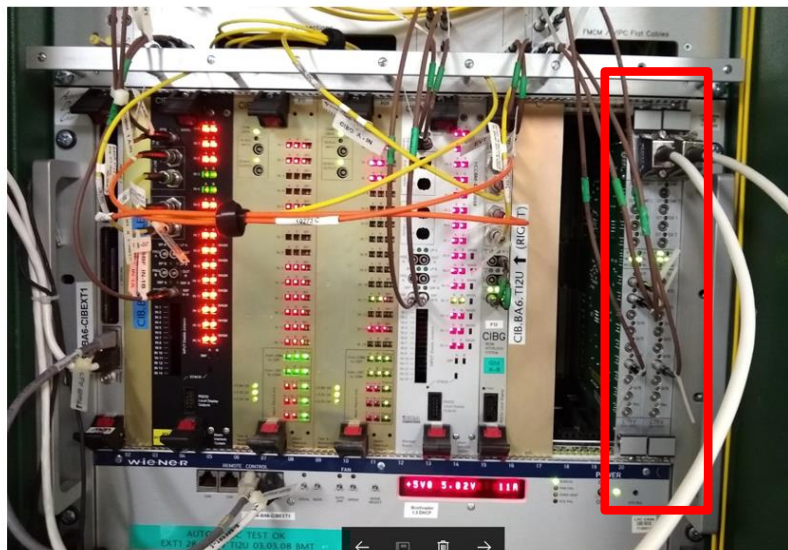
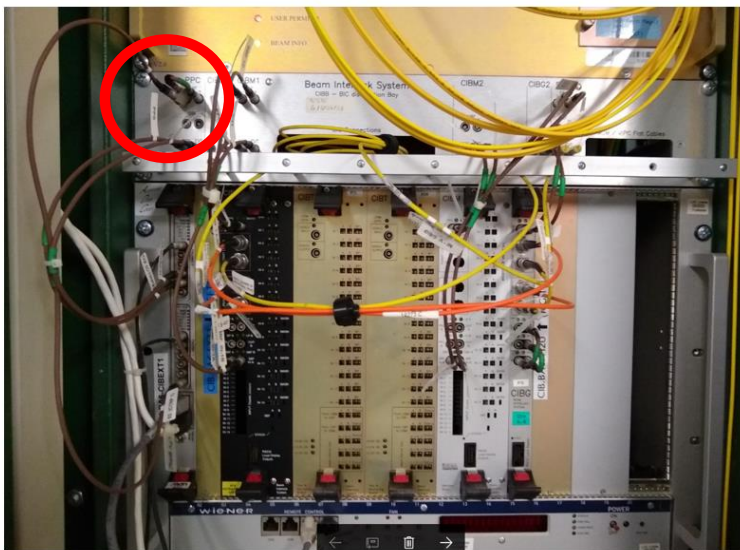
**Commissioning already performed**

(Jan/Feb 2021)

The screenshot displays the 'Safe Machine Parameters in CCC: Detailed Overview' interface. On the left, a 'Device Tree' shows the hierarchy: SMPC > SPS (RA, RB, GA, GB, A) > LHC (RA, RB, GA, GB, A, C) > CISV > BIC > CCR.CIB.1. Below the tree are sections for 'Board Info' (Board Name, Variant Name, Slot Number), 'Monitor FPGA Info' (Version, Revision, ISE Version, Percent used, UTC), and 'Control FPGA Info' (Version, ISE Version, Percent used, UTC). The main area shows a logic diagram with three main sections: 'From Sources', 'Generation', and 'To Arbiter & Extraction BIS'. 'From Sources' includes BCT4/40S Intensity A and B (2.3E9 [p]), BCT3/30S Intensity A (0.0E0 [p]), BCT5/50S Intensity B (0.0E0 [p]), BEM4 Energy Link A, B, M6, and M6 (0.000, 0.000, 0.008, 0.008 GeV). 'Generation' includes a '1 out of 2: Select A then B' block leading to BCT4/40S Intensity (2.3E9 [p]), an 'Operator Probe Beam Limit' (0.0E0 [p]), and another '1 out of 2: Select A then B' block leading to BCT3/30S Intensity (0.0E0 [p]). 'To Arbiter & Extraction BIS' includes a '1 out of 4: Select BEM4 A then BEM4 B then BEM6 A then BEM6 B' block leading to Machine Energy (0.000 GeV), and a table of energy limits: AWAKE (397.440 GeV to 402.600 GeV), HiRadMat (437.400 GeV to 442.560 GeV), and LHC (448.440 GeV to 453.600 GeV). Status flags on the right include SPS Probe Beam Flag (FALSE), SPS Setup Beam Flag (TRUE), TED Beam Flag (TRUE), Energy AWAKE (FALSE), Energy HiRadMat (FALSE), and Energy LHC (FALSE).



# Extraction BIS Timing configuration



- SMP-SPS Setup Beam Flag: changed **BIS Extraction Timing Configuration** (BA4 and BA6)
- Removed a **GMT filter** acting on SMP-SPS frames. Presented at [189th MPP](#)
- Tests carried out on BIS timing configuration and compatibility with recent BE-CO updates. SPS extraction and LHC Injection BIS (8x BIS systems timing reconfigured)

## SPS Extraction BIS:

cfv-ba4-cibext2

cfv-ba6-cibext1

## BIS Transfer Lines:

cfv-ba4-cibtt40

cfv-ba4-cibtt41

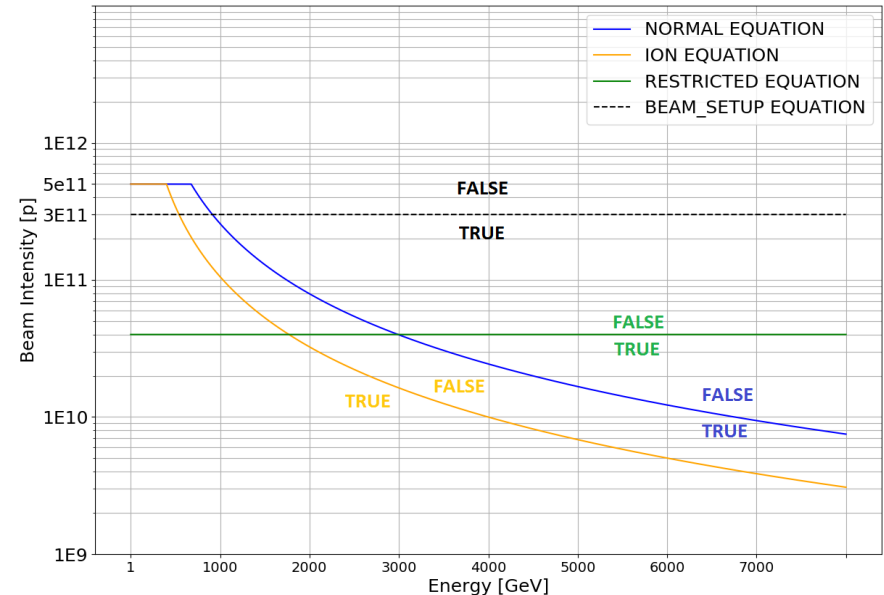
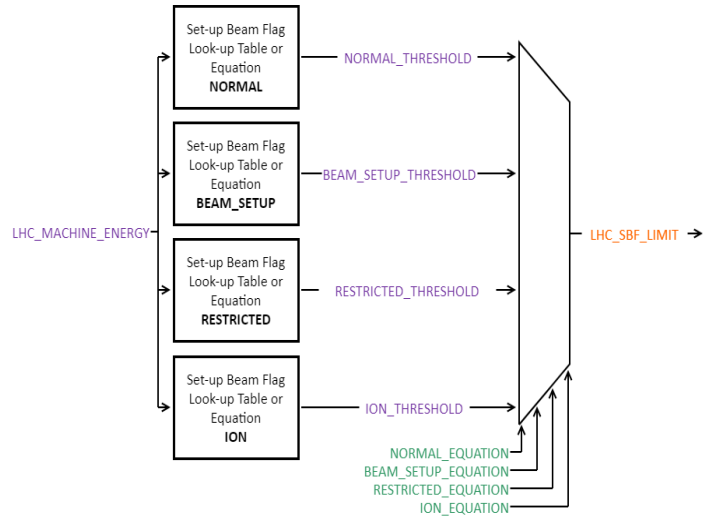
cfv-ba6-cibtt60

cfv-ba6-cibtt66

cfv-sr2-cibti2

cfv-sr8-cibti8

# SMP-LHC Setup Beam Flag – RESTRICTED EQUATION



- AC-dipole operation with 3 bunches (under certain conditions).
- Proposal of **New SBF Equation generated by SMP-LHC**. Presented at [191<sup>st</sup> MPP](#)
- **BEAM\_RESTRICTED** threshold to be changed to 4e10 p

# SMP-LHC Commissioning - I

## Validate Sources connections

- DCBCT
- BETS
- BPM
- Sequencer
- SIS

## Validate Transmission

- GMT network connection
- Beam Presence Flag direct transmission
- Setup Beam Flag direct transmission
- Cross-Checker User Permit (connection to BIS)
- SMP-LHC GMT frames validation
- ~40x CISV correct decoding
- LHC-SBF correctly received
- LHC Cross-Checker

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## Machine Checkout tests (OP):

- LHC Energy
- LHC SBF
- Squeezing Factors
- MDI and STB

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## Tests with Beam (OP):

- Check **SBF** value through all 4 SBF Equations
- Check SPS **SBF** and **PBF** are correctly evaluated by Extraction BIS

# SMP-LHC Commissioning - II

- New **SMP firmware versions** for SMP-SPS and SMP-LHC:
  - SMP LHC New BEAM RESTRICTED SBF
  - SMP SPS TED Flags and Beam Intensity majority voters updated
- SMP functional specifications updated and validated: [LHC-CI-ES-0005 v.3.3](#)
- SMP MPS document [1112187 v.1.0](#):
  - No change to SMP-LHC, updates on SBF/TBF/PBF being added for **SMP-SPS** (to be validated and circulated)
    - **SMP-LHC commissioning** foreseen for **beginning of September**.
    - **Duration: 2-3 days minimum** (test sources and transmission)
    - Tests **are not to be repeated** for Jan. 2022, unless **changes impacting on sources/users**.
    - For SMP-LHC commissioning, list of systems to be ready:
      - BETS
      - BCT
      - BPM
      - BEMs
      - Sequencer and SIS
      - LHC Ring BIS + Extraction and Injection BIS powered on
      - All CISV crates powered on
      - SMP GUI
      - Timing Network

# Outline

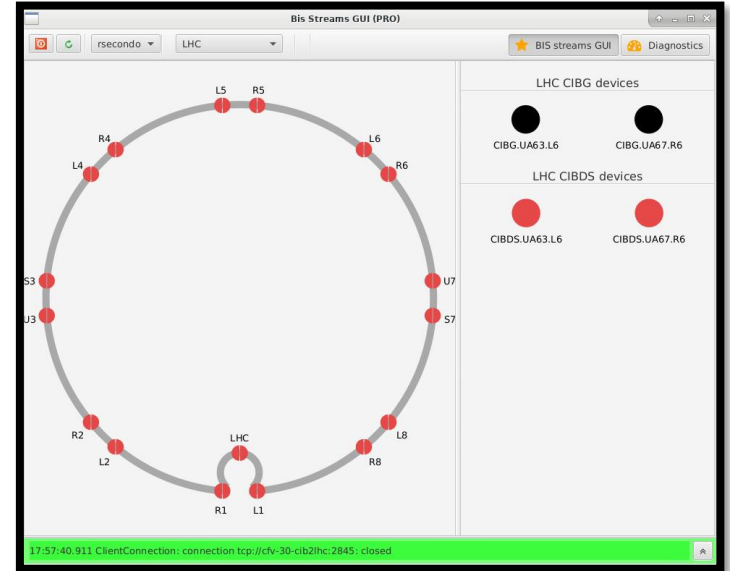
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## LHC BIS hardware modifications:

- CCR BIC, add two new connections on **CIBV** to provide Post Mortem signal to BI (Beam Dumped event)
- **No new** LHC CIBU User connections
- User interface (CIBU) **displacement**:
  - LHCb VELO, move CIBU from rack C3B03 to rack D3E01. Foreseen May 2021
  - **BPMs** point 6: evaluate new system in “test mode” (YETS 2021)
    - BPMs connected on a BIS disabled input, only for monitoring
  - **BPMs** point 6, move 4 CIBUs from SRs to UAs (2022?) after validation of the new BPMs Electronics

# LHC BIS SOFTWARE MODIFICATIONS

- All FECs upgraded to CC7 and FESA classes migrated to FESA3
- New JavaFX-based BIS GUI
- **COSMOS** checks for diagnostics as replacement to **DIAMON** (new BIS Grafana dashboards)



# Beam Interlock System end of LS2 - KEY DATES

LHC- BIS **current status**: BIS Local Loops in UA63 and UA67 are in place since January 2021

- All Users **must power** the CIBUs in their racks by **end of May**
  - CIBUs can be remotely set in test mode only if they are powered
  - After **end of May** → **Users must ensure that racks hosting CIBUs remain powered**
- During **June**, the BIS LHC optical fibres will be **checked** and **cleaned**
  - Measure fibre attenuation, power margin from BIC to BIC
  - Outside of BIS procedure but essential for BIS availability
  - 5 days duration if we have full access to all LHC BICs crates located in the UAs

## Prerequisite for these tests :

- All CIBUs must be powered
- BIS controls must be available (FESA, GUI ...)
- The BIS Local Loop will stay in place, no need for ABT systems
  - The optical fibres between the BIC and the TSU will be tested later



- **End of June:** Beginning of the BIS **IST** tests EDMS [1513541](#)
  - The BIS Loop must be closed in **Test Mode** (A or B)
  - Duration: **~10 days** (with start date flexible)
    - Tests performed remotely and/or from the CCC, **no need to access the LHC machine**, there is **no interaction with the other LHC equipment**
    - Tests to validate the “internal” behaviour of the BIS without any external systems connected on it (no Users and no actuators)

Prerequisite for these tests:

- Same as for previous test (Local Loop stays in place)
  - Timing and network connections functional on each crate
- 
- **IST-BIS (1):** Tests the **BICs** in **stand alone mode**: access all boards, History buffer integrity...
  - **IST-BIS (2):** Verify **users interface**: communication CIBM / CIBUs, CIBM enable channels ...
  - **IST-BIS (3):** Close the **optical loops**. Close the loop in test mode (A or B), verify that **each BIC can open the loop**

- **September 2021:** beginning of the MPS BIS tests EDMS [889281](#)
  - The BIS loops **must be closed**
  - **Duration: ~10 days.** These tests must be performed just before LHC operation.
  - *Tests performed from the CCC, no need to access the LHC, full dependencies with the others LHC equipment (Users, LBDS)*
  - These tests are intended to validate the “connection” of the BIS with the external systems

## Prerequisite to these tests:

- Same as for previous test plus
  - BIS Local Loop removed
  - All the CIBU Users must be ready for operation (user electronics operational)
  - All the ABT systems must be ready (TSU ready)
- *Within the MPS test document it is notified that the Users have to provide User permit A & B independently during these tests (to check the redundancy).*
- *Currently for the LHC, 54 over 147 Users cannot set A & B independently → Not possible to verify the redundancy*

# MPS Test details - I

- **MPS Test A:** Test links from User systems to BIS
  - In the procedure it is notified that only Users with **automated tests** features are to be verified, for the others there is no check in place

## Users with automatic test method

System Name	Connections(*)	Automatic test mode
Collimators	36	Yes
Powering Interlock Controllers	32	Yes
Vacuum	30	Yes
Beam Loss Monitor System	16	Yes
Fast Magnet Current Change Monitor	12	Yes
Warm Magnet Interlocks	8	Yes

**70 %** of the LHC BIS Users are able to perform an **automatic test**

*Note: The equipment owner or the CCC operators are responsible of the procedure and the execution of these tests*

# MPS Test details - II

System Name	Connections(*)	Automatic test mode
Beam Screens (BTV)	9	No
Kicker Systems (LBDS & MKI)	6	No
TCDQ & BETS-TCDQ	5	No
RF	4	No
ATLAS	6	No
CMS & TOTEM	4	No
ALICE	2	No
<u>LHCb</u>	3	No
BCCM (Beam Lifetime)	2	No
BPM (Beam Excursion)	4	No
Access System	4	No
Operator Push-Buttons	2	No
Programmed Dump	2	No
CIBDS	2	No
Crystal collimator (UA9 experiment)	1	No

## Users without automatic test method

- For these Users, there is no systematic tests performed. The tests can be performed User by User **on demand**. (Acceptable?)

### Note:

- These tests are “**functional tests**”, different from the **CIBU Hardware Tests**
- If a user system is **modified**, the **BIS team must be always informed** in order to perform a **new commissioning test (this is not optional)**

# MPS Test details - III

- **MPS Test B:** Tests links from **Software Interlock System** to BIS
  - The SIS must be operational and must provide permits A & B TRUE to the BIS
- **MPS Test C:** Test **Setup Beam Flag** transmission through GMT
  - The SMP system and the timing system must be operational
- **MPS Test D:** Test links from BIS to **Beam Dump**
  - The LBDS must be ready and ABT system expert must be present in CCC during this test
- **MPS Test E:** Test links from BIS to **Injection Interlock System**
  - *The injection BIS must be ready*

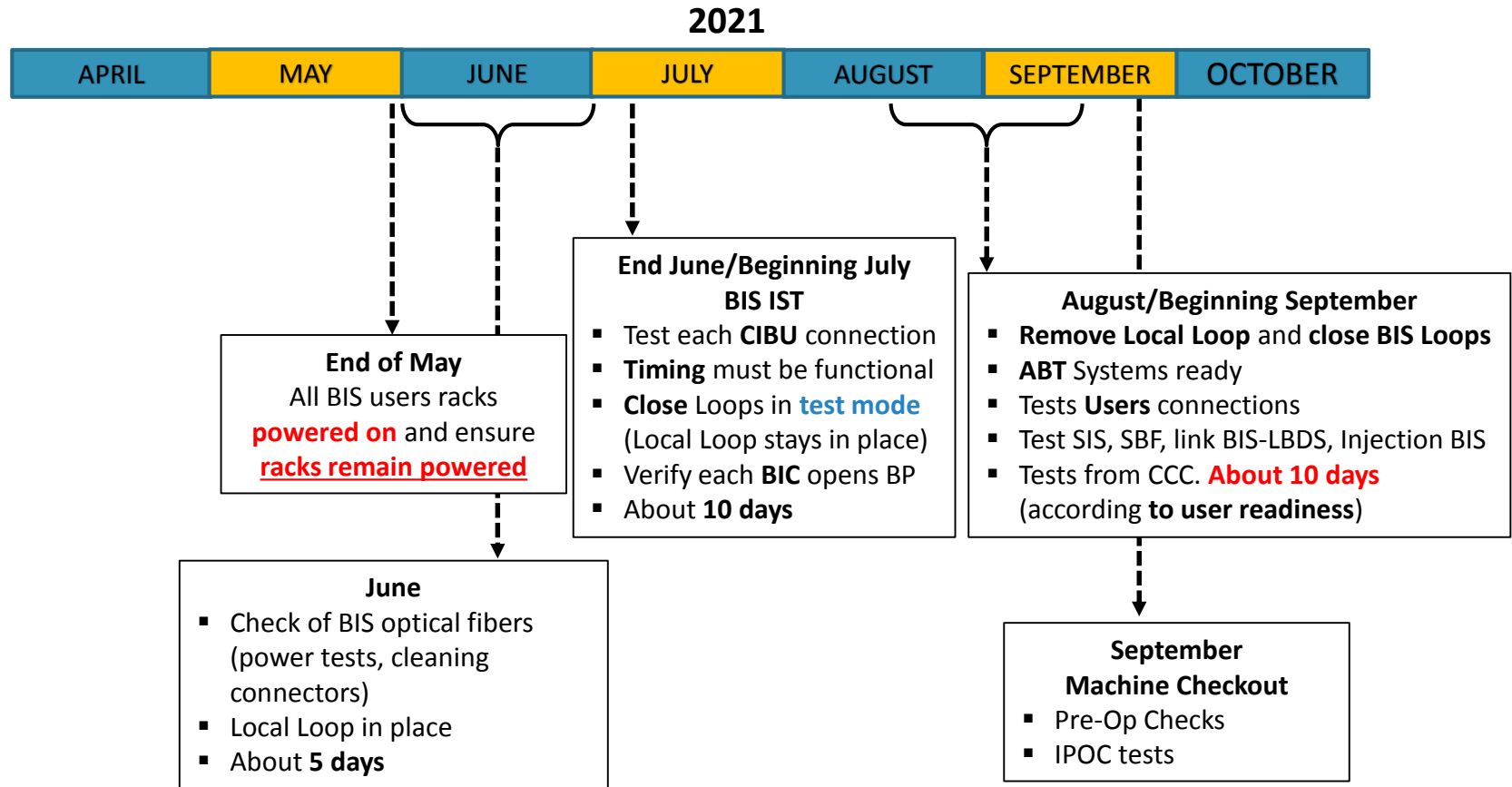
*Note: If these tests cannot be performed for any reason (all users must be ready, LBDS ready, software available, LHC UPS ready ...) → A **delay** must be added to the **~10 days** required to perform these tests.*

- **Duration: ½ day**
  - Tests that must be performed just before **pilot** beam
- Execute the BIS **Pre-operational Checks** → No error must be received
- Provoke a **Dump event** and check BIS **IPOC** → Results must be coherent

- **LMC 3<sup>rd</sup> February 2021:**
  - “Go back to Local BIS and continue collecting statistics until final cold check-out in spring 2022”
  - Half day to set-up the local BIS loop (Access in UA 63 & 67)
- To return to the normal loop (January 2022?) the following BIS tests must be repeated:
  - **Partial BIS MPS tests (~5 days)** → depends on what was “touched” between September 21<sup>st</sup> and first beam.
  - Machine Checkout tests (half day)

*Note: In any case (with or without Local Loop after September pilot beam) we have to re-validate some of the MPS tests and Checkout Tests*

# Summary of BIS Commissioning Timeline 2021









# Beam Beam Compensation Wire

The BBCW are powered by **LHC type  $\pm 600A / \pm 40V$**  power converters.

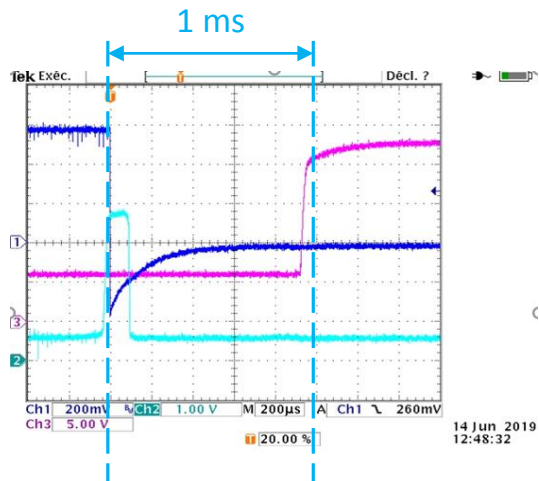
There was a concern whether the response time of the **FGC2** control to process an internal fault and propagate it to the WIC was fast enough ?

Together with L. Ceccone (TE-EPC), we measured this delay accurately using an oscilloscope: **< 1 ms**

**Endorsed by MPP: [177th MPP](#)**

## **Status today:**

- HW and SW modifications completed
- Ready for IST



Test set-up in bldg. 180 (FAIR)

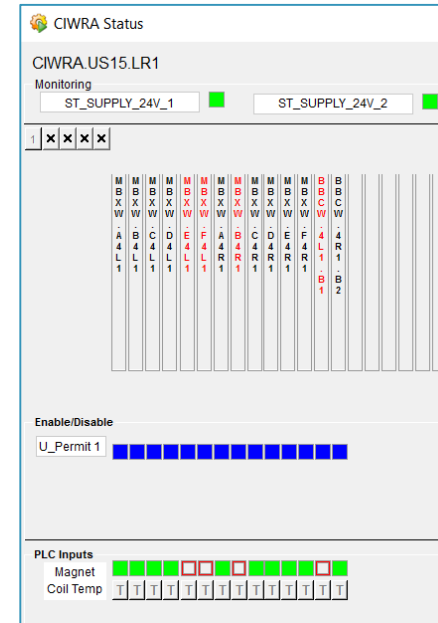
# WIC Supervision

New generic Magnet and PC widgets with additional information:

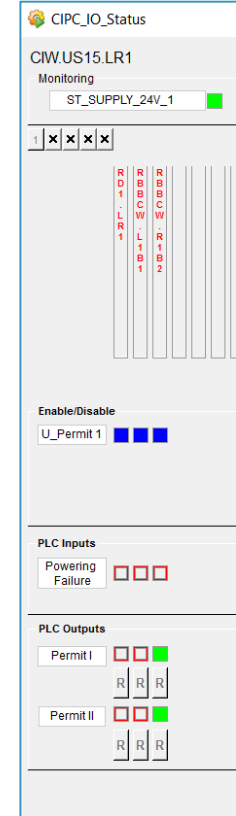
- To know which magnet or PC is associated to **which** «User\_Permit» (in case of multiple outputs) →
- To know which magnet or PC is **Active / Inactive** in the calculation of the signal sent to the BIS

Solid **blue** square = **Active**

Empty **blue** square = **Inactive**



Magnet widget  
in IR1



PC widget  
In IR1