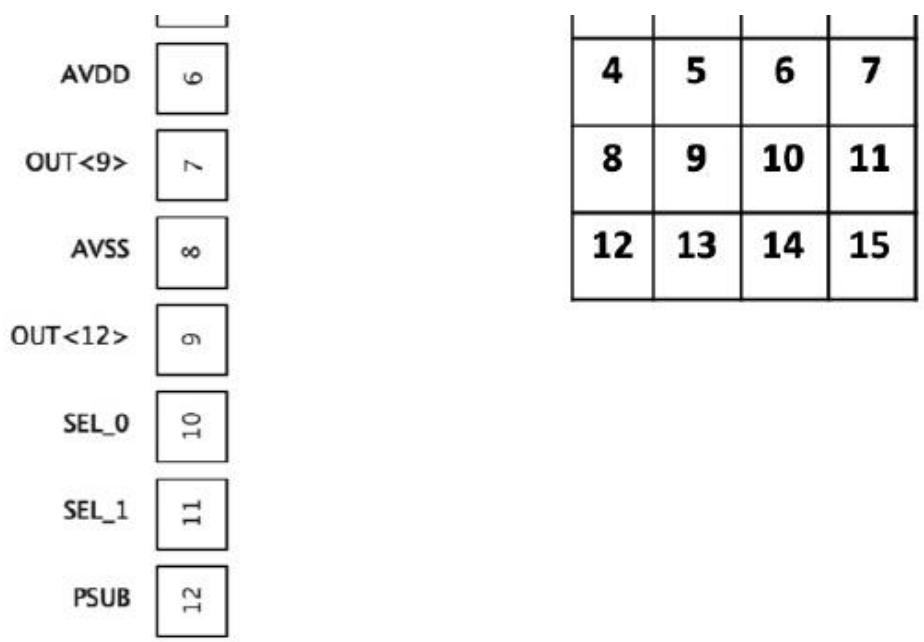
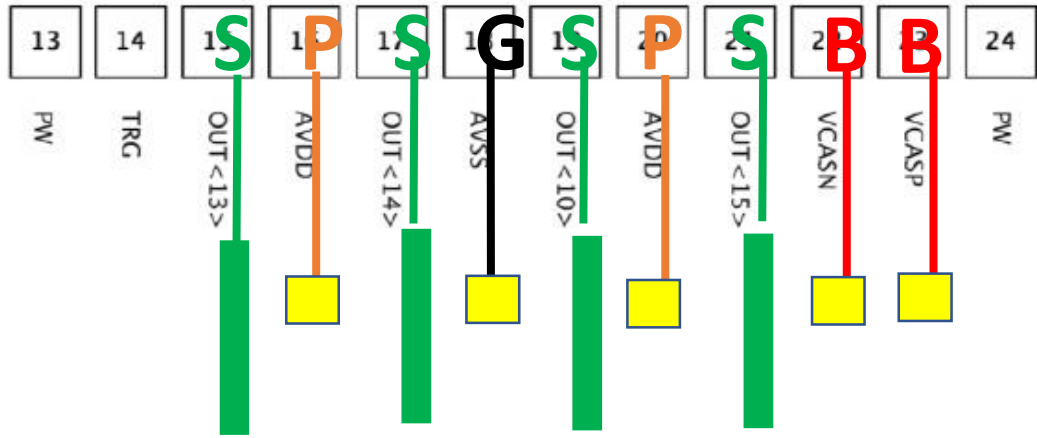
APTS carrier (OPAMP version)

Wirebond diagram





Vias

SIGNAL	1st plane, signal traces
Ground	2nd plane, GND
POWER	3rd plane, POWER
SIGNAL/GND	4th plane, BIAS or ground

50 Ohm matching. Shortest wirebond possible

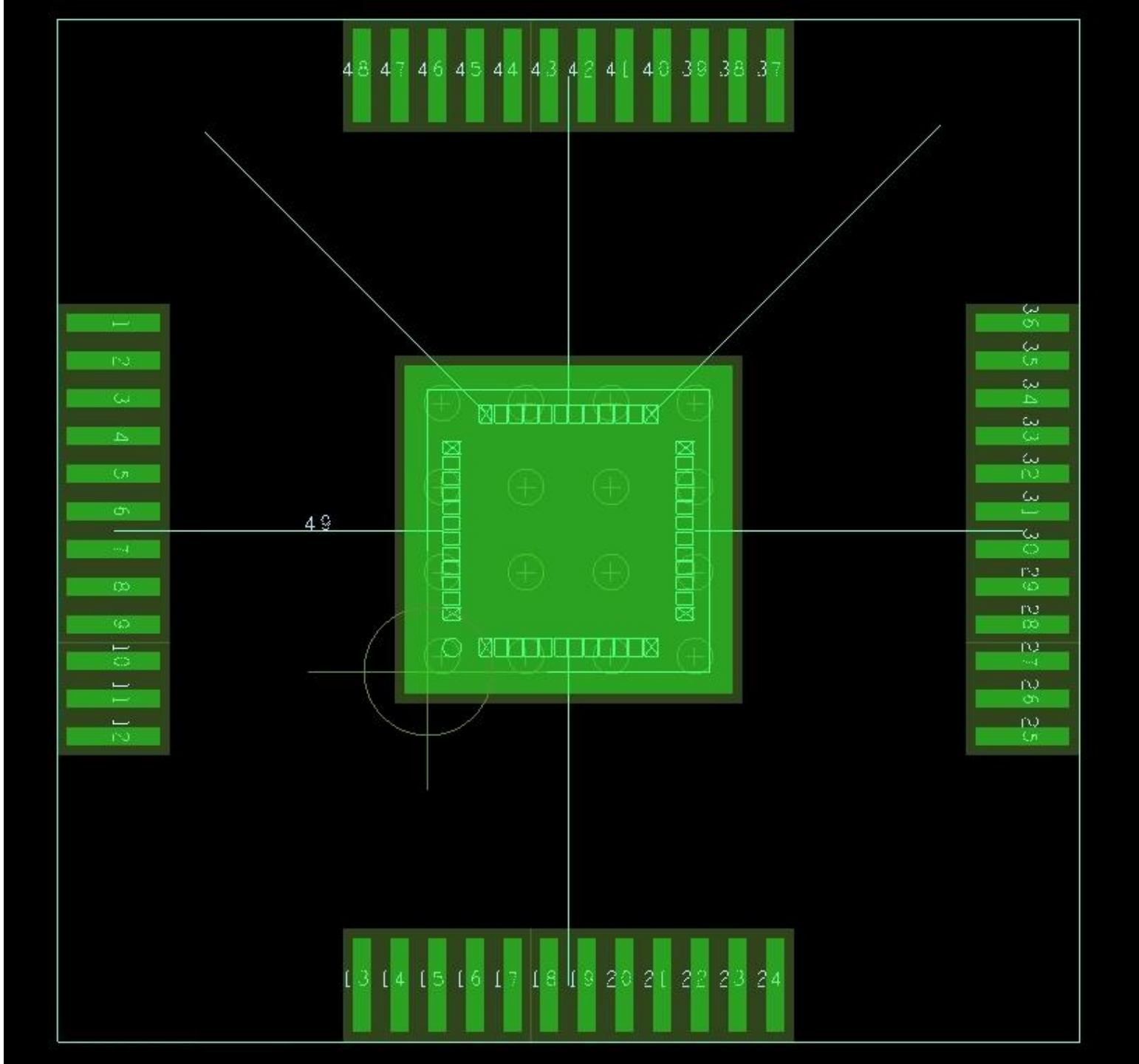
MLR1_APTS Footprint

Torino Ver 1.1 (2.03.2021)

- Bonding pad dimensions: 100x500 µm

- Bond lenght (min) ≈ 1,8mm
- Chip height = 500 µm ?
- Bond lenght, estimated: 2.5mm

- MINIMUM possible distance between the pad centers= 1.5mm



LAYOUT SKETCH

BOARD DIMENSIONS: ~6x6 cm2

CONNECTION TO PROXIMITY: PCI EXPRESS 98 pins

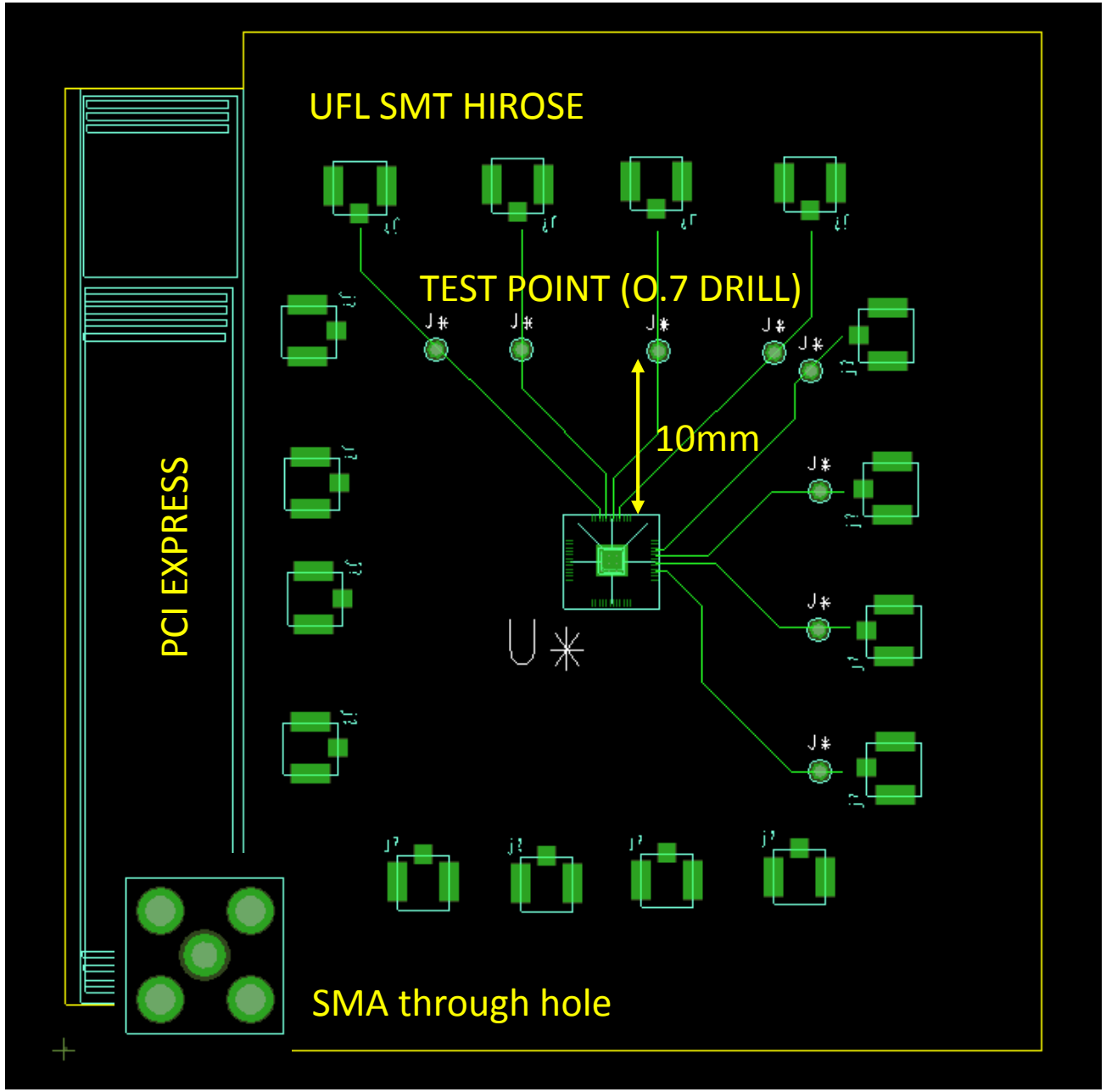
TEST POINTS?

CONNECTORS: UFL HIROSE

4x4mm2

SMA SMT

7x7mm2



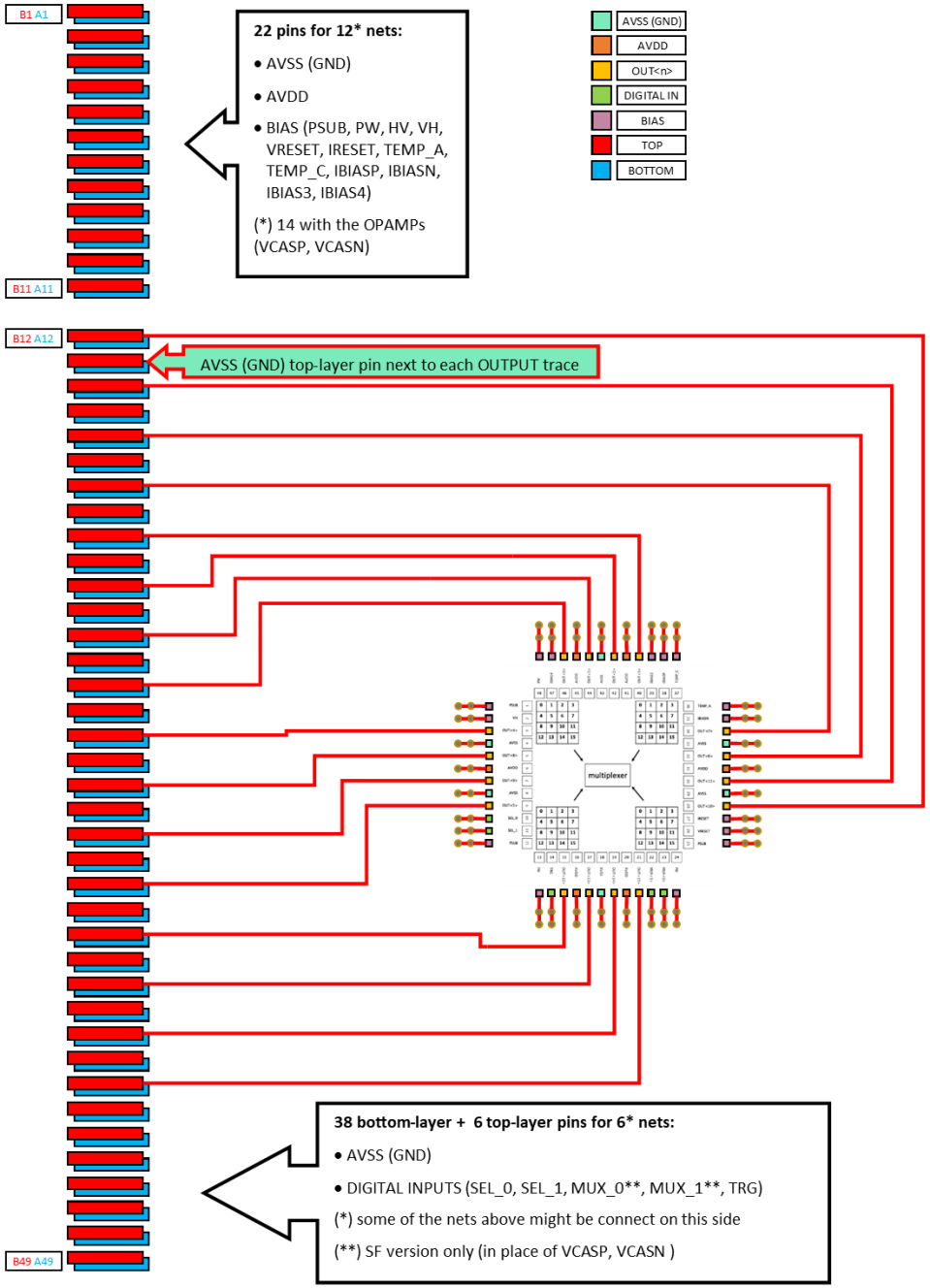
Comparing table for bias requirements

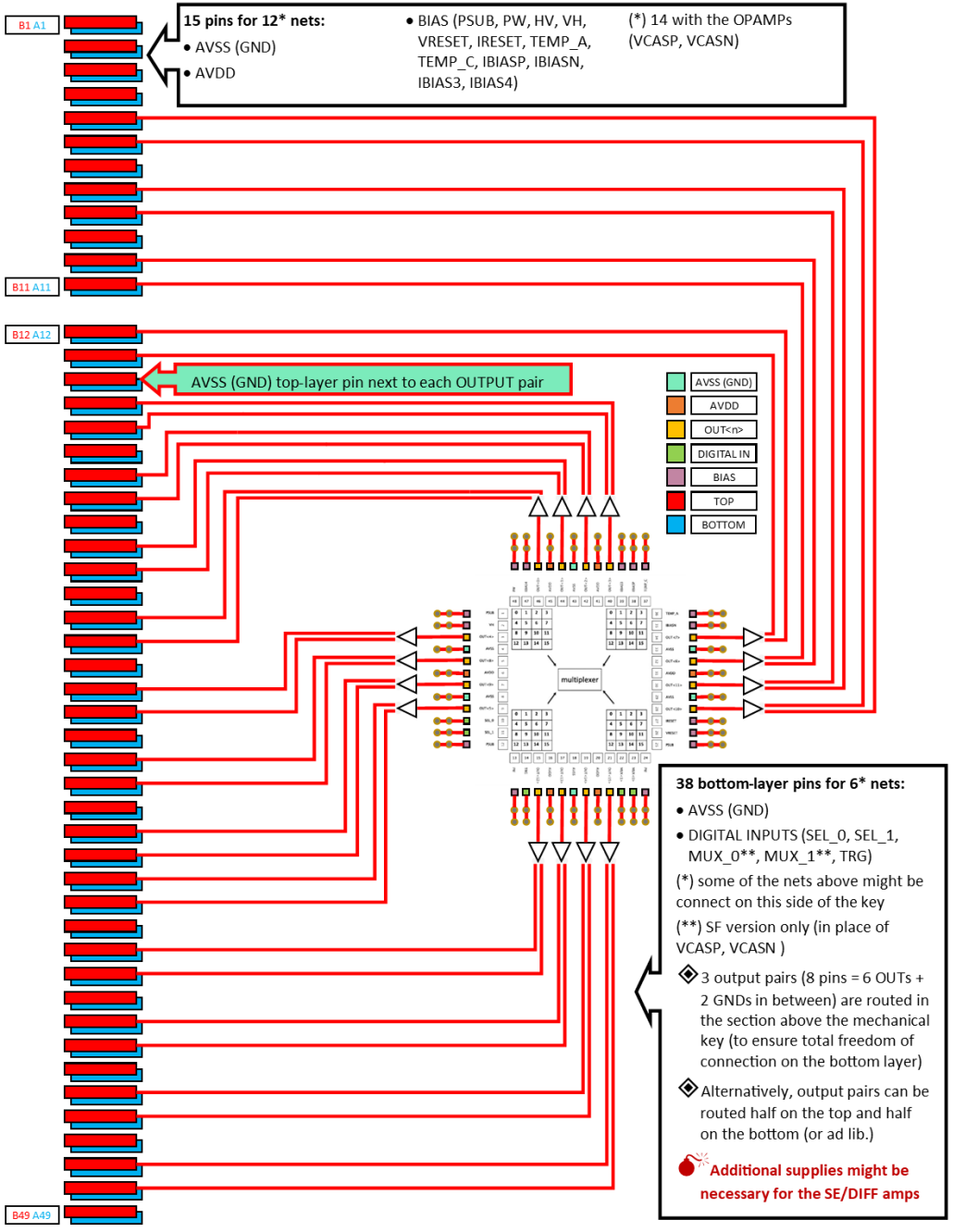
APTS	APTS	DPTS	CE65
OPAMP Version	SOURCE FOLLOWER Version		
VBIAS: (tot:3)	**VBIAS: (tot:1)**	**VBIAS: (tot:2)**	**VBIAS: (tot:1)**
VRESET (200 mV)	VRESET (200 mV)	VCASN (300 mV)	VRESET (1V; ?)
VCASN (750 mV)		VCASB (300mV)	
VCASP (300mV)			
IBIAS: (5)	**IBIAS: (5)**	**IBIAS: (4)**	**IBIAS: (6)**
IBIASN (-800 µA)	IBIASN (-800 µA)	IBIASN (+1 µA; 1:1000µA)	BIAS_SF_MAT (1mA; 0:10mA)
IBIASP (+80 µA)	IBIASP (+80 µA)	IBIAS (+1 µA; 1:500µA)	BIAS_SF_COL (100 µA; 0:1mA)
IRESET (+1 µA)	IRESET (+1 µA)	IRESET (+1 µA; 1:100µA)	BIAS_SF_NMOS_PIX (1 µA; 0:10µA)
IBIAS3 (+800 µA)	IBIAS3 (+800 µA)	IDB (+10 µA; 1:500µA)	BIAS_SF_PMOS_PIX (-1 µA; 0:10µA)
IBIAS4 (+2,5mA)	IBIAS4 (-6mA)		DAC_IBIAS_A (0,8 µA; 20xLSB)
Positive Current (+) from pin to gnd on board			DAC_IBIAS_B (10,72 µA; 268xLSB)

APTS carrier (SF version)

Things get trickier…

Possible layouts: single ended vs differential





Open points for both versions (page 1/2)

LAYOUT

- SF: NO impedance matching [discuss with chip designers]
- SF: priority to trace shielding wrt capacitance reduction [discuss with chip designers]
- OA: 50-Ω matching (?) [discuss with chip designers]
- OA: pad or connector for oscilloscope (?) [discuss with chip designers]
- SF: equalise output-trace lengths (?) [discuss with chip designers]
- SF: reduce trace length AMAP [of course]
- Central pad to GND (?) [discuss with chip designers]
- OA: PW/HV (pins 13, 24, 48) double function (?) [discuss with chip designers]
- SF: PW (pins 13, 24, 48) single function (?) [discuss with chip designers]
- Are VH pulses fast (?) [discuss with chip designers]
- Is TRG speed-critical / does it need to be matched or terminated (?) [discuss with chip designers]
- Are the other digital signals (SEL and MUX) slow (?) [discuss with chip designers]
- Is VRESET stationary (?) [discuss with chip designers]
- SF: 16 single-ended or 32 differential output traces (?) [discuss with chip designers]
- SF: 16 traces (or diff. pairs) or MUX on carrier board (?) [discuss with proximity-board designers]
- Board size constraints (e.g. chip-connector distance…) (?) [discuss with proximity- and OA-board designers]

Open points for both versions (page 2/2)

LAYERS

- 4 layers (TOP/GND/POW/BOTTOM?) [discuss with proximity- and OA-board designers]
- Materials, thickness (1,6 mm for PCIe), tech. constraints (?) [discuss with proximity- and OA-board designers]
- Buried or top-layer signal traces (?) [discuss with proximity- and OA-board designers]

COMPONENTS:

- Are bypass capacitors necessary on carrier board (?) [discuss with chip designers]
- If so, of which value (?) [discuss with chip designers]
- Other passive components (resistors, diodes, jumper...) (?) [discuss with chip designers]
- Voltage regulators needed on carrier board (?) [discuss with proximity-board designers]
- Other active components (buffer, SE/DIFF…) (?) [discuss with chip designers]

CONNECTIONS:

- With proximity board (TBD), Edge Card type (?) [Probably a PCIe]
- 50-V (lemo?) connector [on Proximity or DAQ board]
- Allow for huge-curved-chip connection (?) [discuss with OA-board and HCC designers]
- Bias levels and quantity, DAC resolution on proximity (CE65 version) compatible with APTS (and possibly DPTS) (?) [discuss with proximity-board and chip designers]