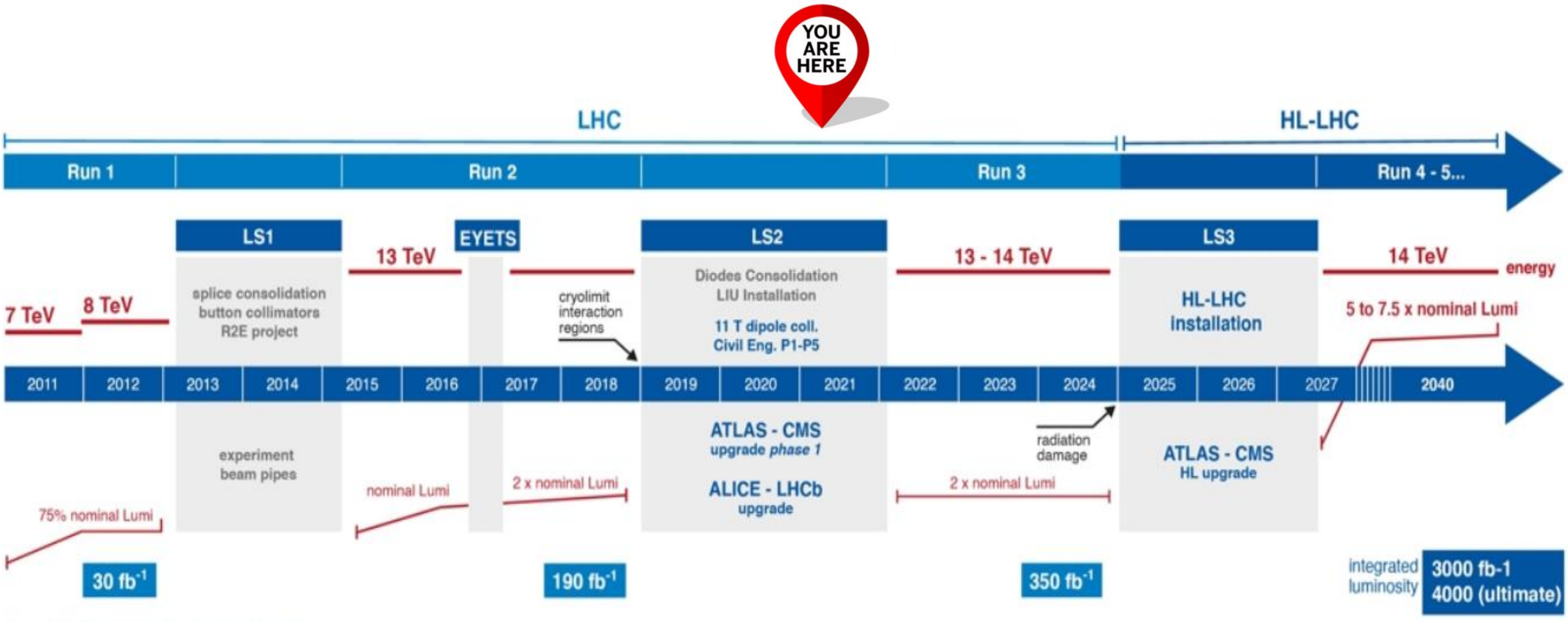
Steve McMahon
RAL/Oxford

Upgrades at the LHC

IOP meeting – Monday 12.04.2021

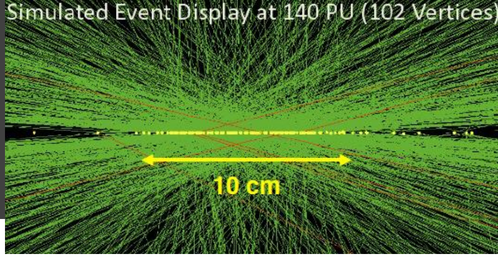
Acknowledge helpful discussions with A. Tapper, F. Wilson, A. Papanestis, M. Chartier, R. Lemmon, S. George

Introduction: timelines and energies (2011:2040)



Note this schedule is updated to the latest version of LS2 – There are other schedules that sit on top of this and I will get to them
I am mainly going to concentrate on MAJOR upgrades that are happening NOW – and looking forward

Some of the challenges in the HL-LHC era



In particular for the GPDs:

Instantaneous luminosities of **$L = 5.0 \times 10^{34}$ cm^{-2} s^{-1}** (Ultimate **$L = 7.5 \times 10^{34}$ cm^{-2} s^{-1}**)

Number of p-p interactions per bunch crossing: **$\langle\mu\rangle = 200$** (around 50-60 in Phase I)

Integrated luminosities of **$L = 3{,}000$ fb^{-1}** (Ultimate integrated **$L = 4{,}000$ fb^{-1}**)

Extreme radiation tolerance requirements: (fluences at small radius up to 2×10^{16} n_{eq} /cm^{-2})

Target Performance that is at least as good as, and if not better than, the LHC (run-2) operation.

For everyone:

driven to low power on detector, small feature sizes, development of new ASICs, novel powering (DC-DC or SP), new ways of delivering services.. end of life issues

Unprecidented requirements on cooling (few x 10^{2} of kW of FE cooling power required for trackers (drives to $C0_2$))

Decommissioning, in-situ replacements, Components ~20+ years old by 2025, approaching radiation lifetime

High Trigger rates, large data volumes, readout complexity, pattern recognition complexity, NEW timing detectors

Multiple challenges in areas of: reconstruction, simulations & efficient physics object reconstruction

Computer architectures are changing

- Multi cores, low memory/core
- Existing software approach do not scale to meet requirements….New framework & algorithms/codes needed
- Efficiently utilization of computing resources

Strategies of UK groups in HL-LHC era

Consolidate and expand on experiences gained in original constructions and operation of original LHC experiments
Expand into new applications of “established” technologies: strips → pixels, CPU → GPU
Consolidate/improve areas like: mechanics/cooling/powering/radiation tolerance
Open up new areas of investigation: monolithic CMOS detectors, LGADs for timing, new paradigm in calorimetry
Start to think about to use these technologies in the next generation of upgrades, detectors and spin-offs

Consolidate software (and firmware) as a critical ingredient of physics exploitation (but hard to show photographs of)
Includes: simulation, reconstruction, optimized detector performance, physics exploitation

Run the experiments, maintain the existing detectors
Maintain UK leadership at a time when funds are tight
Funding agencies increasingly have their own set of goals that are “parallel” to our own

CMS Phase-II Upgrades

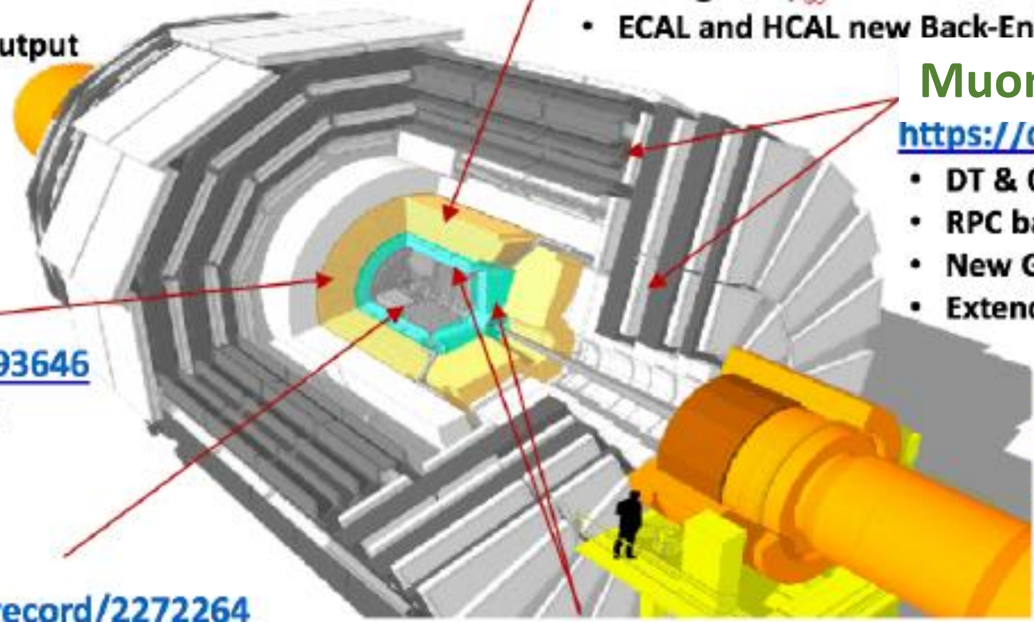
Technical proposal CERN-LHCC-2015-010 https://cds.cern.ch/record/2020886
Scope Document CERN-LHCC-2015-019 https://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf

Replacement

L1-Trigger/HLT/DAQ
https://cds.cern.ch/record/2283192
https://cds.cern.ch/record/2283193
- Tracks in L1-Trigger at 40 MHz
- PFlow-like selection 750 kHz output
- HLT output 7.5 kHz

Calorimeter EndCap
https://cds.cern.ch/record/2293646
- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS

Tracker
https://cds.cern.ch/record/2272264
- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \simeq 3.8$



Upgrade / Consolidation Electronics

Barrel Calorimeters
https://cds.cern.ch/record/2283187
- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon Systems
https://cds.cern.ch/record/2283189
- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \simeq 3$

New Detector Systems

Beam Radiation Instr. and Luminosity, and Common Systems and Infrastructure
https://cds.cern.ch/record/2020886

MIP Timing Detector
https://cds.cern.ch/record/2296612

Precision timing with:
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

CMS Phase-II Upgrades

UK Involvement

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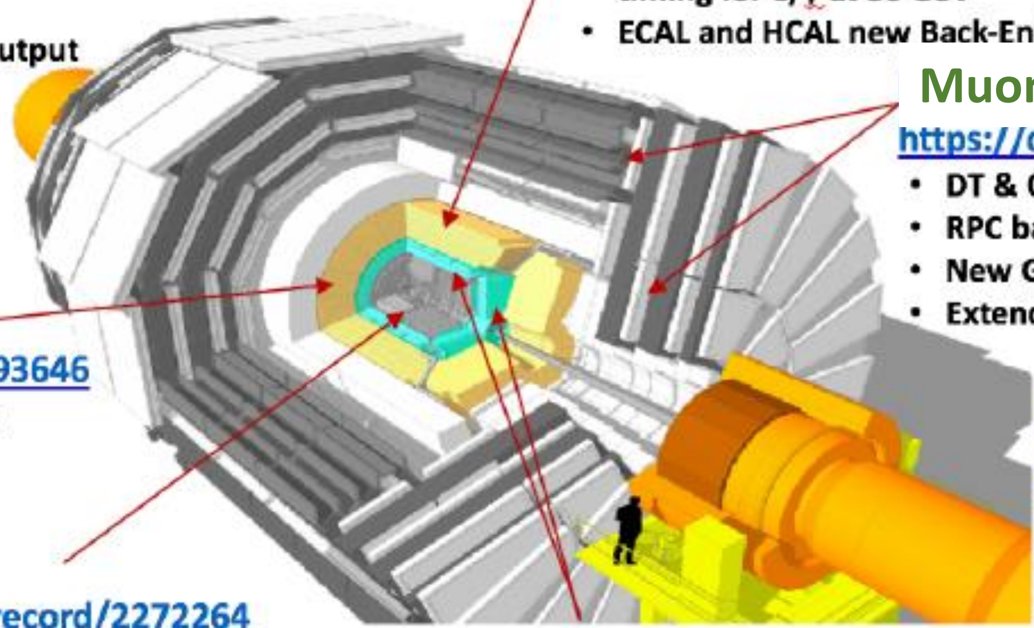

Upgrade / Consolidation

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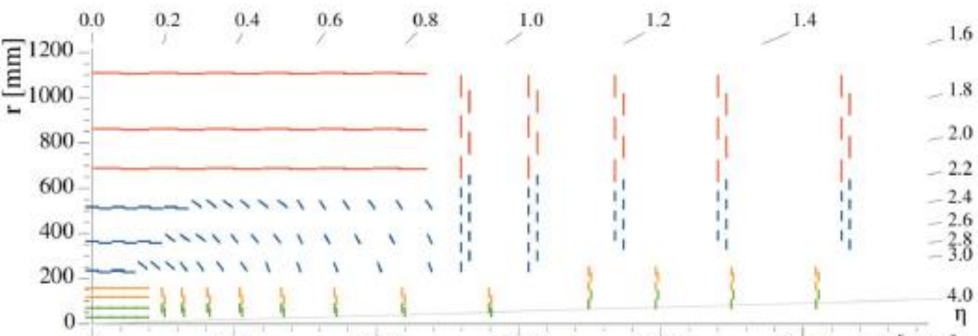
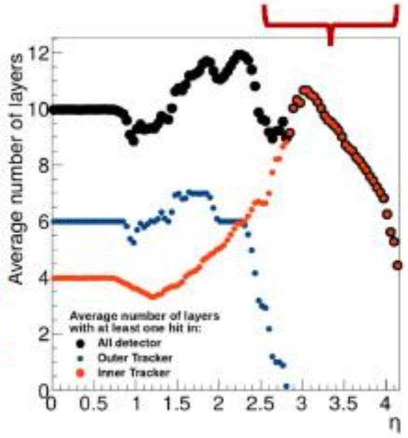
CMS Upgrades – All new Silicon Tracker



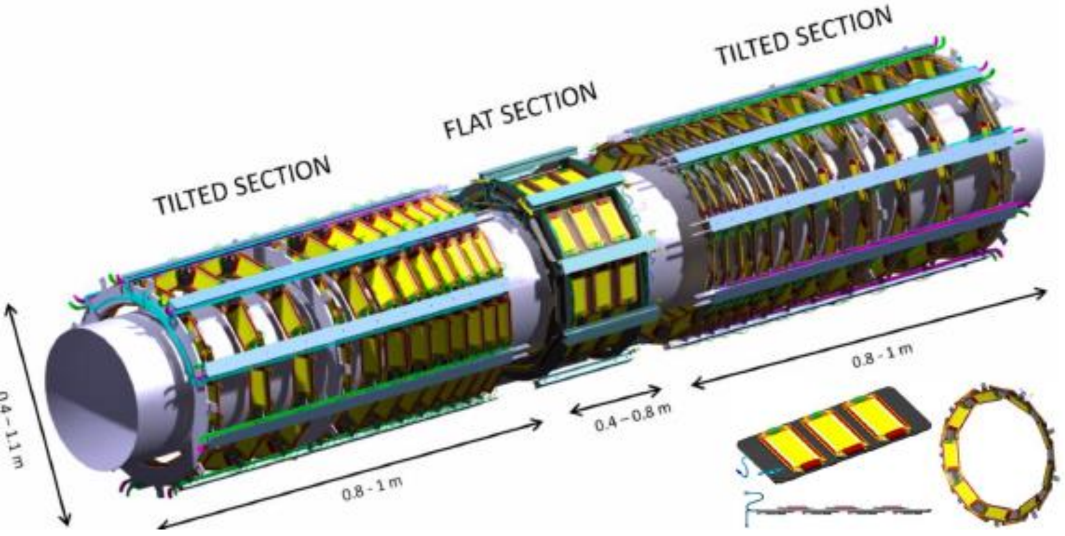
Extended solid angle coverage

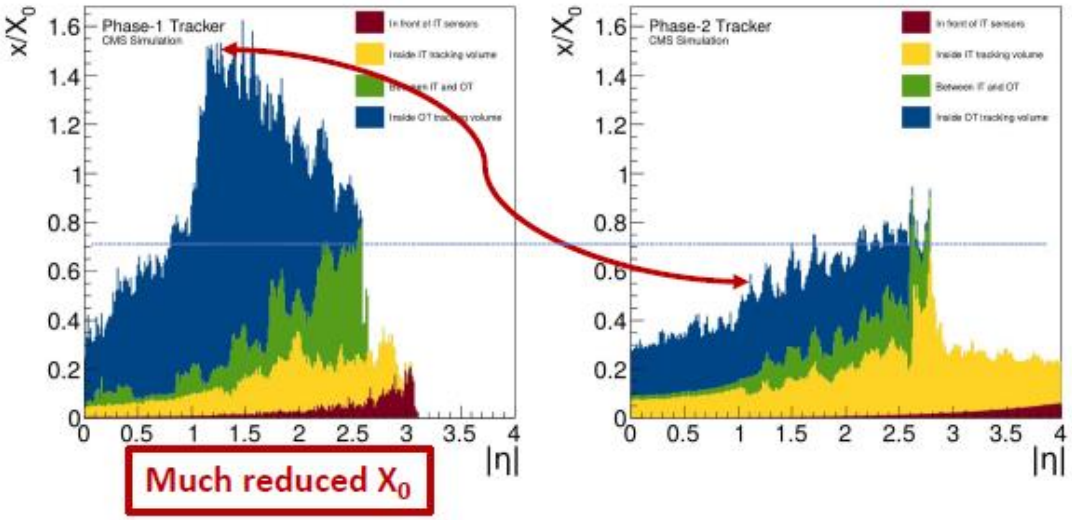


All new Tracker

Pixels and Silicon Strips

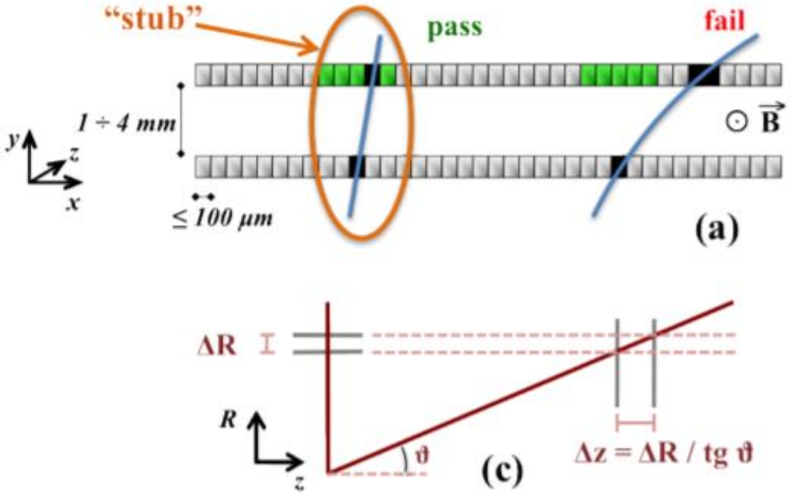
- 200m^2 if silicon
- ~10^9 channels
- 100μm strips
- Outer strips used in L1 trigger
- Tracker provides full tracks to L1 trigger

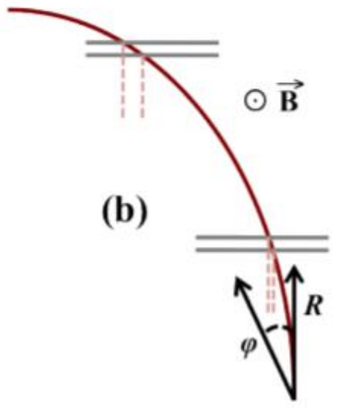


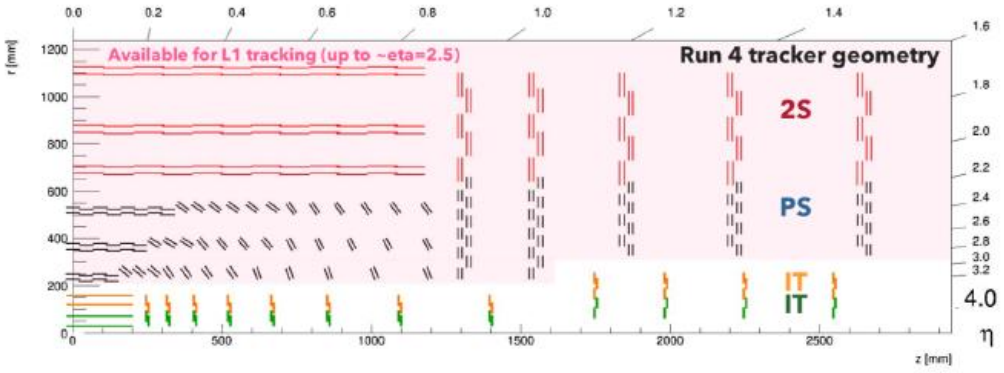


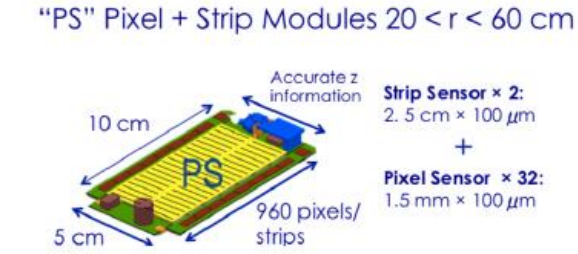
CMS Upgrades – Tracker & Track Triggering

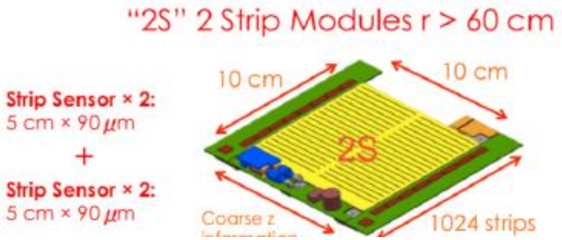
Hardware Track Triggering is an integral part of the tracker design











CBC – 254 channels @320MHz readout in 130nm, latency 12.8μs, development complete and wafers being received

P_T module – doublet of sensors connected to common electronics that can correlate digitizations between adjacent layers.
Distance between layers defines lower P_T cut
Data volume greatly decreased

UK Involvement
The development of the concept of the P_T module, used to identify high P_T tracks. This includes the development of the design and production of the ASIC to be used in the 2S modules (**CBC – 130nm ASIC**)

Development of **FPGA** solution to provide tracking information to L1 trigger at **40 MHz**

CMS Upgrades – Track Triggering

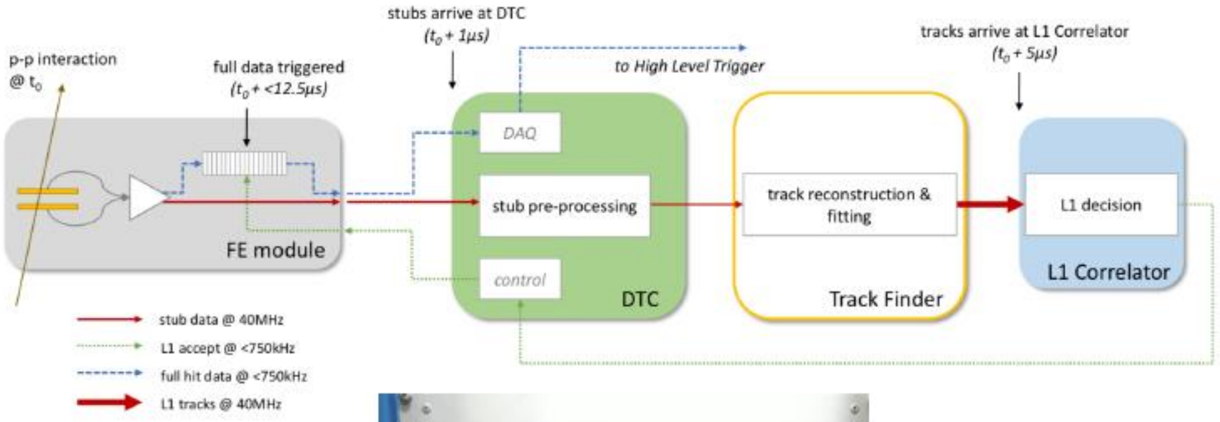
Hardware Track Triggering is an integral part of the tracker design

UK Involvement

UK has developed the concept of L1 Track-Trigger and has overall lead in several areas.

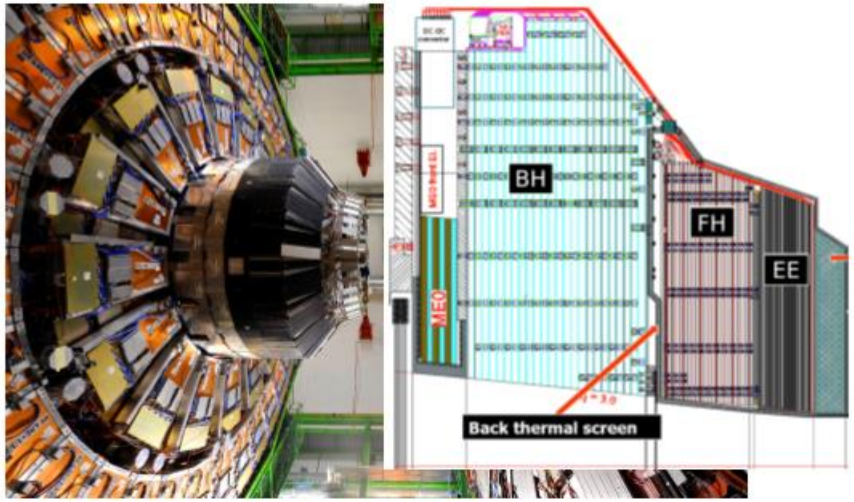
UK responsible for implementing ALL-FPGA solution, including SW/FW/HW demonstrators

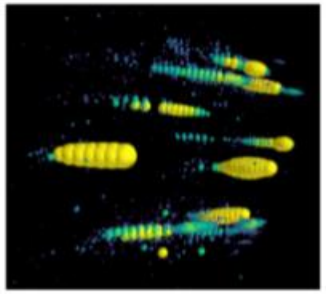
For the project UK has responsibility for Data, Data & Control Card (DTC) and Track Finding Algorithms (with international colleagues)



CMS Upgrades – Calorimetry Upgrades

High Granularity Calorimeter with 4D reconstruction of Shower Development
Sampling calorimeter with silicon sensors optimized for a high pileup environment (1cm^2 and timing of < 50ps)





300 GeV pions

~600 m² of silicon
6M channels
~100 µm strips

28 electromagnetic layers (14 for L1 trigger)
22 hadronic layers
4 cm² trigger granularity

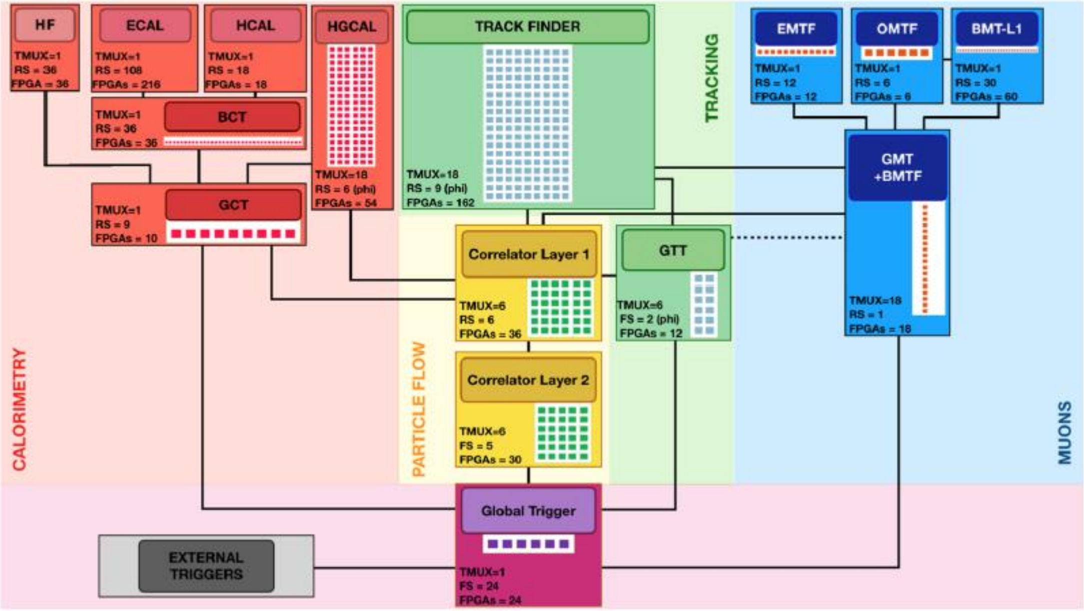
Delivers 3D clusters to L1 trigger latency 4 µs

HG Calorimeter *UK Involvement*
Developed the new paradigm for HG calorimetry
Leading in the development of Trigger Primitives, electronics and simulations

Current status
Boards in hand (same as tracker and trigger)
Writing firmware for calorimeter
Firmware for 3D clusters
Simulations & Reconstruction, part of the baseline
Prototype modules starting to be produced

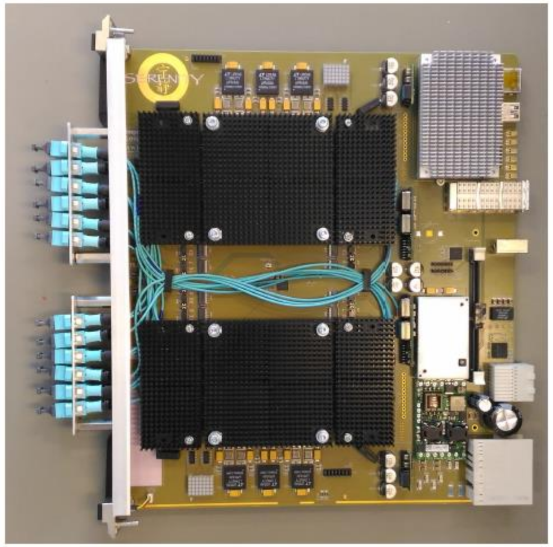
The **UK** is also involved in the upgrade of the **Barrel Calorimeter** developing trigger primitive firmware and Software.
In addition he UK is involved in Optical Fibre sharing, the sharing of crystal data between the 216 trigger processor FPGAs Serving 36 ECAL Barrel Super-Modules. Development of algorithms to reject spurious signals

CMS Upgrades – L1 Trigger



7Tb/s: 288 fibres @ 25Gb/s via 12x MTP24s

Feeds directly into all other UK upgrade projects



Trigger provides independent triggers for **Calorimeter, Muon** and **Tracking** systems. Also provides a particle flow Trigger combing sub-detector information. All serve The **global Trigger**. Aim to keep LHC thresholds.

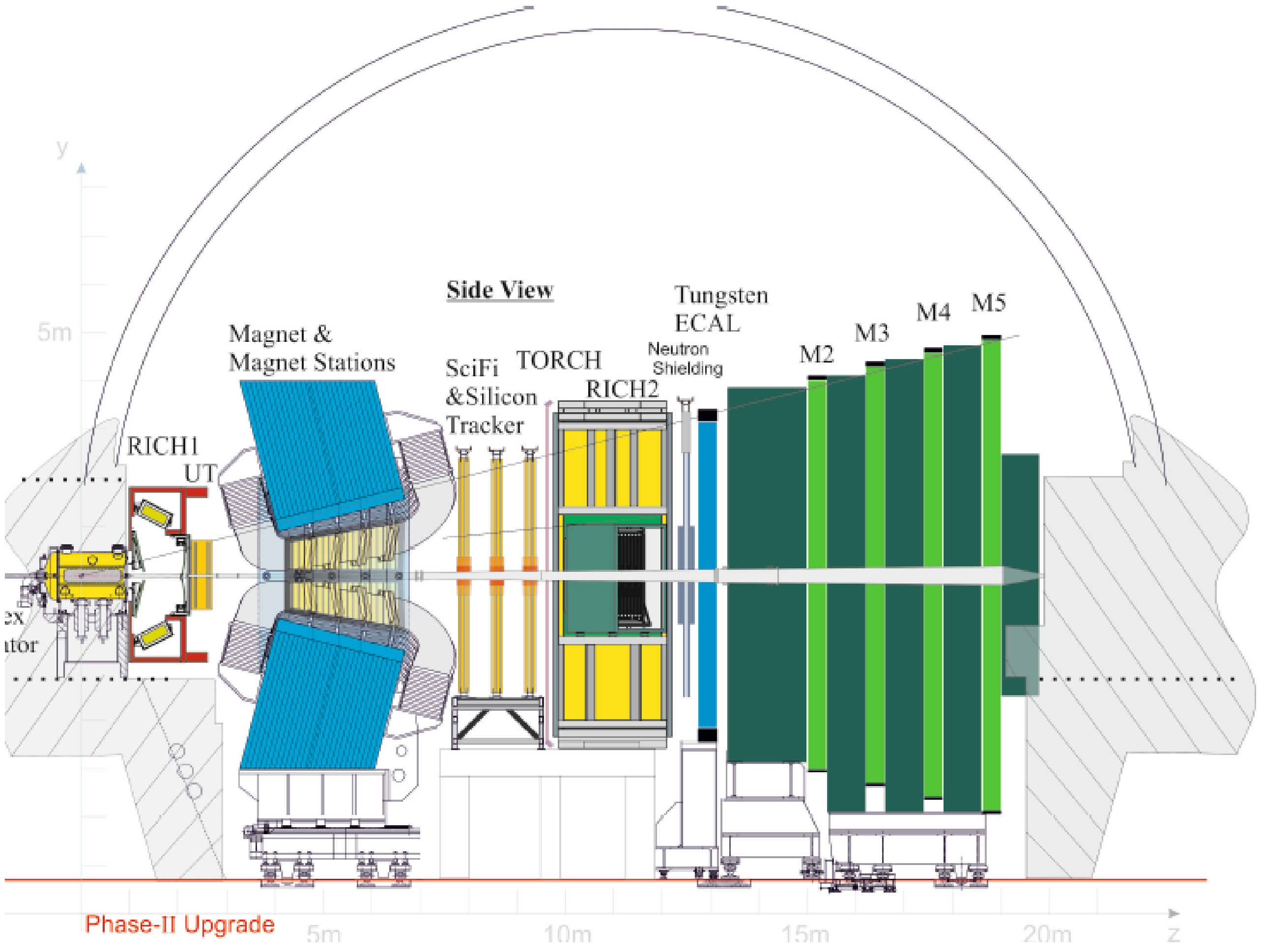
L1Rate increased from 100kHz to 750kHz. Latencies are increased from 3.8μs to 12.5μs. Link speed 25Gb/s
Data partition by region and in time as appropriate
Event and Time multiplexing

UK will provide Common Technology solutions – **Serenity ATCA** solutions to back-end electronic services

Flexible dual FPGA card : Flexible pluggable FPGA units
High density, low profile interposer Running at 28Gb/s
Prototype cards delivered.
UK provides: firmware and software, system integration
Status – multiple prototypes now in hand.

LHCb : Upgrades

LHCb is a b-physics experiment, designed primarily to measure the parameters of CP-violation in the interactions of b-hadrons



Upgrade now in progress as part of LS2

Single arm spectrometer operating in the range 10mRad to 300 (250) mRad in the bending (non-bending plane) corresponding to a rapidity range $1.9 < \eta < 4.9$.

Momentum measurement from a di-pole magnet

Aim to operate with the LHC in Run-2 at $2 \times 10^{33}\ cm^{-2}\ s^{-1}$

Factor of 5 increase on previous operation

Will be capable of trigger-less readout of the full detector at beam crossing rate of 40 MHz

Trigger is all software → full flexibility

Full reconstruction at readout - online

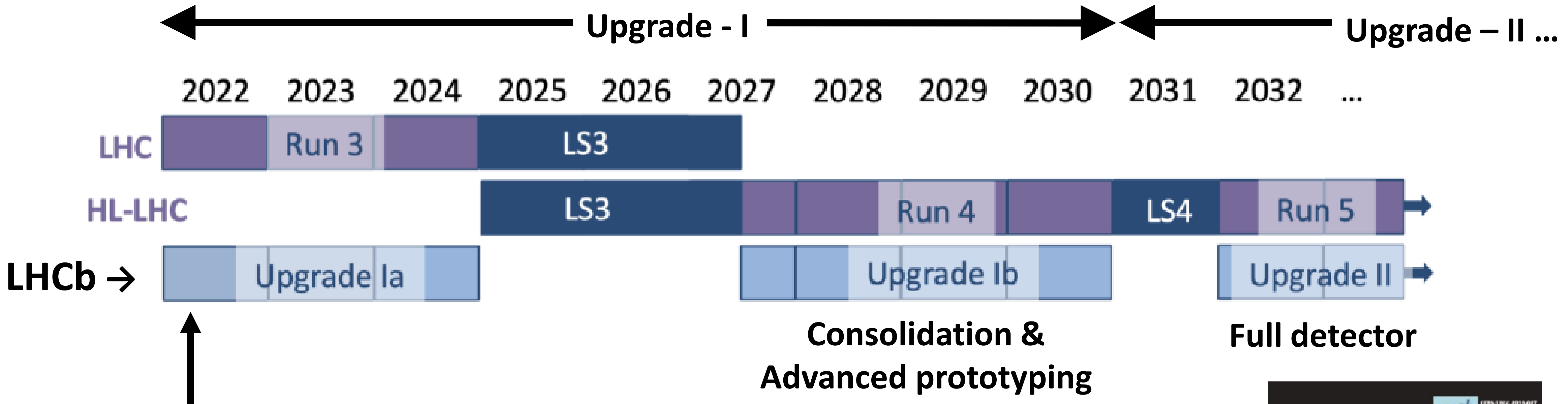
Upgrade to 90% of the detector channels

Upgrade to 100% of the readout & DAQ channels

Goal is to collect **50fb^{-1}** of data in **Upgrade-I** (2030) and **300fb^{-1}** in **Upgrade-II** (2032)

Strong UK involvement in many areas including VELO, RICH, …, MightyTracker, TORCH….

LHCb : Upgrade-timeline

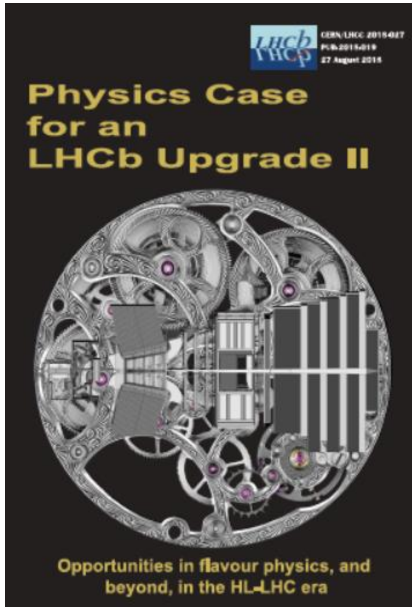


Next year

EoI was submitted in 2017
Physics case submitted in 2018
A Framework **TDR** is in preparation and will be submitted later this year

[LHCB-PUB-2018-009] arXiV:1808.08865

- Time dependent CP violation
- Time integrated CP violation
- Unitarity triangle
- Mixing and C violation in charm
- Rate decays
- Forward and High Transverse momentum physics
- Exotic hadrons and spectroscopy
- *Lepton universality*

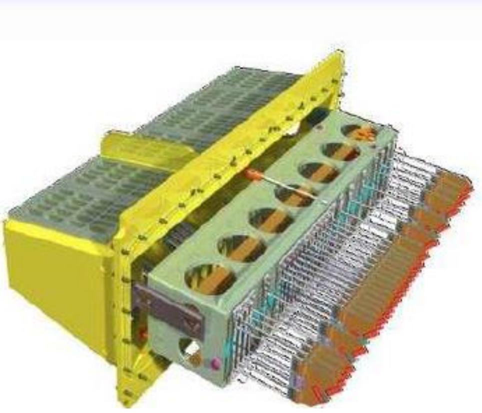


LHCb : Upgrade-I – Slide - 1

Vertex Locator VELO Upgraded

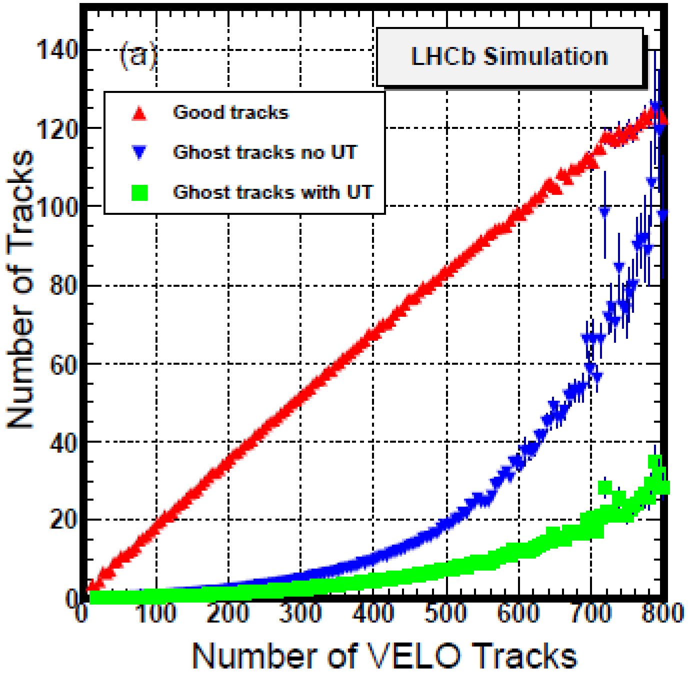
Strong UK involvement

26 planar stations of hybrid modules
41M channels of 55μmx55μm pixels
Readout by VeloPix ASIC .
Going closer to the beamline at 5.1mm from beam axis
Al foil reduced to 200-250μm.
Reduced material, closer to impact
Improved vertex resolution
Currently being installed at CERN



Upstream Tracker Upgraded

4 detector layers using silicon MS sensors
537k channels read out by custom ASIC. called SALT.
Below see number of ghost tracks with and without UT



RICH (1,2)

Strong UK involvement

Original & upgraded have 2 RICH detectors
RICH-1 upstream of dipole – full acceptance
RICH-2 downstream of dipole
Combination C_4F_{10}(R1) and CF_4 (R2) radiators – excellent K/π separation up to 100 GeV/c.
Same location and radiator for upgrade.
RICH-1 optics to be replaced, to deal with increased occupancy. R1&2 to use Multi Anode PMT with high granularity with new FE electronics.

LHCb : Upgrade-I – Slide- 2

Scintillating Fibre Tracker

Down-Stream Tracker

6 scintillating fibre mats composed of 6 layers of 2.5m long fibres with 250μm diameter.
Fibre modules couple to SiPM, cooled to -40oC and readout electronics, mounted in C frames with associated serves.

ECAL and HCAL

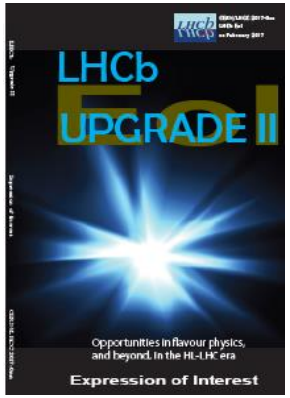
Combination of pre-shower/scintillating pad detector PS/SPD
Electro-magnetic calorimeter **ECAL** lead-scintillator Shaslik
Hadronic Calorimeter **HCAL**: iron absorber and scintillator tiles
PS/SPD was part of old L0 and is now obsolete
ECAL and **HCAL** new electronics for 40 MHz

Muons

Old system composed of 5 MWPC stations (1 M1 up and 4 downstream M2-M5)
M1 was part of trigger and is now obsolete
M2-M5 retained, M2 to use Triple-GEM (rate) all electronics to be 40 MHz

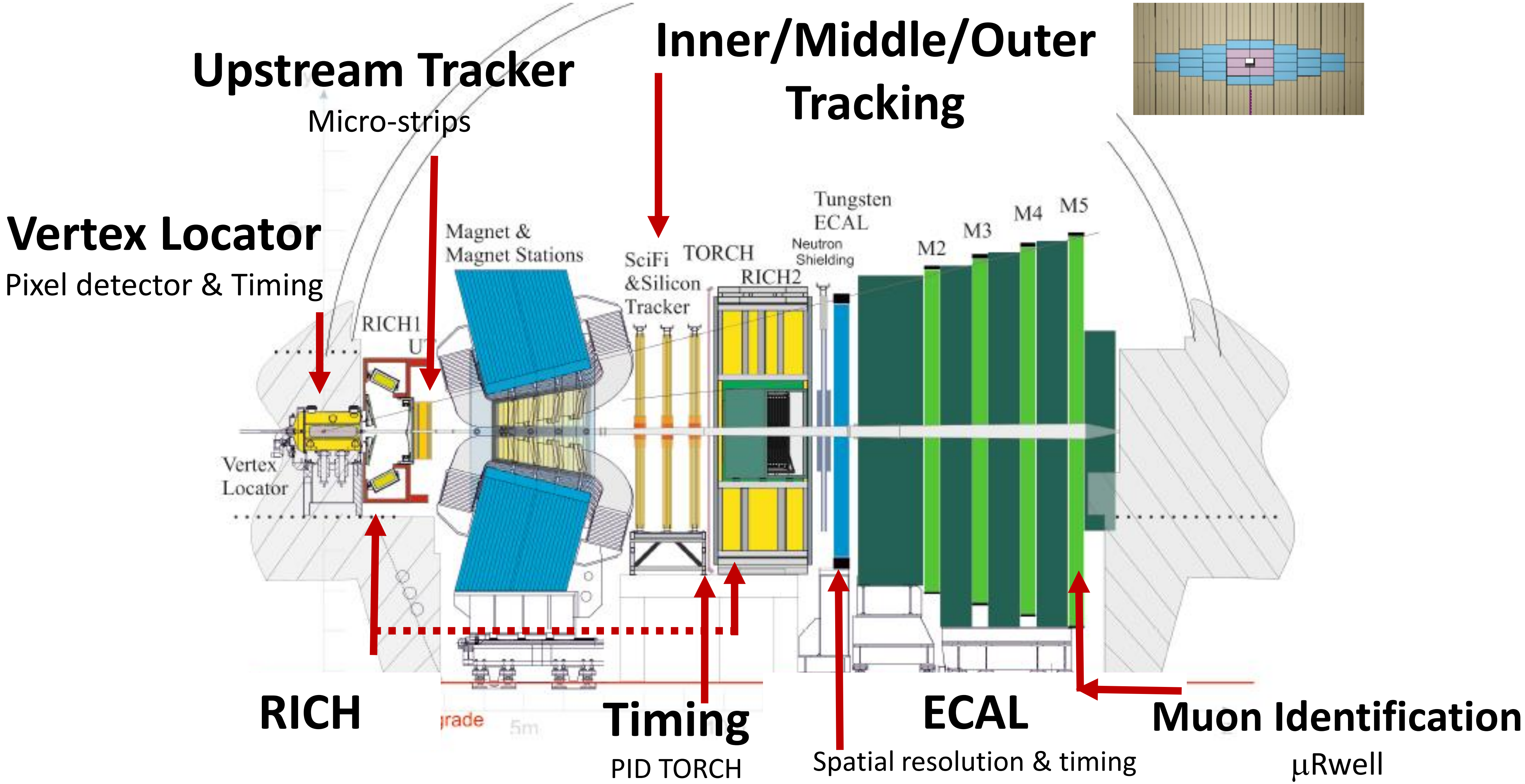
LHCb – Upgrade-II

- The challenges
  - Luminosities of 1.5 x $10^{34}cm^{-2}s^{-1}$ corresponds to 42 pp interactions per bunch-crossing
    - Or about 2,000 particles per crossing inside the detector acceptance
    - Most of the particles are produced over a narrow highly collimated region of the detector
    - Need excellent/pure association of tracks to charm and beauty vertices
  - Simulations show that excellent timing can play a crucial role in vertex separation
    - Requiring ~50ps per track allows miss-associated tracks to be kept at the % level
  - Tracking detector need to be able to cope with increased occupancy and be more radiation tolerant
    - Development of LGAD for timing resolutions and possibly using depleted monolithic CMOS or HV-CMOS detectors for the so-called Mighty-Tracker *(strong UK involvement)*
  - ECAL with finer segmentation and using materials with smaller moliere radius

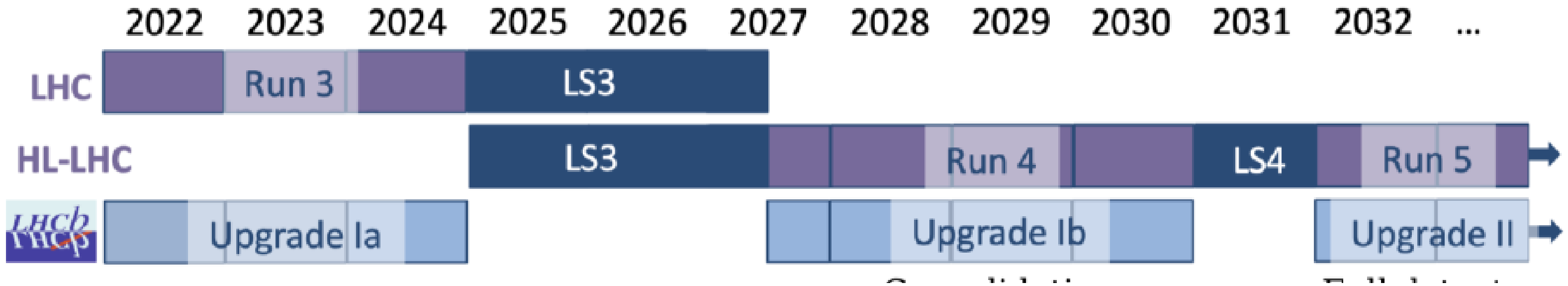


- Using LS3 (so-called Upgrade-Ib) for consolidation of Phase-I detector.
  - Install silicon-pixel tracker in the tracking stations downstream of the magnet MightyTracker HVCMOS
  - Commission technologies foreseen for Upgrade-II
  - A TORCH (**T**ime **O**f **I**nternally **R**eflected **CH**erenkov) light installed between RICH2 and Calorimeter could extend the particle identification capabilities for hadrons down to 10 GeV/c. Detector has 70ps timing resolution for single photons. *Significant UK involvement*

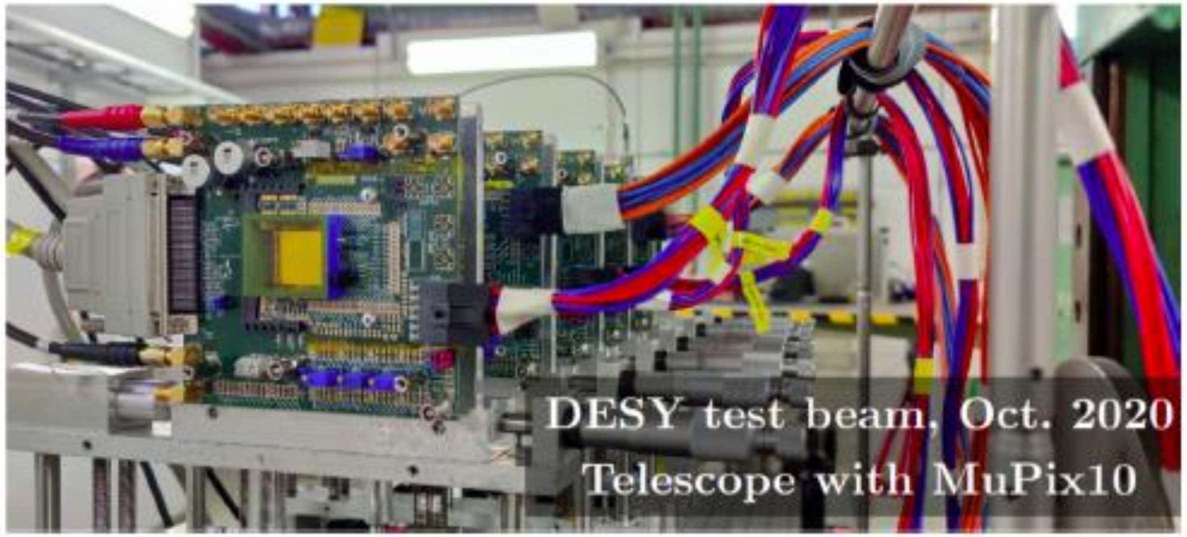
LHCb – Upgrade-II

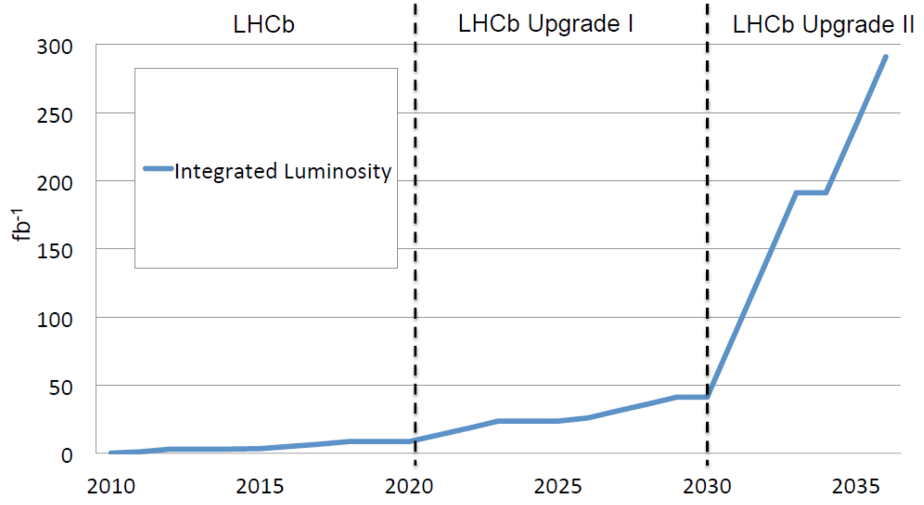


LHCb – Upgrade-II



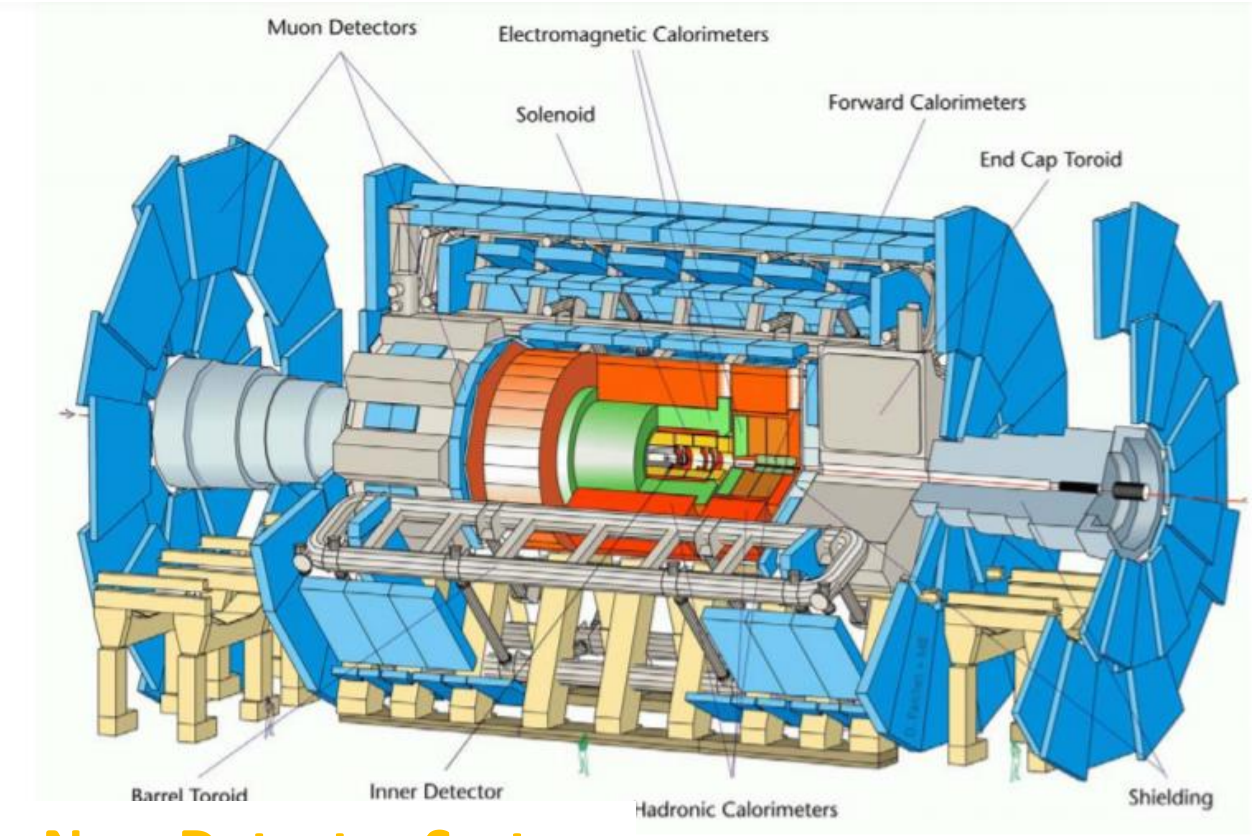
Upgrade II will be installed in LS4 to operate between **1-2 x 10^{34}cm^{-2}s^{-1}** and aims to collect **300fb^{-1}** of data
Probably the only large flavour physics experiment in the world on these time scales.
A program of R&D already underway for ECAL, Mighty Tracker and VELO
Picture shows CMOS chip being tested in a test-beam at DESY





ATLAS - Upgrades Phase I and II

Phase II Letter of Intent https://cds.cern.ch/record/1502664 **:The scoping document** https://cds.cern.ch/record/2055248



New Detector System

High Granularity Timing Detector
https://cds.cern.ch/record/2719855

Replacement

Inner Tracking Detector
https://cds.cern.ch/record/2257755/
https://cds.cern.ch/record/2285585/

TDAQ Upgrade .
https://cds.cern.ch/record/2285584

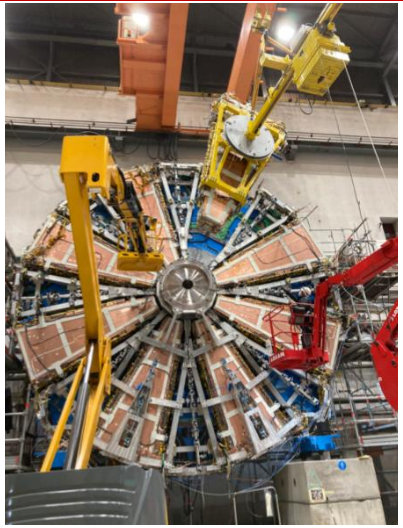
Electronics Upgrade/Consolidation

Muon system upgrade
https://cds.cern.ch/record/2285580

LAr Calorimeter
http://cds.cern.ch/record/2285582

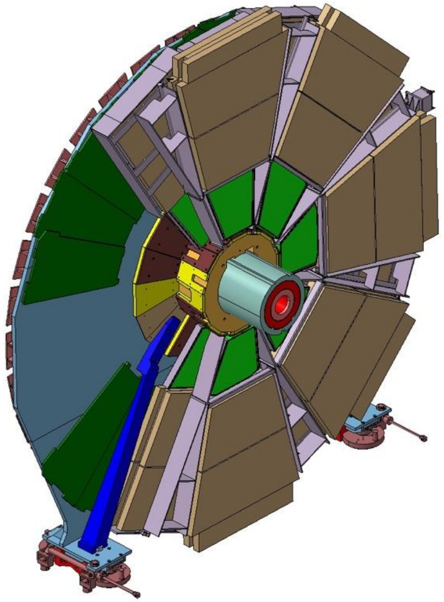
Tile Calorimeter
http://cds.cern.ch/record/2285583

ATLAS - Upgrades Phase-I



- Phase-I
  - Infrastructure consolidation
  - Upgrades to Calorimeter Electronics and associated triggering
    - Includes new Feature Extractors eFEX, jFEX …(strong UK involvement)

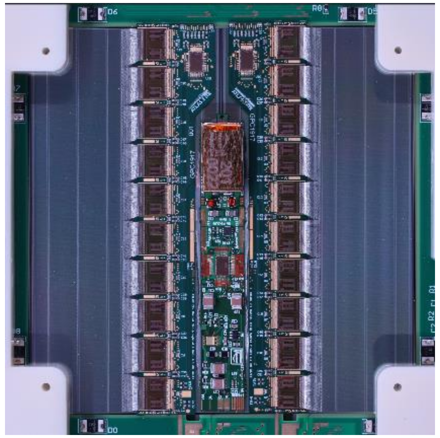
  - New Small Wheels
    - Major construction project
    - Replaces the first layer of End-Cap muon instrumentation and provides instrumentation and improved triggering – compatible with Phase II
    - need <1mrad angular resolution and associated trigger vector capability
    - *2 sTGC quadruplets for trigger, bunch id and vector tracking with <1mrad resolution*
    - *2 MicroMegas quadruplets for tracking with resolution <100μm*
    - **NSW-1** on track for installation in LS2 - **NSW-2** very tight for installation in LS2



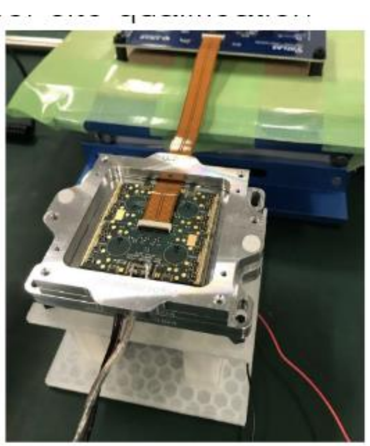
Inner Tracker ITk – Phase II

- All new Silicon design replaces the existing ID
- **Strips**: 4 barrels and 6 disks .
- **Pixel**: 5 flat barrels at small η, inclined layout at intermediate η, and ring geometry at large η.
- *Significant UK involvement*

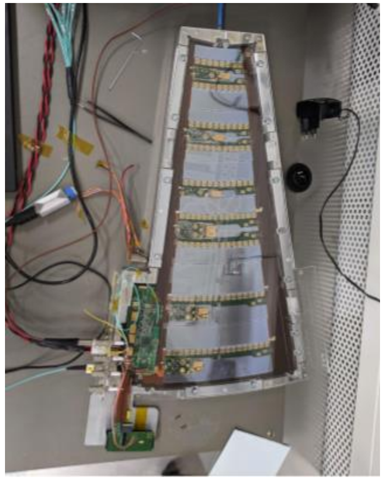
Strip Barrel Module

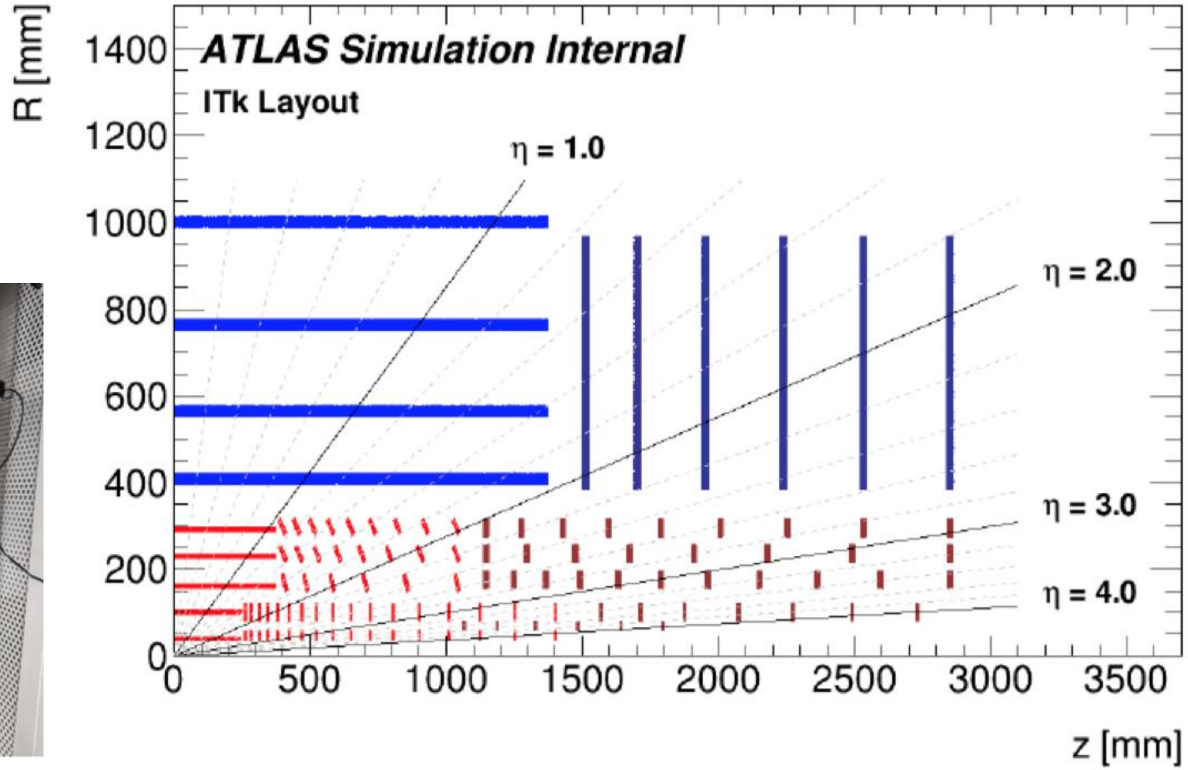


Pixel Module



Strip Petal



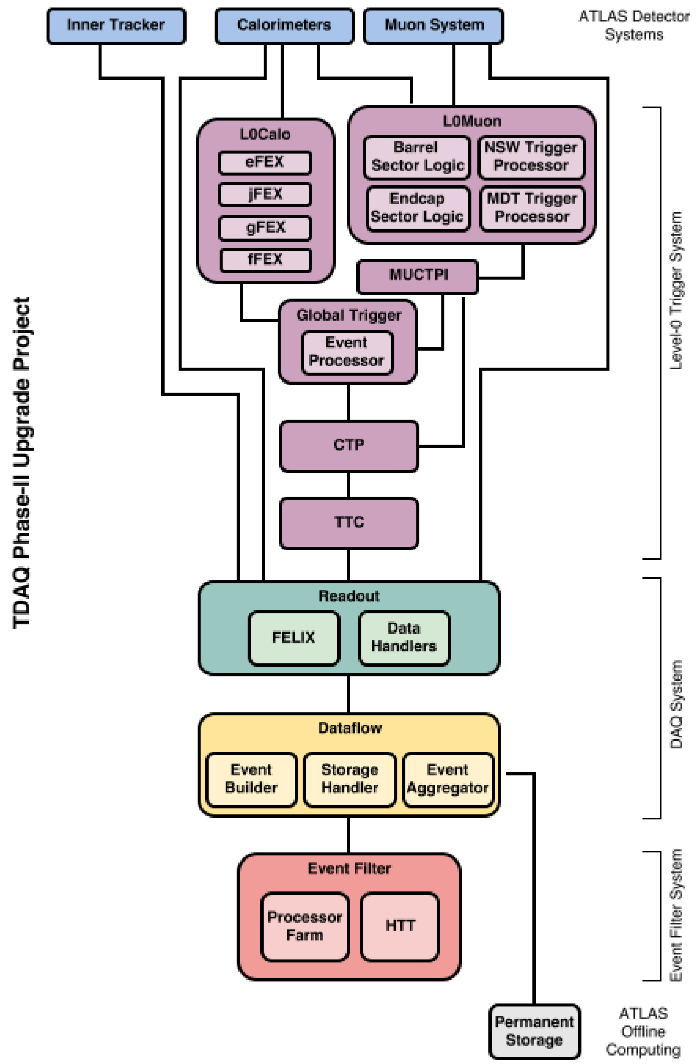


- Acceptance extended from |η|<2.5 to |η|<4.0 – Inner pixels must be replaced at **400fb^{-1}**
- Number of hits in barrel ~ 13 including 2 hits/strip module) In forward regions at least 9 pixel hits
- Minimizes silicon area and material.

TDAQ in Phase-II

CERN-LHCC-2017-020

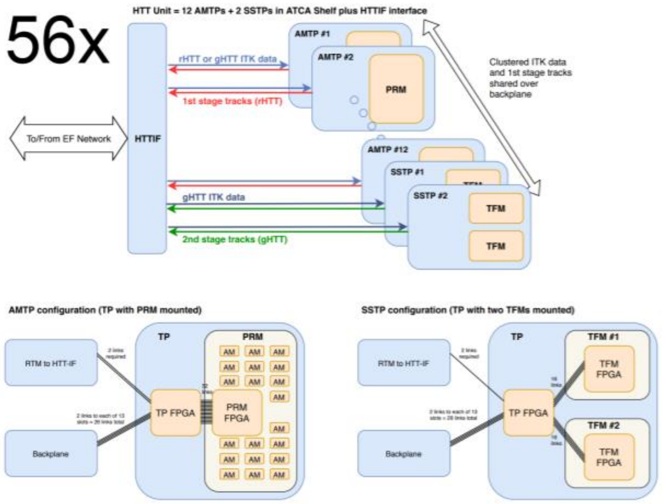
- Goal is to keep trigger-object thresholds as low as for Run2
- Baseline is a single-level of Hardware trigger L0 running at 1 MHz (latency/rate < 10 µs)
- Input from Calorimeter and Muons
- The system includes a single L0 trigger running at 1 MHz.
  - *A 4 MHz split L0/L1 evolution option dropped in late 2020*.
- EF farm performs offline-like reconstruction and selection on commodity processors, with track reconstruction offloaded to custom hardware (regional @1MHz, global @100kHz)
- The output to tape is 10kHz.

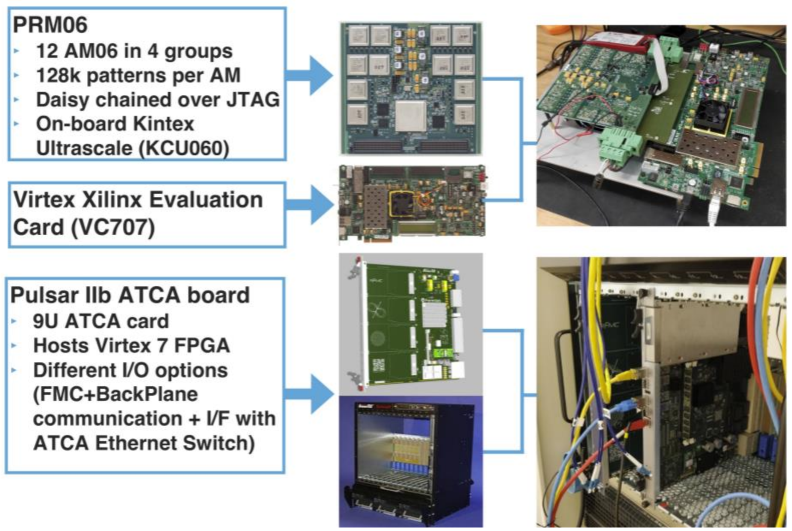


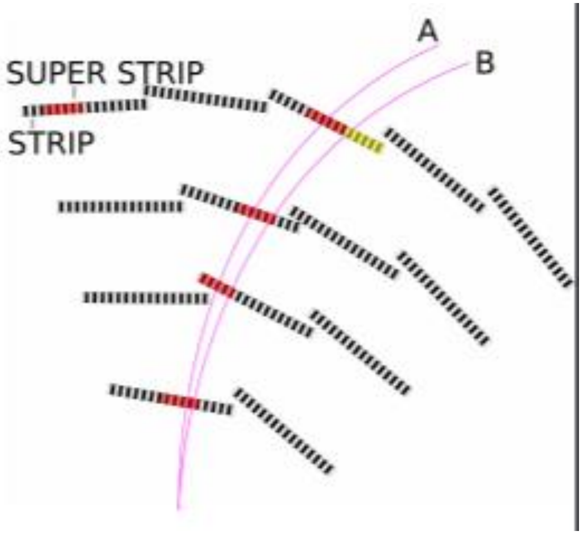
Hardware Track Triggering

Strong UK involvement

- One of 3 options currently under study in 2021 for Event Filter Tracking
- **Tracking steps**: Data preparation, Pattern recognition, 1st stage track fit, 2nd stage track fit
- 1st stage in **FPGA**, 8 layer tracks with cluster resolution, 2nd stage FPGA full 13 layers close to offline resolution
- **HTT** hardware are on track: demonstrators, firmware, architecture
- Associative Memory (**AM**): development like FTK
- Track Processor (**TP**): full demonstrator schematics, layout and routing complete.
- Rear Transition Module (**RTM**): 1st hardware versions complete & under test
- Pattern reco Mezzanine (**PRM**) Demonstrator board design completed: TFM two demonstrator boards produced



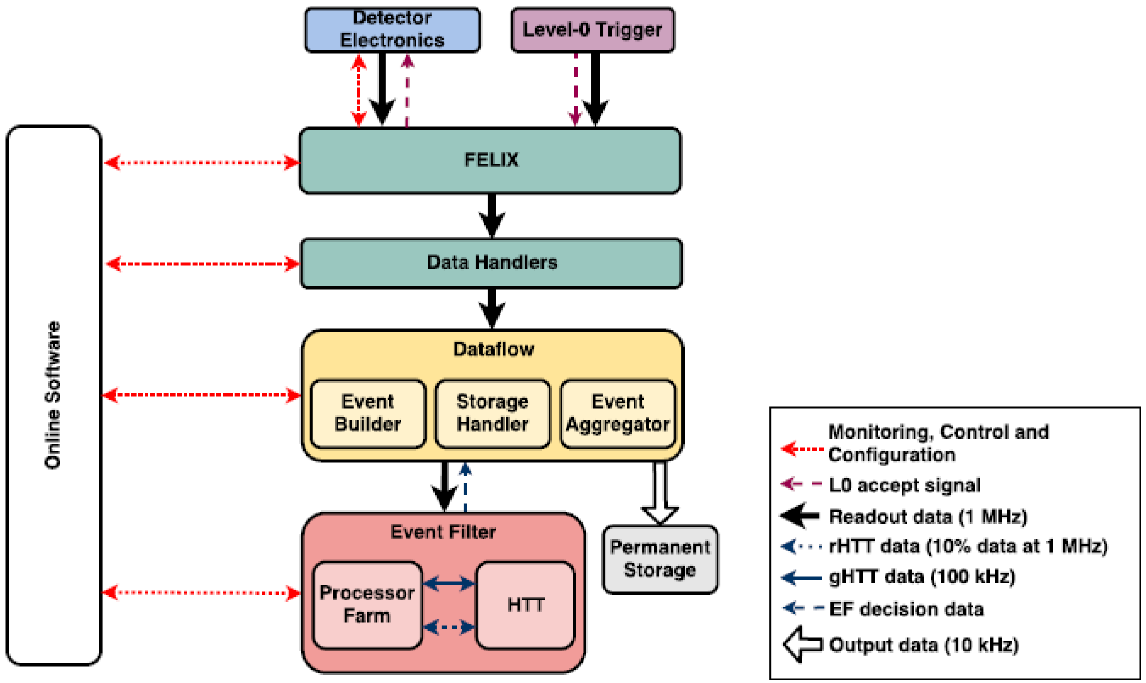


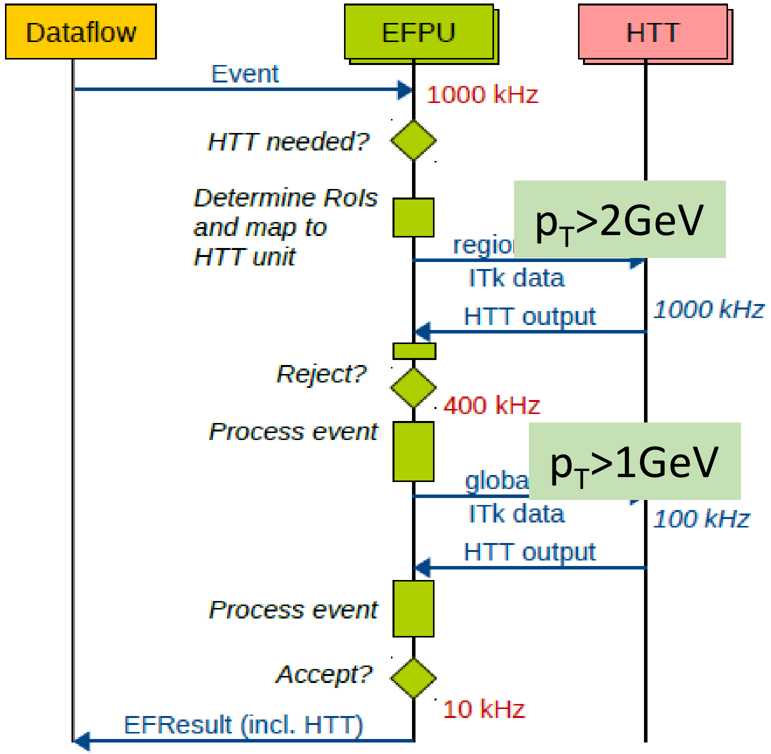


TDAQ Upgrade DAQ and HLT

CERN-LHCC-2017-020

- **DAQ** system based on FELIX universal network-based interface for **TTC** and all **DAQ** functions.
- **Event Filter** one option consists of Hardware-based Tracking for the Trigger (**HTT**) (based on Associative Memory technology for track finding and FPGAs for track fitting) and processor farm for sophisticated HLT event selection.
- **Regional HTT** runs on 1 MHz event stream and reduce rate to ~400 kHz output. **Global HTT** runs at ~100 kHz to find all tracks with p_T > 1 GeV and reduce final output to the required 10 kHz.



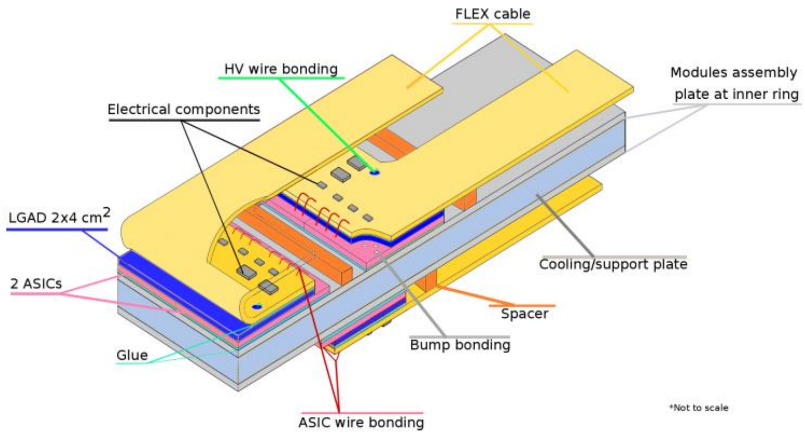


Strong UK involvement

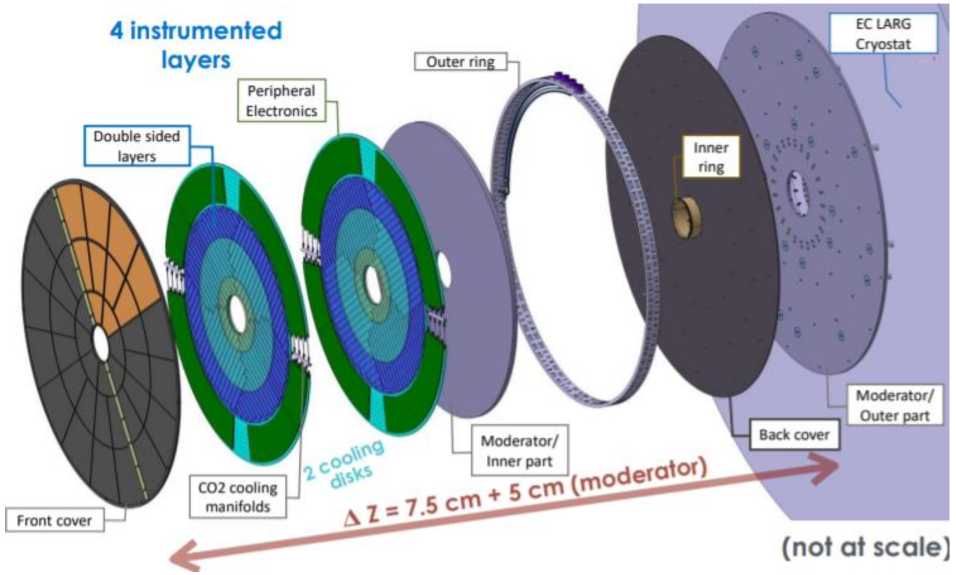
High Granularity Timing Detector

CERN-LHCC-2018-023

- Timing detector that can be used in addition to track z_0 to separate vertices from different pp interactions in a high pile-up environment
- Covers the region between $2.4 < |\eta| < 4.0$ or 12cm < R < 64cm in 3 consecutive rings
- ~4 layers of low-gain avalanche detectors LGAD with 30-50 ps time resolution on track, to be installed in space between ID and calorimeter end-caps. Also provides luminosity measurement



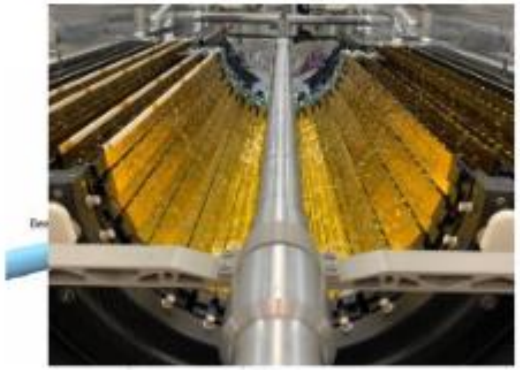
LGAD sensors
8032 modules 2 cm x 4 cm
2 ASICs (ALTIROC), 3.6 M channels
Pad size 1.3 x 1.3 mm^2



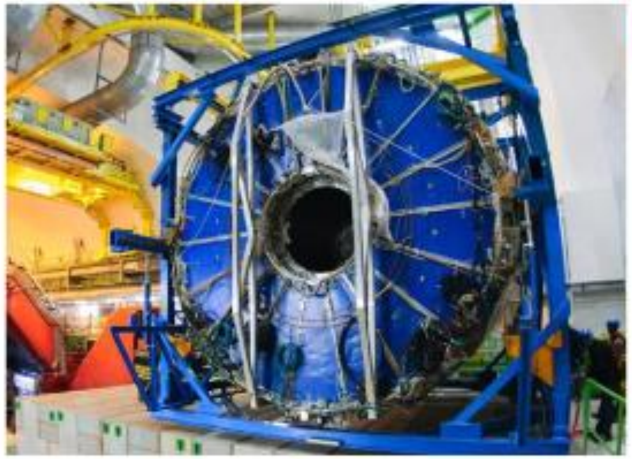
ALICE

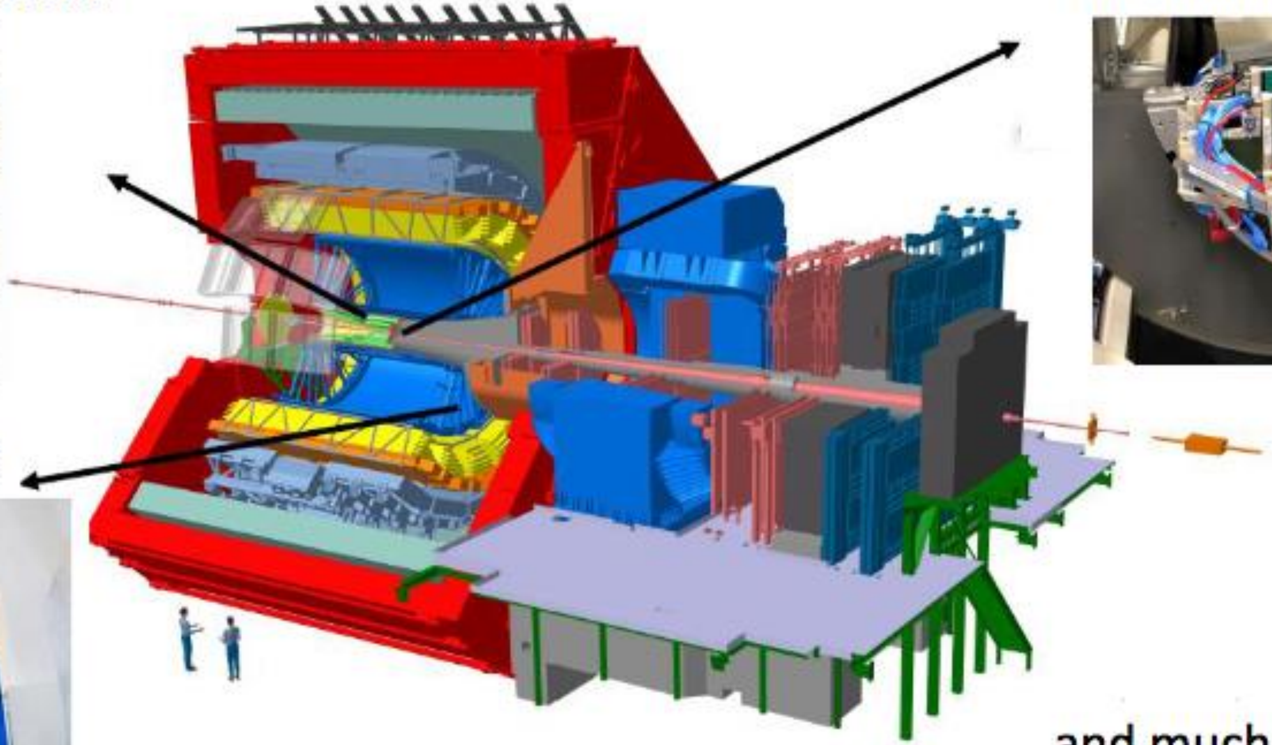
ALICE is optimized to study heavy-ion Pb-Pb nuclei collisions at a CoM energy up to 5.02 TeV per nucleon pair.

All-pixel Inner Tracking System

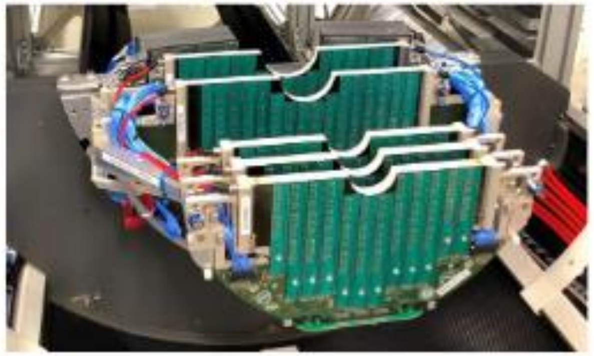


GEM-based TPC readout





Pixel Muon Forward Tracker



Challenges

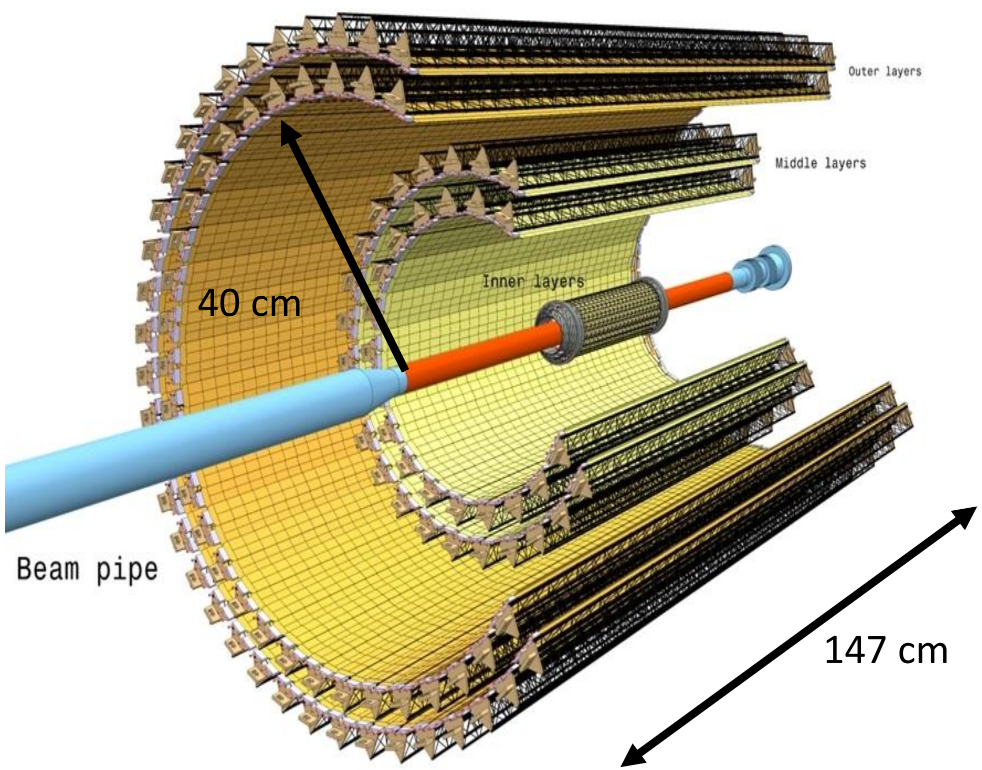
Record minimum-bias collision data at 50kHz (limited to ~1kHz in Run-2 by TPC)

Goal - Collect 13nb^{-1} in Runs 3 & 4

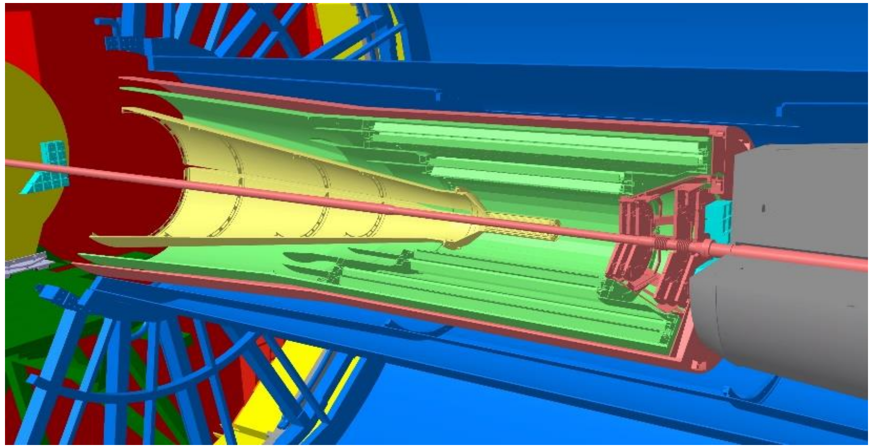
… and much more:

- Fast Interaction trigger
- New Online-Offline systems
- Readout upgrade of all detectors

ALICE - ITS



Expected radiation load
- TID: ~ 270 krad
- NIEL: ~1.7×10^{12} 1MeV n_{eq} / cm^2



ITS2 has a barrel geometry:
- 7 layers; 3 (IL), 2 (ML), 2(OL)
- 192 staves; 48 (IL), 54 (ML), 90 (OL)1

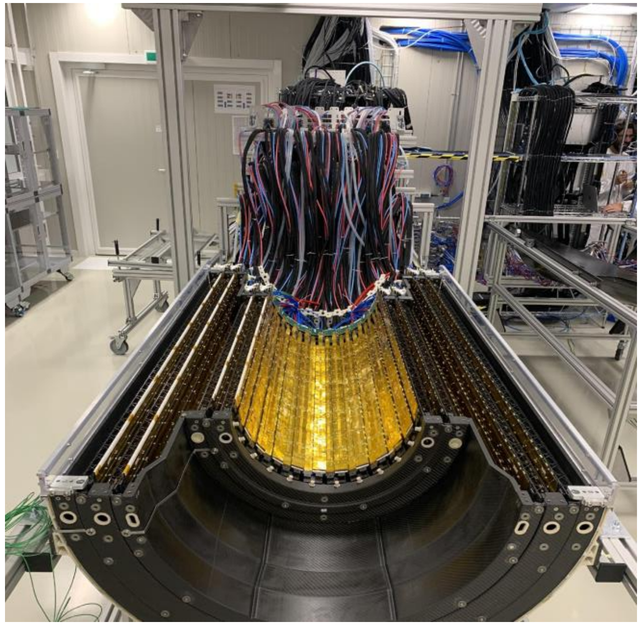
- Monolithic chip produced by Tower Jazz in 180 nm CMOS imaging process technology
- High resistivity (>1 kΩcm) p-type epitaxial layer

(25 µm thick) on p-type substrate

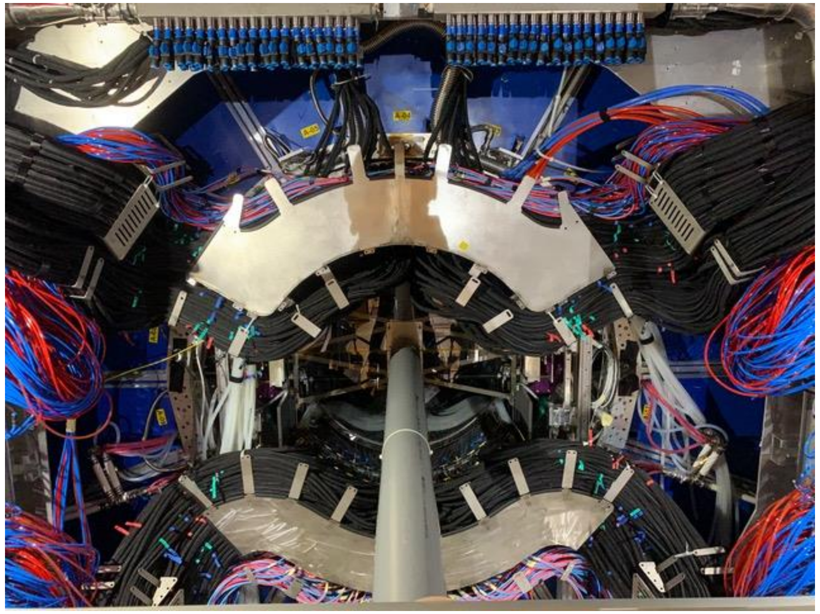
First large Si tracker entirely based on CMOS Monolithic Active Pixel Sensors (MAPS) – ALPIDE (50 µm inner/100 µm mid/outer)

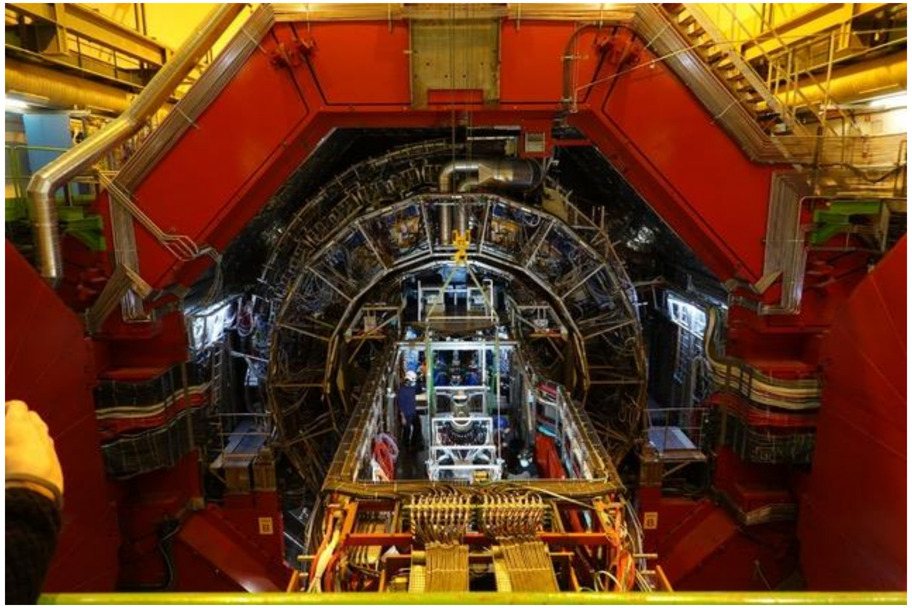
ALICE -

2019 End of Construction

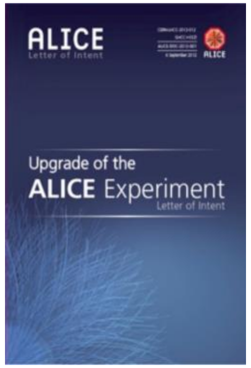


Installation on the beamline in 2021

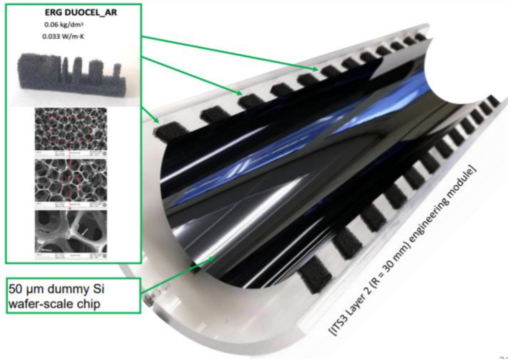


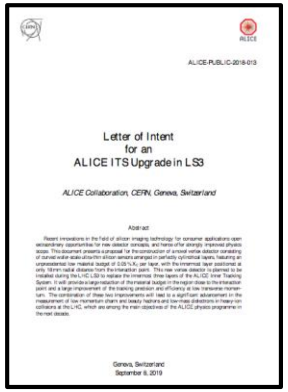


UK involvement in module production and stave loading.
Reception and commissioning at CERN
R&D for sensors at Tower



Inner-most tracking layers to be replaced by 3 ultra thin, wafer-scale, bent MAPS. UK involvement




ALICE-PUBLIC-2018-013

Letter of Intent
for an
ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

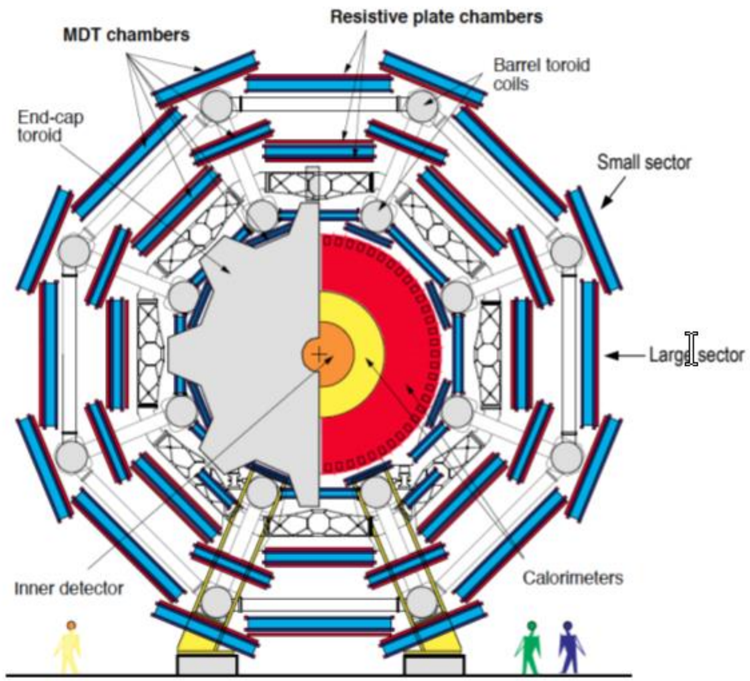
Geneva, Switzerland
September 6, 2019

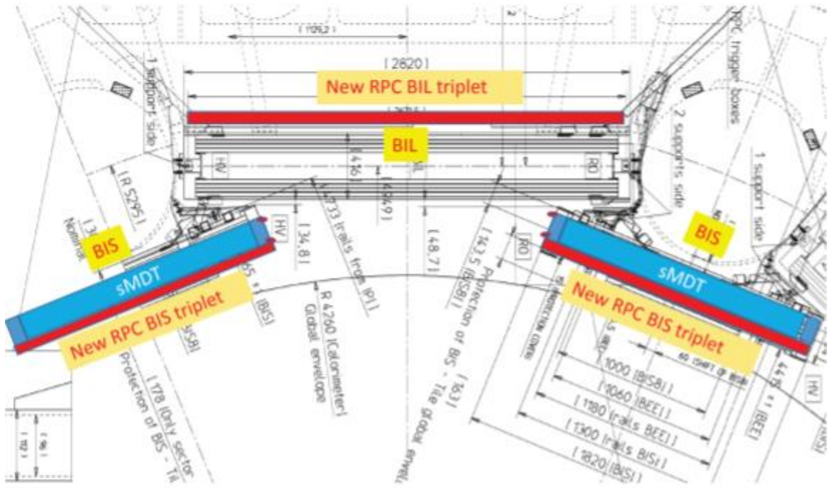
Conclusions

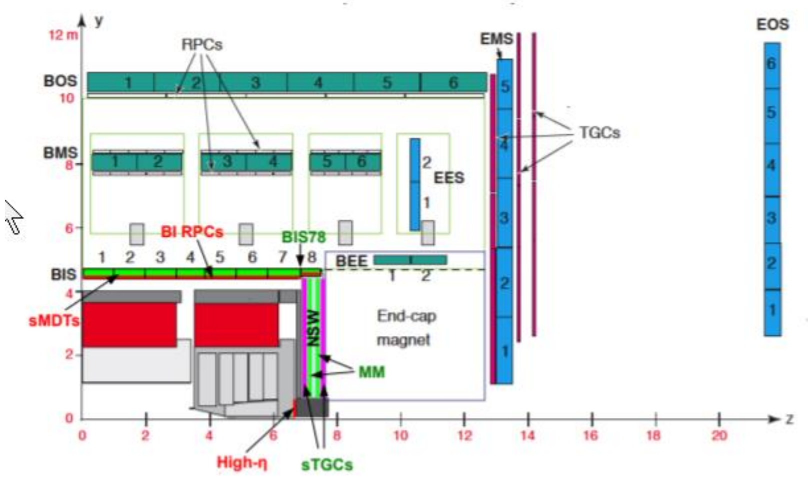
- LHC and HL-LHC upgrades are enormously challenging technical endeavours driven to delivering the exciting physics that the machine was conceived for.
- The plans and execution of the Phase-I and Phase-II upgrades are in progress and proceeding well.
- Over the last 12 months, Covid-19 has slowed down the progress and the established timescales are now under threat and are being examined afresh.
- Future upgrades are also being planned and they look very exciting.
- The UK is playing a unique role and is at the heart of these developments.

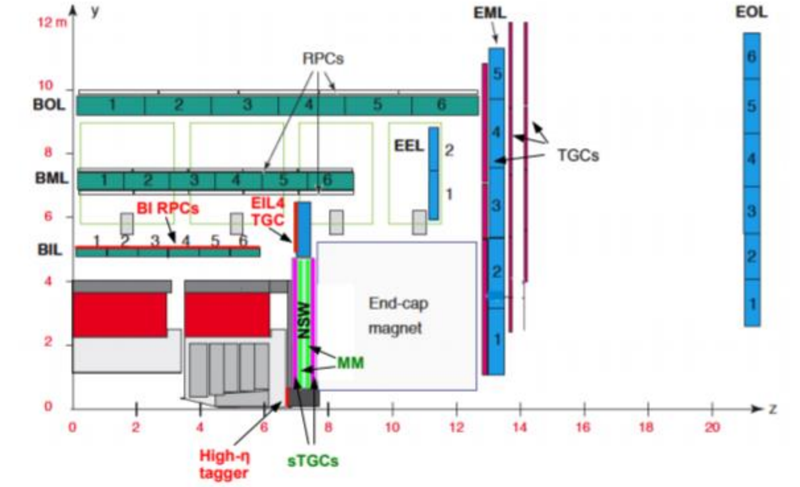
Muon Spectrometer Upgrade

CERN-LHCC-2017-017









- Replacement of all frontend on-and off-detector readout and trigger electronics. Enhanced triggering, all data shipped to USA15
- Major improvement in trigger capability, robustness, background suppression and increased acceptance by adding new detectors: **BI RPC, sMDT, EIL4 TGC**
- Present MS has three RPC layers. Addition of fourth RPC layer (triplet) => major improvement in robustness!
- Replacement of the HV and LV supplies