Track Finding in the CMS Level 1 Trigger for HL-LHC: Challenges, Design and Implementation

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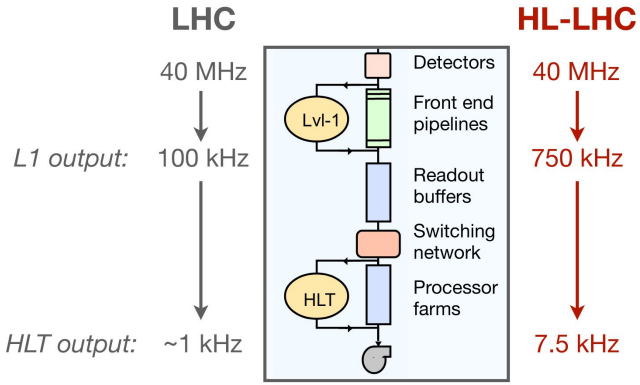
Contents

Introduction

- Triggering at CMS achieved in 2 stages:
  - Level 1 (L1): online reconstruction, small window
  - High Level Trigger (HLT): offline, uses full event dataset
- HL-LHC will produce large datasets
  - Up to **4000fb^{-1}**
  - Will enable precise measurements of Higgs boson properties & searches for rare SM and BSM processes
- Cost of HL-LHC is an increase in pileup by an order of magnitude, from up to 200
- Increased luminosity will be a particular challenge for the trigger system

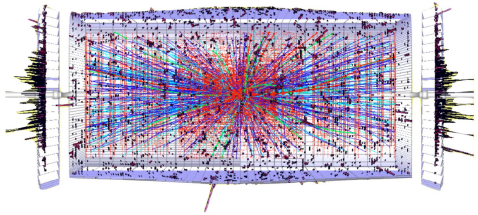


Instantaneous Luminosity

LHC (design): 10^{34} cm^{-2}s^{-1}

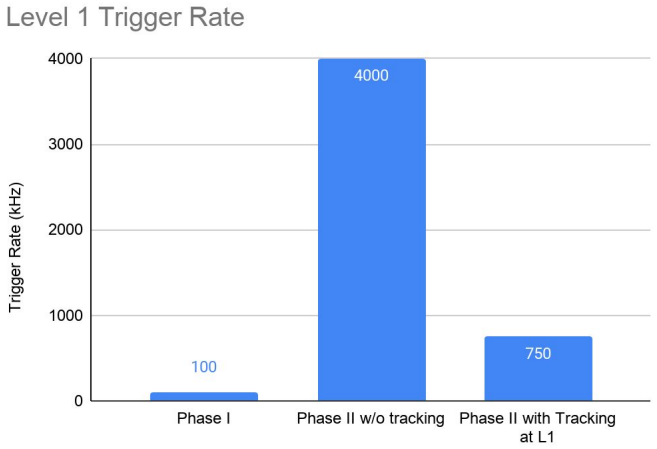
LHC (Run-2/3): 2 x LHC

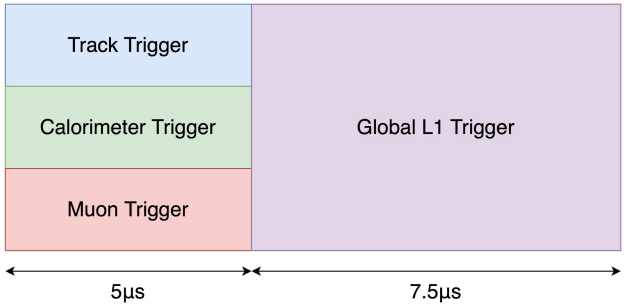
HL-LHC: 7.5 x LHC



Tracking at L1

- Tracking information will be used for the first time at L1
- Presents an unprecedented challenge in data processing
  - Raw hit rate of approx. **400Tb/s**
  - Decision window of 12.5μs (**5μs for track reconstruction**)
- On-detector filtering to reduce hit rate
- Off-detector reconstruction using next-generation Xilinx FPGAs on custom hardware

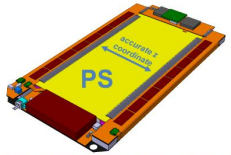




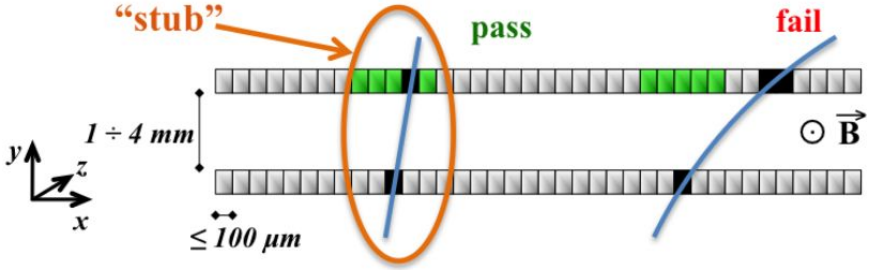
Front End Processing

- **Novel** design for silicon tracker modules
  - Dual layer to allow determination of bend
- Only low bend (high p_T) hits sent to L1
  - Stubs below **2 GeV/c** suppressed
  - Reduces data rate by **a factor of 20**
- FE ASICs located on the module perform initial processing, reduces required bandwidth to counting room.
- All stubs stored in a circular buffer on module for 12.5μs, before signal received from L1 to readout or discard event

PS modules (pixel-strip)
- Top sensor: 2x2.5 cm strips, 100 μm pitch
- Bottom sensor: 1.5 mm x 100 μm pixels

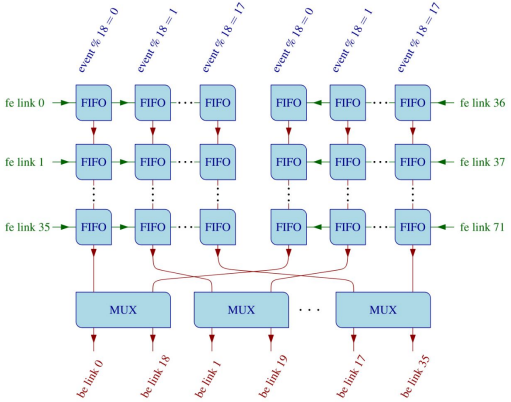


2S modules (strip-strip)
- Strip sensors 10x10 cm^2
- 2x5 cm long strips, 90 μm pitch

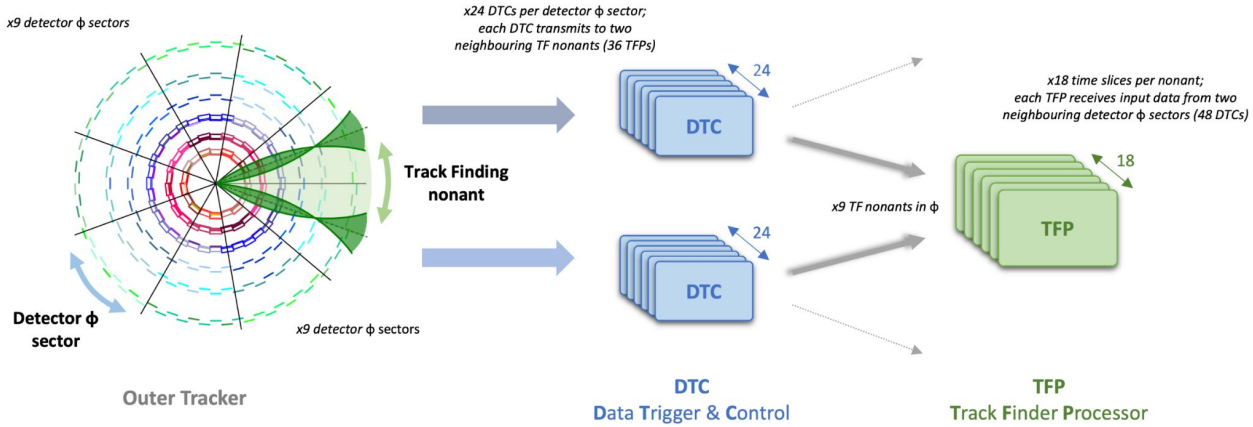


Back End Processing

- Outer Tracker split into 9, 40° sectors (nonants) in ϕ
- Data from each nonant first processed in 24 DTC boards (216 total)
  - Decode optical link data
  - Convert stub coordinates from local to global
  - Route stubs to the appropriate TF board using a systolic array of FIFOs
- Each TF board handles all stubs in a nonant for 1 in every 18 events
  - 9 x 18 (162) TFP boards required in total

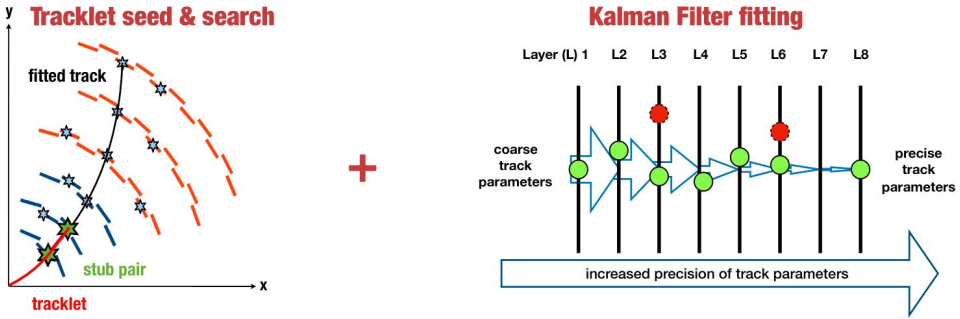


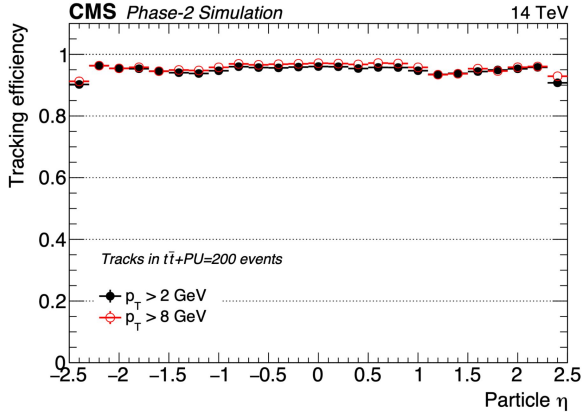
Above: Diagram showing the algorithm for the DTC stub routing.

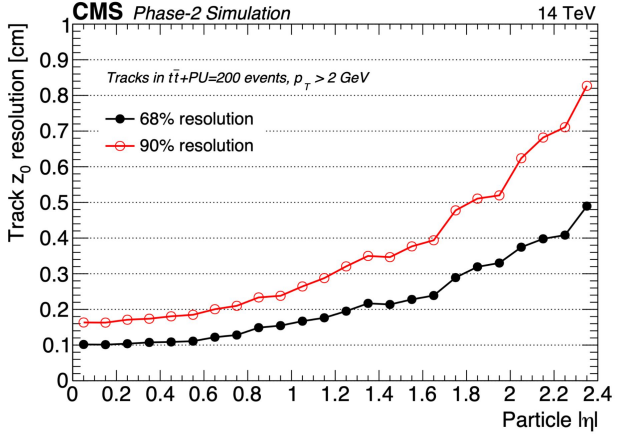


Track Finding Algorithm

- Seeds (“tracklets”) formed of pair of stubs, collections of valid stubs generated using road-search algorithm
- Fitting of track helix parameters and identification of best candidates performed by Kalman Filter
- Makes use of HLS for development
  - Language similar to C++ for use in FPGAs intended to lower the barrier for contribution to project
- Extensions to algorithm to account for displaced tracks and improve efficiency for electrons now being considered

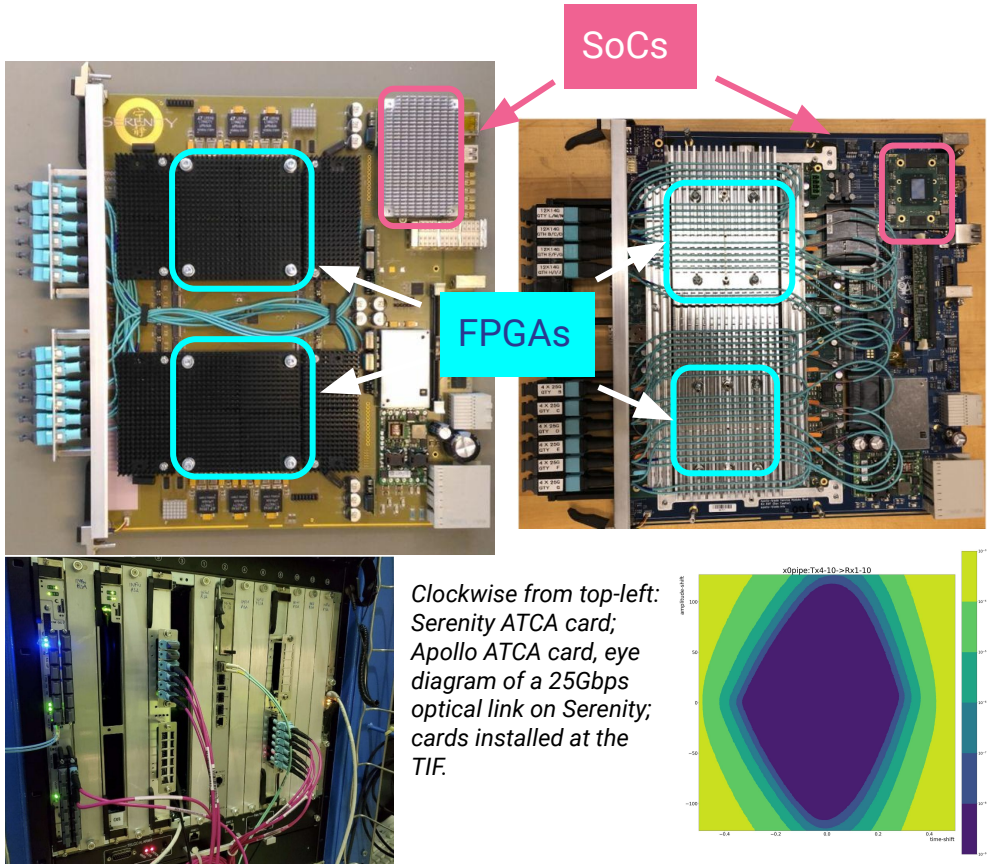






Back End Hardware

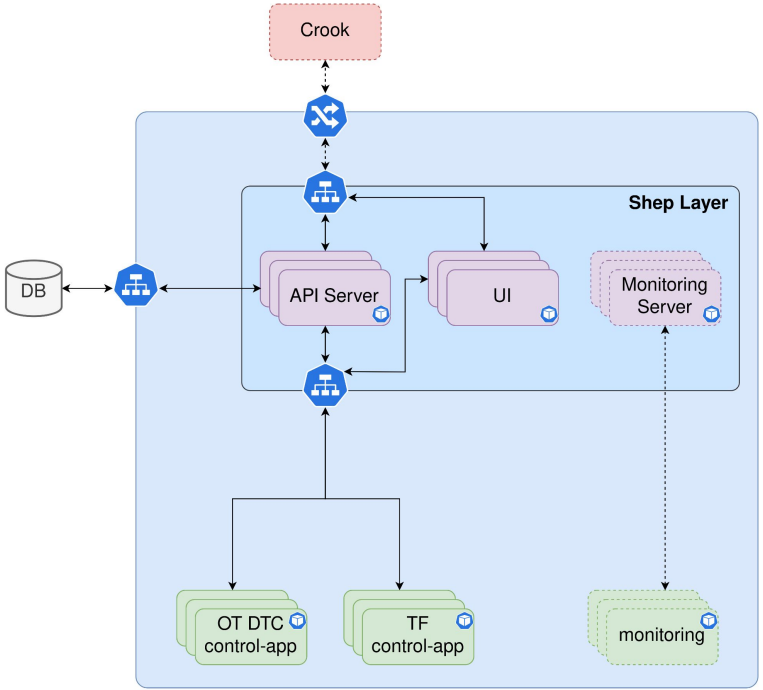
- ATCA form factor, up to 14 cards in a crate, each capable of **terabit** scale processing
  - DTC: Serenity
  - TFP: Apollo
- Highly flexible design, will be used for other sub-detectors as well as other experiments
- FPGA technology allows for parallel processing at a level impossible on standard CPU architecture
- All variants have same fundamental design
  - Up to 2 Xilinx FPGAs
  - Optical links for data transfer (up to 200 links, each capable of up to **25Gb/s**)
  - SoC for board control
  - 300-400W per card
- Algorithms developed using the EMP framework



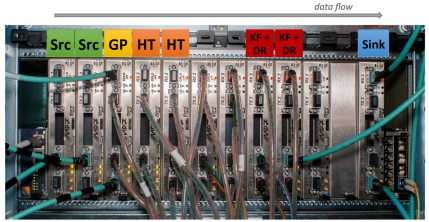
Clockwise from top-left: Serenity ATCA card; Apollo ATCA card, eye diagram of a 25Gbps optical link on Serenity; cards installed at the TIF.

Online Software

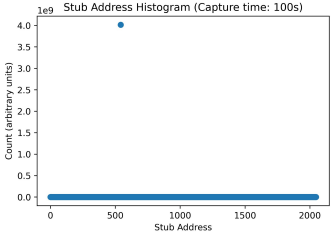
- SoC on each BE processing card provides scope for edge computing within the system.
  - Individual control of cards
  - Calibrations & histogramming at a card level
- Leveraging use of industry software for control and monitoring
  - Docker + Kubernetes
  - RESTful APIs
- 3 Tier design
  - HERD: on-card processing
  - Shep: multi-card command and control
  - Crook: system-wide command, interface with CMS run control



Demonstrations



Proposed track finding algorithms demonstrated on Phase I hardware



First stubs generated by the front end hardware received on prototype Phase II back end card

Hardware demonstration of Hybrid TF algorithm

2016

2019

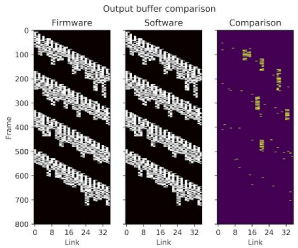
2020

Early 2021

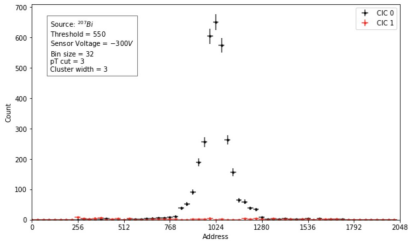
Mid 2021

Late 2021

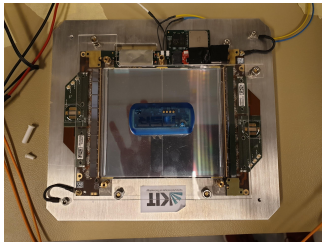
DTC routing firmware demonstrated



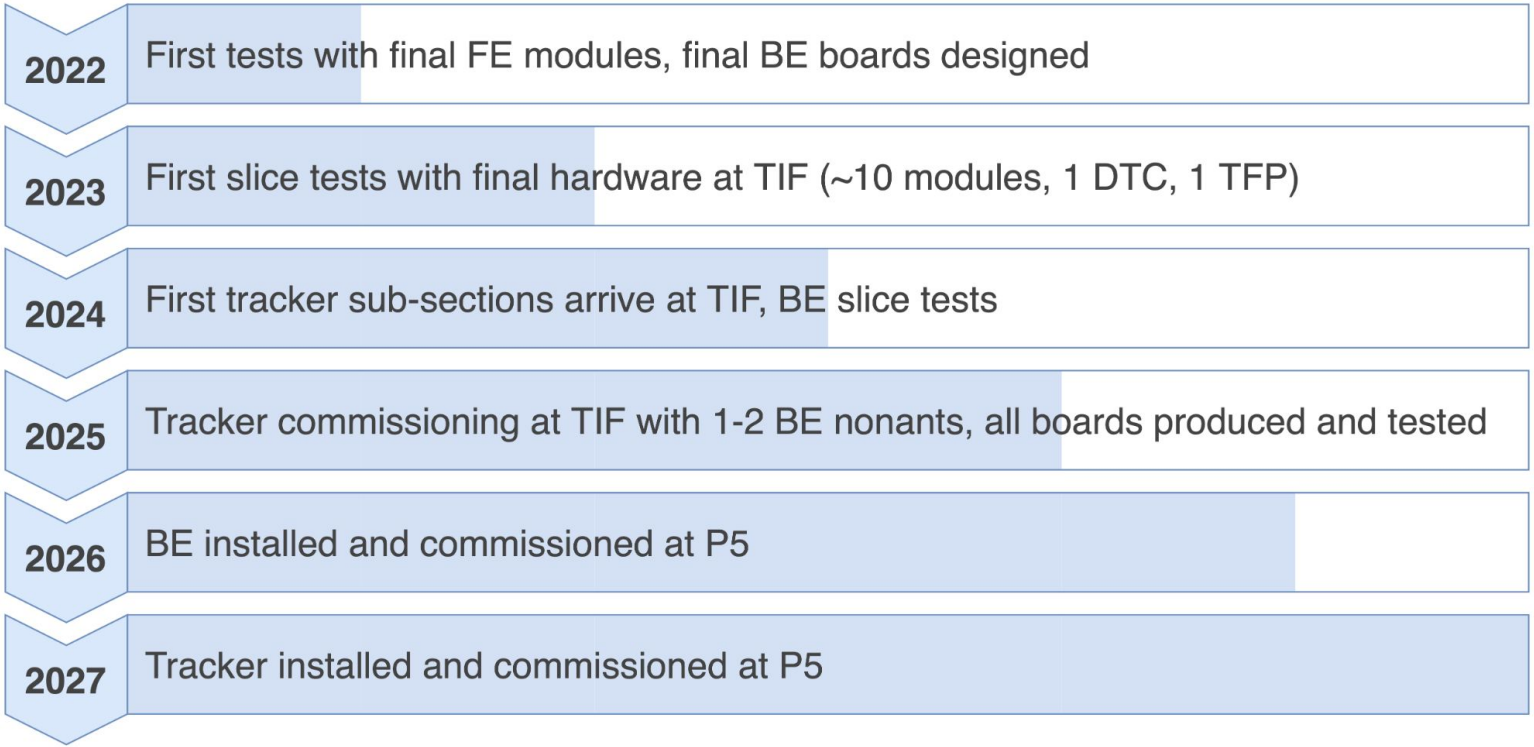
First genuine stubs recorded in DTC



Beam Test of vertical slice



Looking Towards LS3

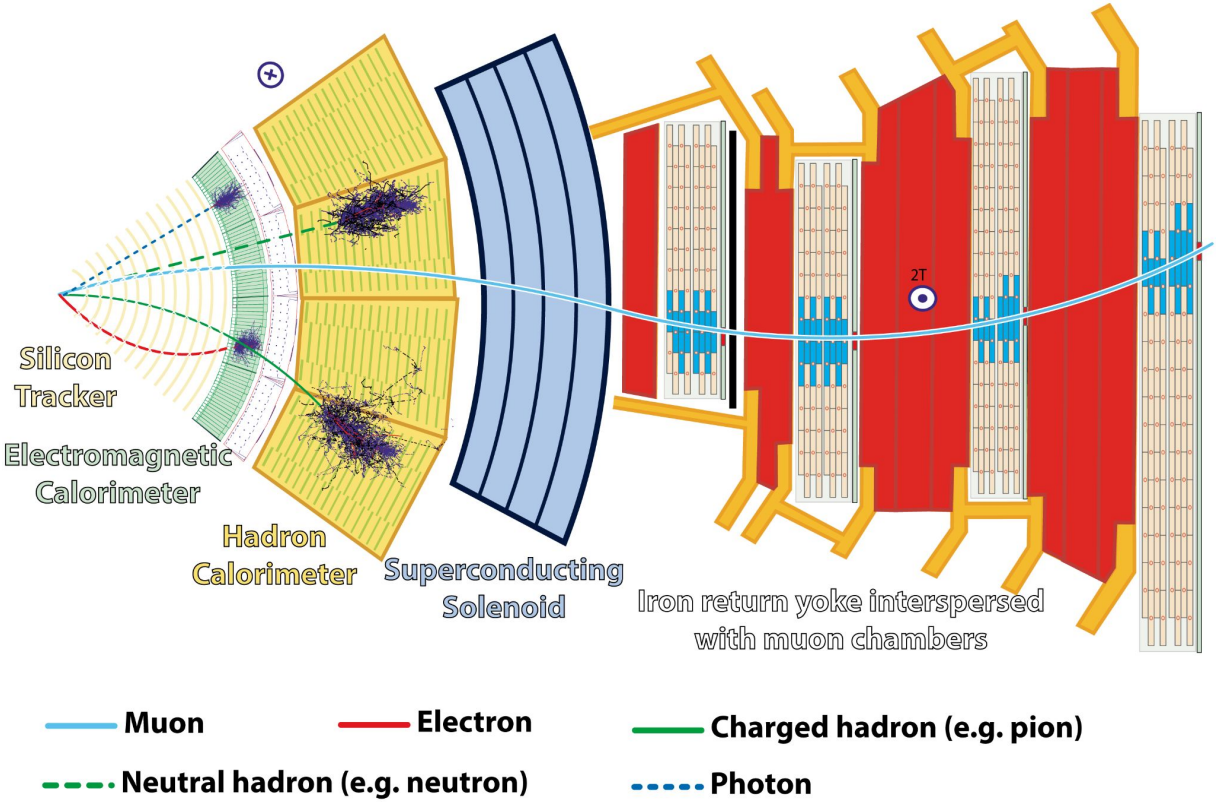


Conclusion

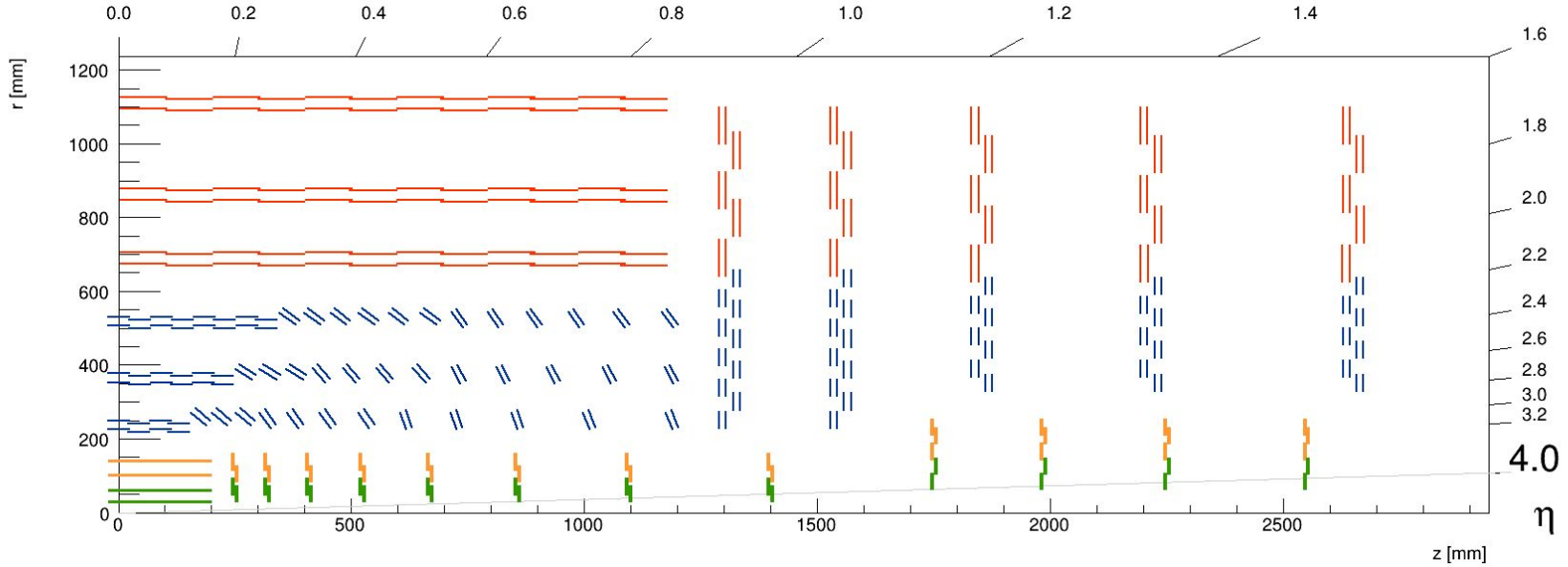
- To achieve the physics goals of CMS during HL-LHC, the addition of tracking into the L1 trigger will be critical
- Many aspects of the project are coming together in preparation for future integration tests
- Extensions to the current algorithm are being considered
    - Displaced tracking + improving electron efficiency

Backup

CMS Detector Diagram



Tracker Layout



L1 Trigger Architecture