# Test system: Inner Tracker hardware

#### Outline

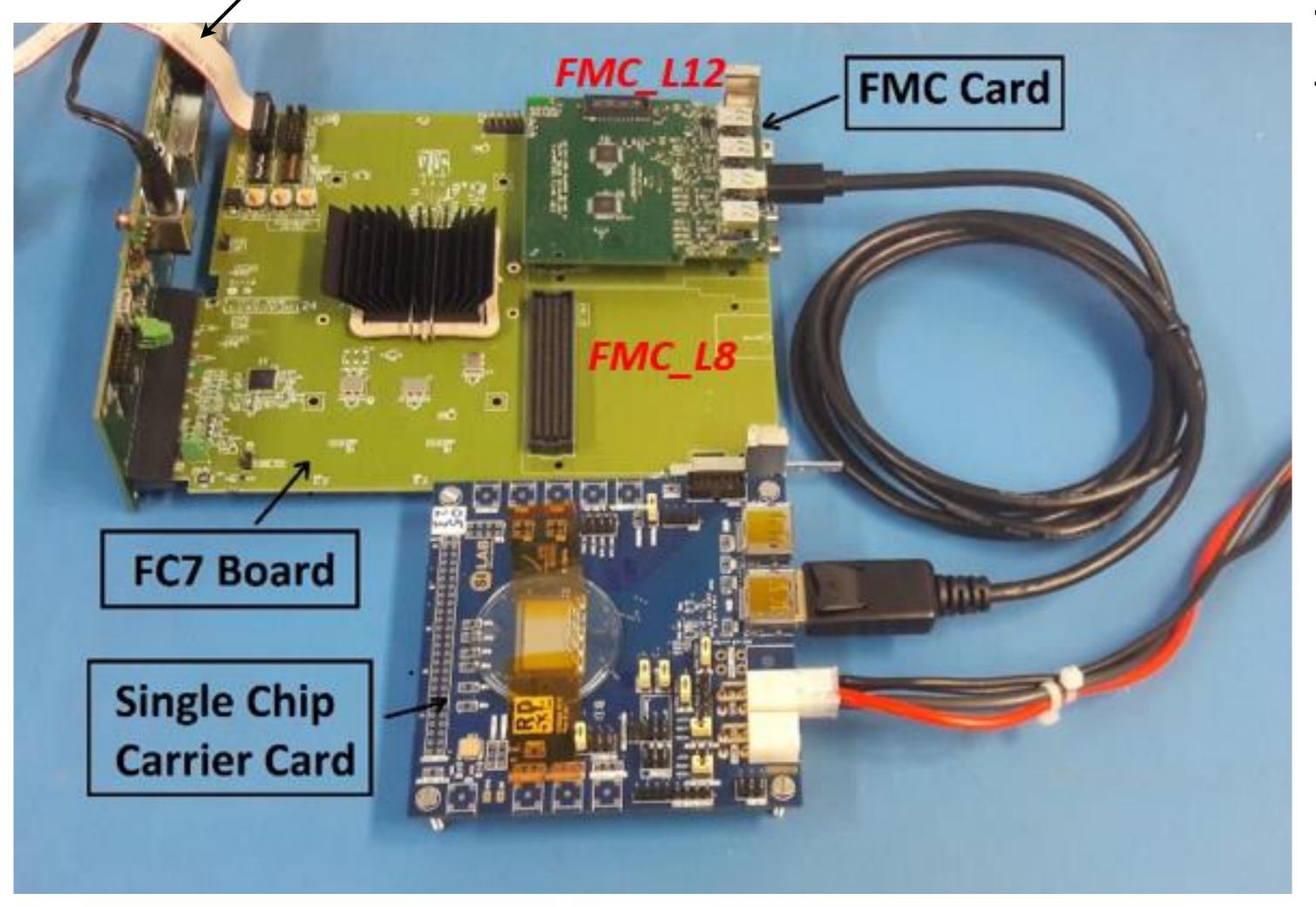
In this presentation I'll try to go through all possible types of hardware and connections which are currently available and supported within the Ph2 ACF software and firmware

Details on the software and firmware can be found on the official gitlab repository: <a href="https://gitlab.cern.ch/cmsinnertracker/Ph2\_ACF">https://gitlab.cern.ch/cmsinnertracker/Ph2\_ACF</a>

#### Electrical readout



SFP connector (ethernet to/from computer)



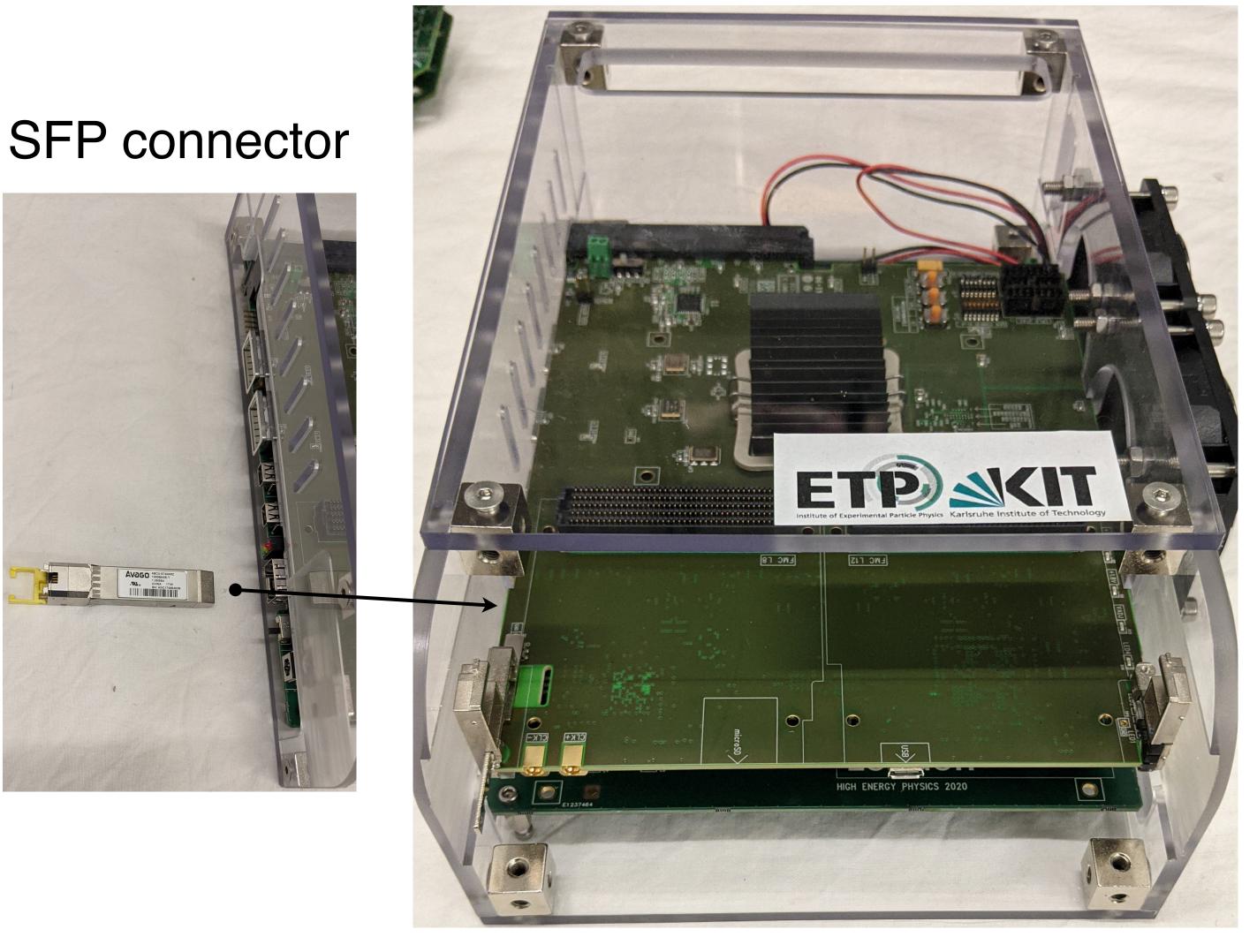
Typical electrical readout for test bench:

- FC7: backend board with FPGA
- FMC board (FPGA Mezzanine Card): needed to interface multi-pins on FPGA to particular readout
- card holding the frontend chip(s)
- connection to the computer: via ethernet cable through SFP connector (Small Formfactor Pluggable transceiver)

#### Electrical readout

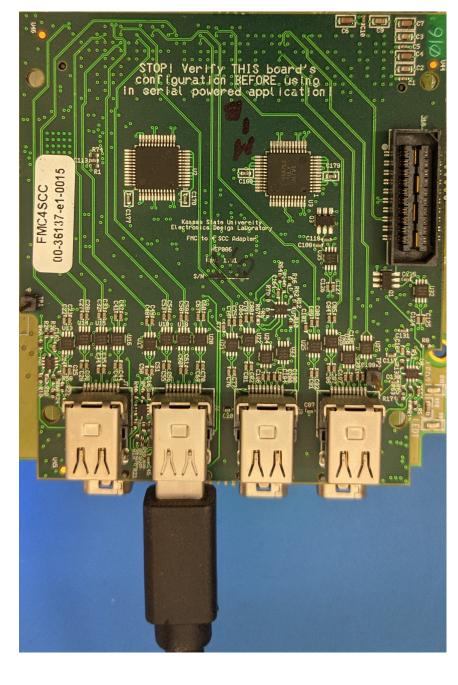
# CMS

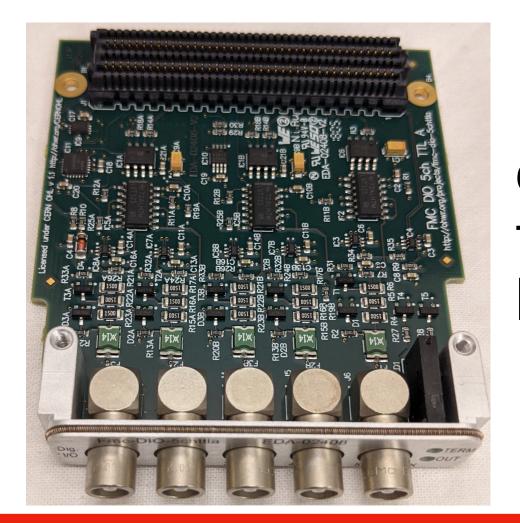
FC7 nano crate (with IC board that provides power)



# Two FMC board supported CERN-FMC KSU-FMC



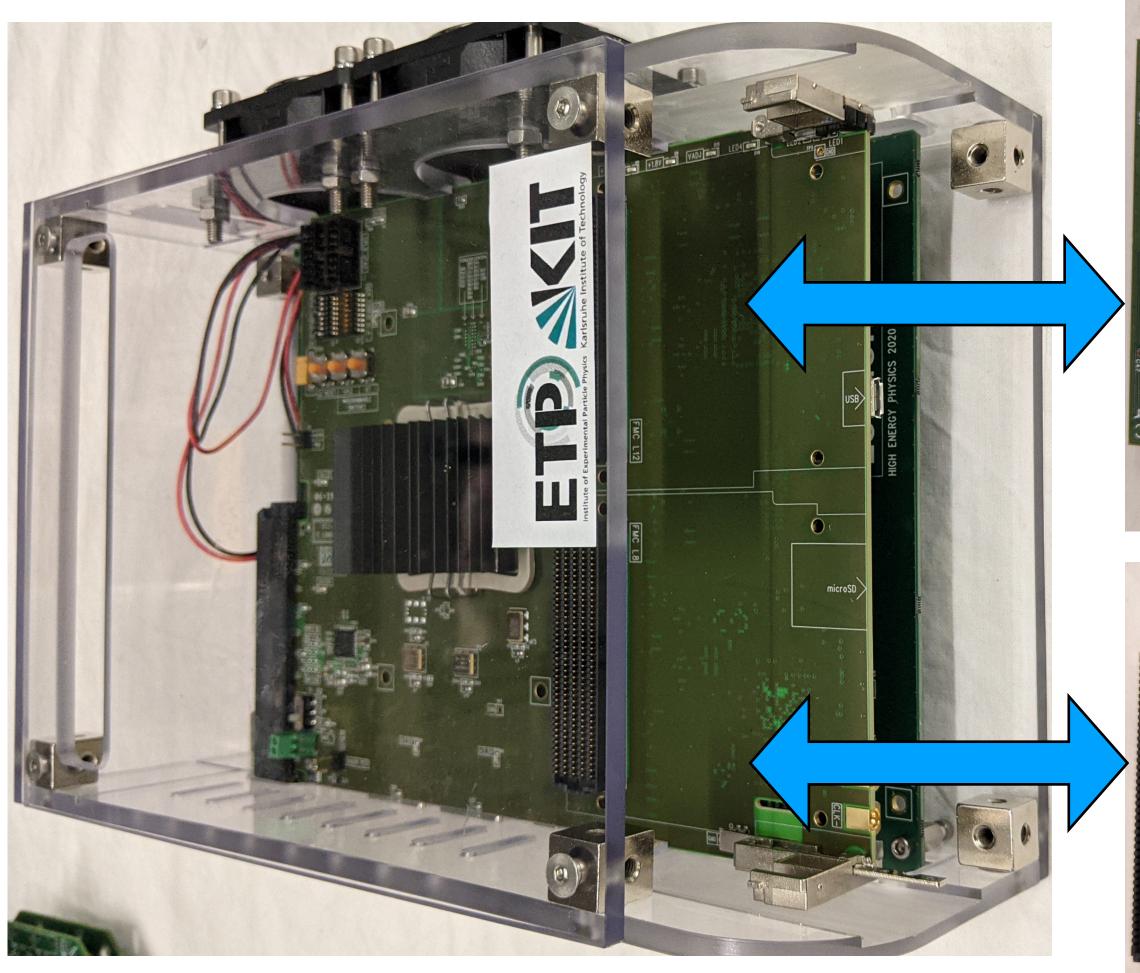




DIO5 to provide ext. clock and trigger, this is also an FMC board

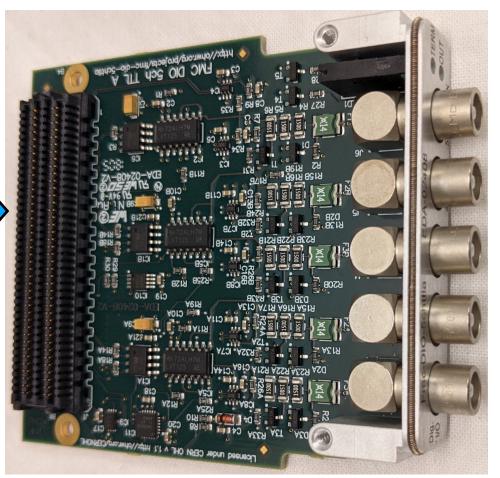
# CMS

# FC7 nano crate (with IC board that provides power)



#### **CERN-FMC**





CERN-FMC

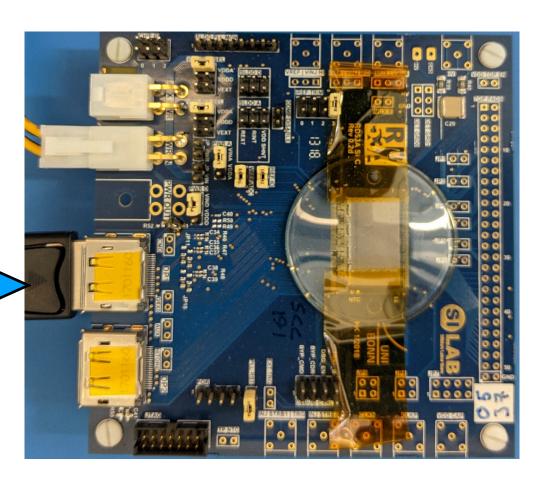
upside down

DP1\_FMC

DP2\_FMC

JTAG

Display Port to Display Port cable

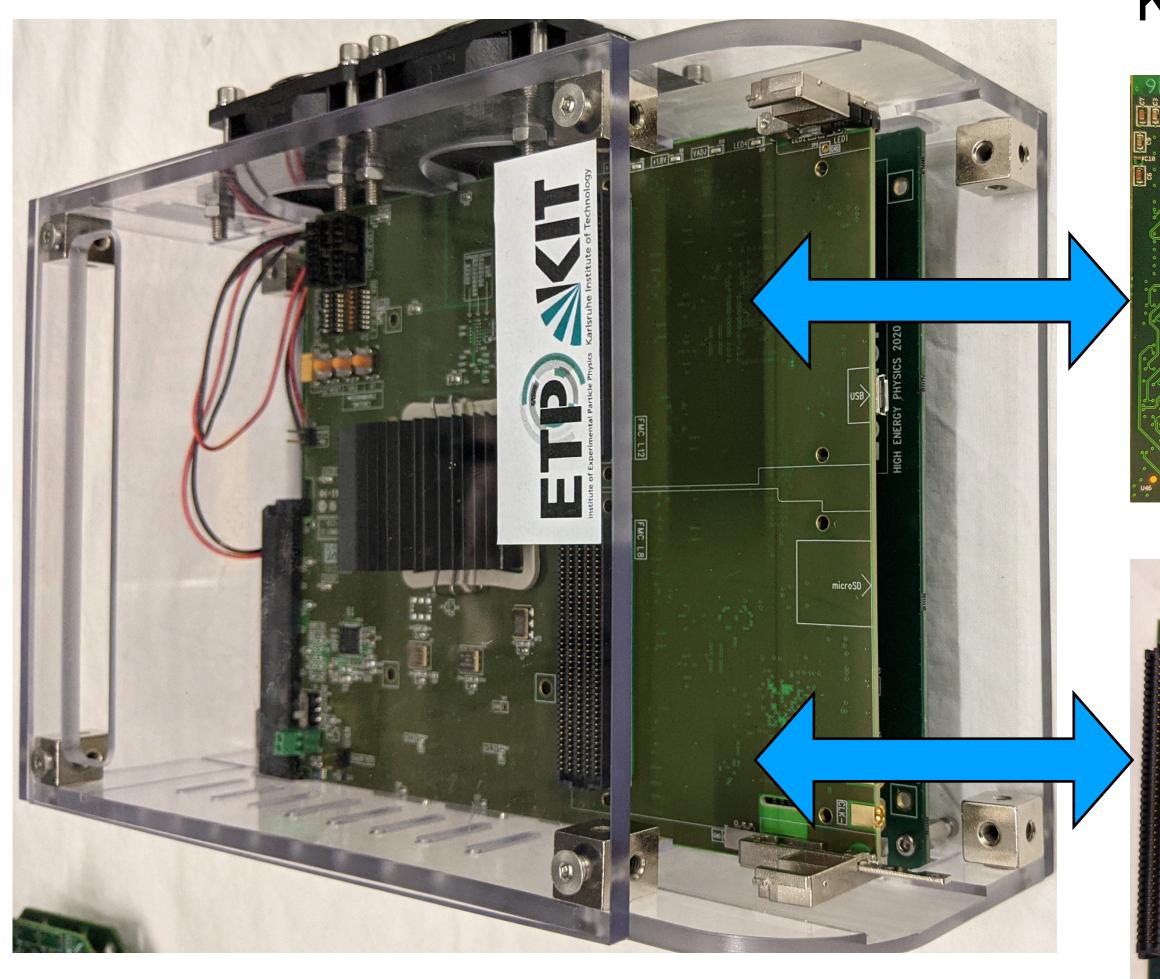


Single Chip Card

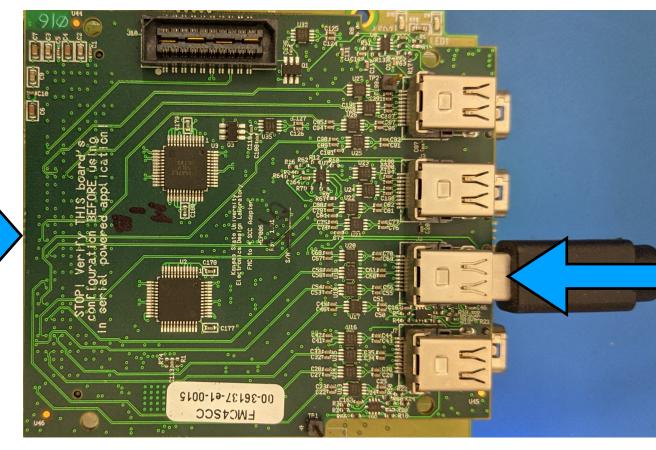
DIO5 (not strictly needed)

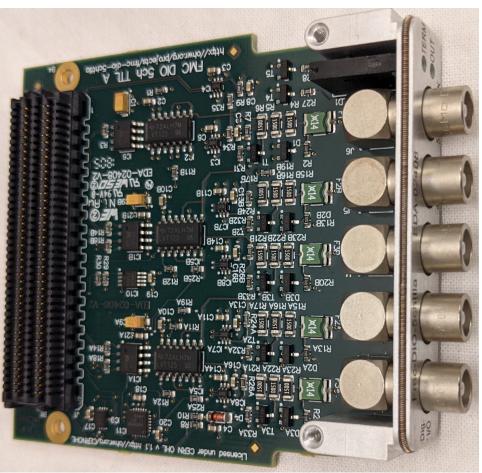


# FC7 nano crate (with IC board that provides power)



#### KSU-FMC



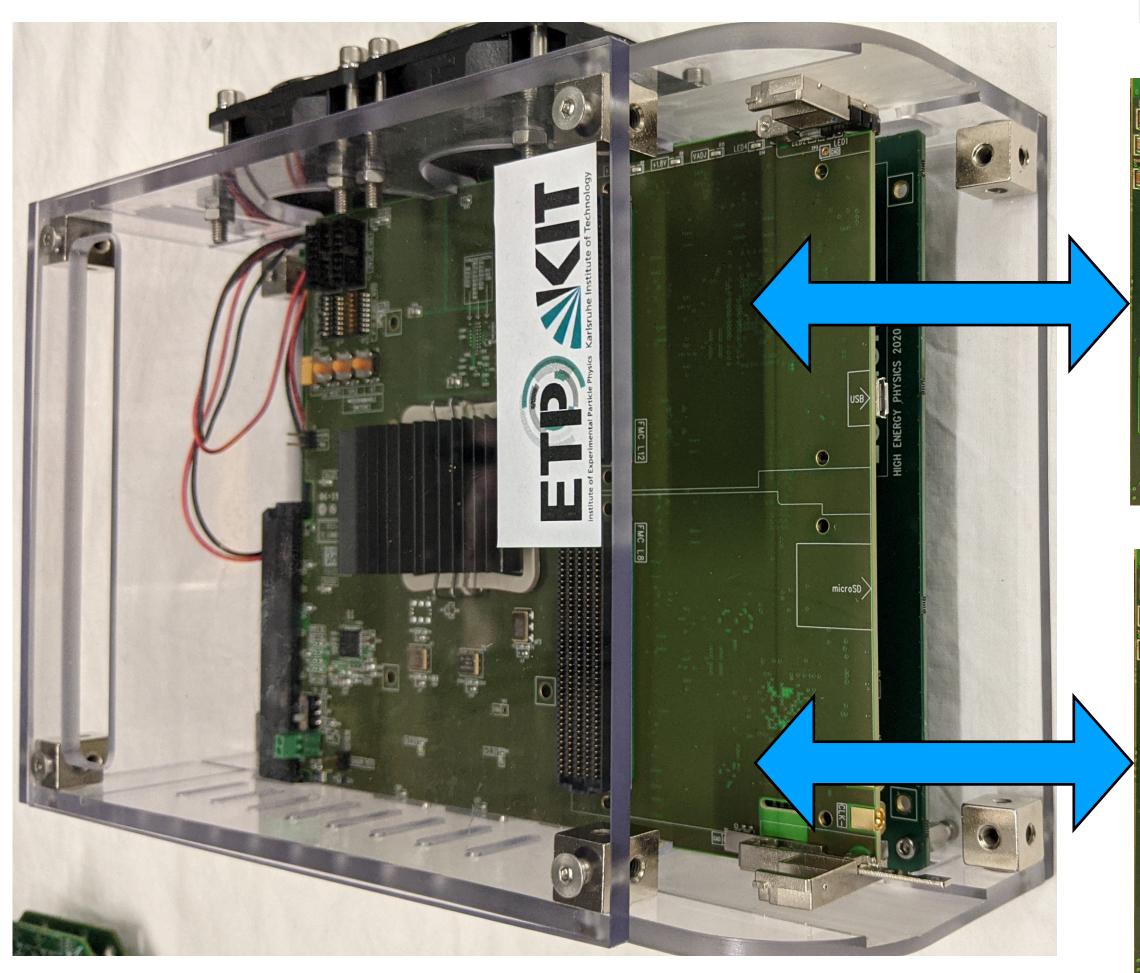


DIO5 (not strictly needed)

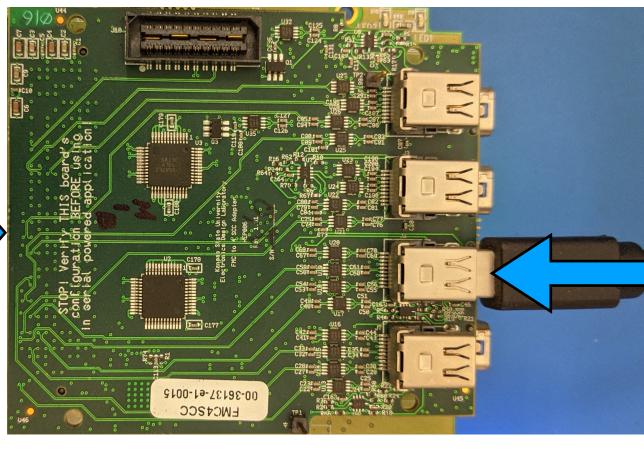
Mini Display Port to Display Port cable to Singe Chip Card or to Quad Modules

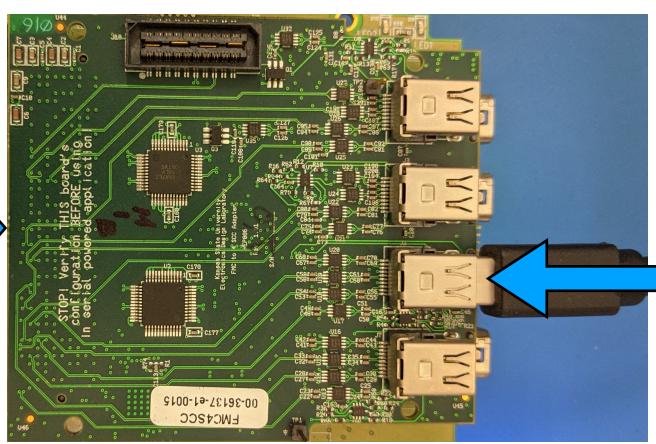
# CMS

# FC7 nano crate (with IC board that provides power)



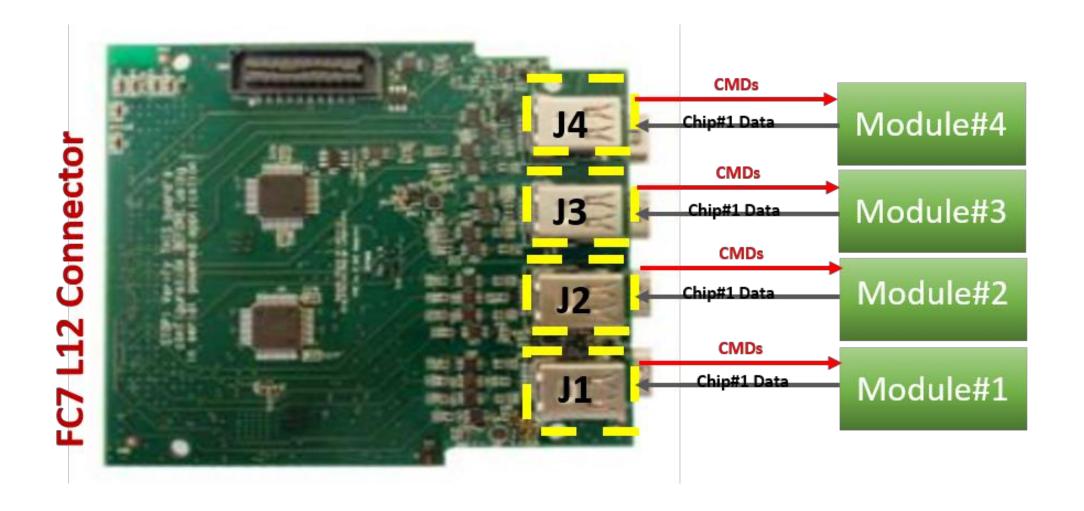
#### KSU-FMC

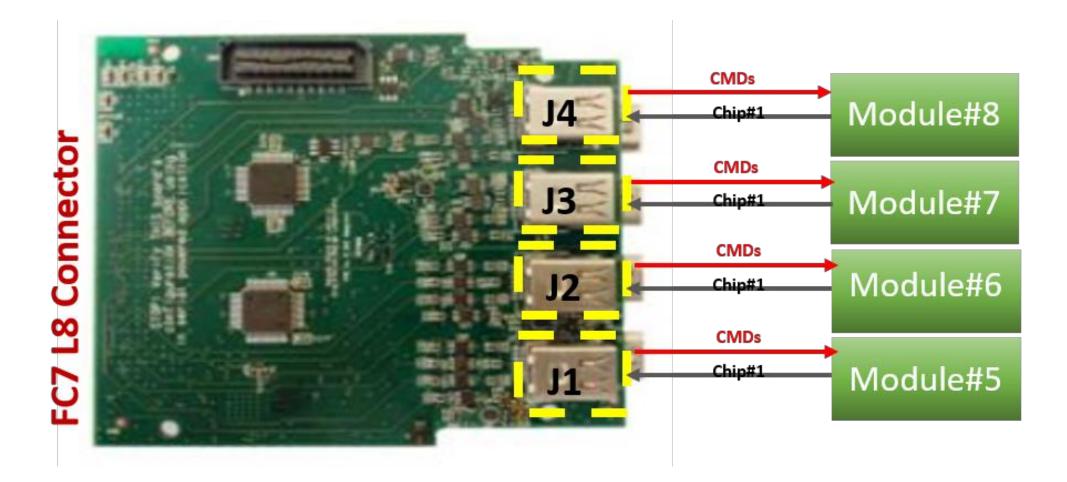




KSU-FMC

Mini Display Port to Display Port cable to Singe Chip Card or to Quad Modules





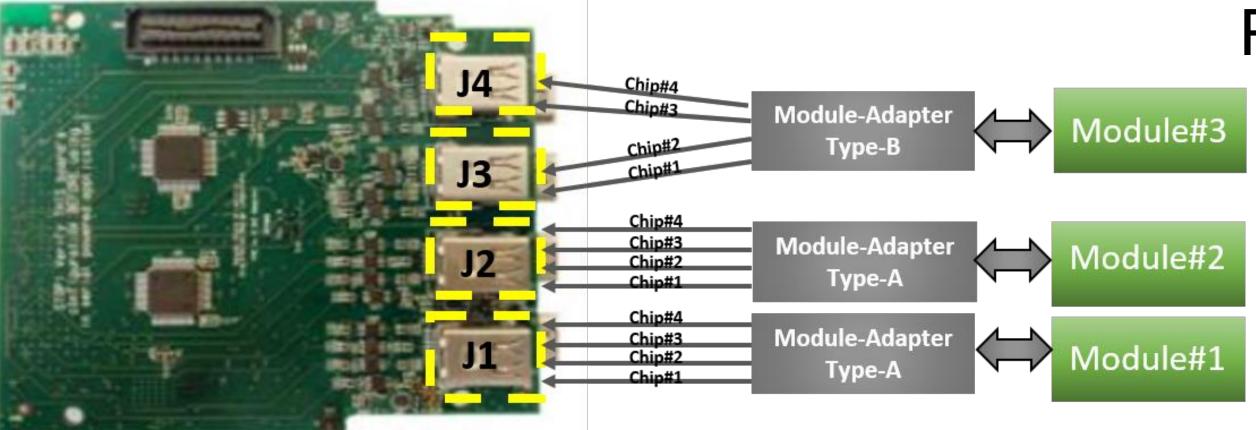
Possible connections to Single Chip Cards

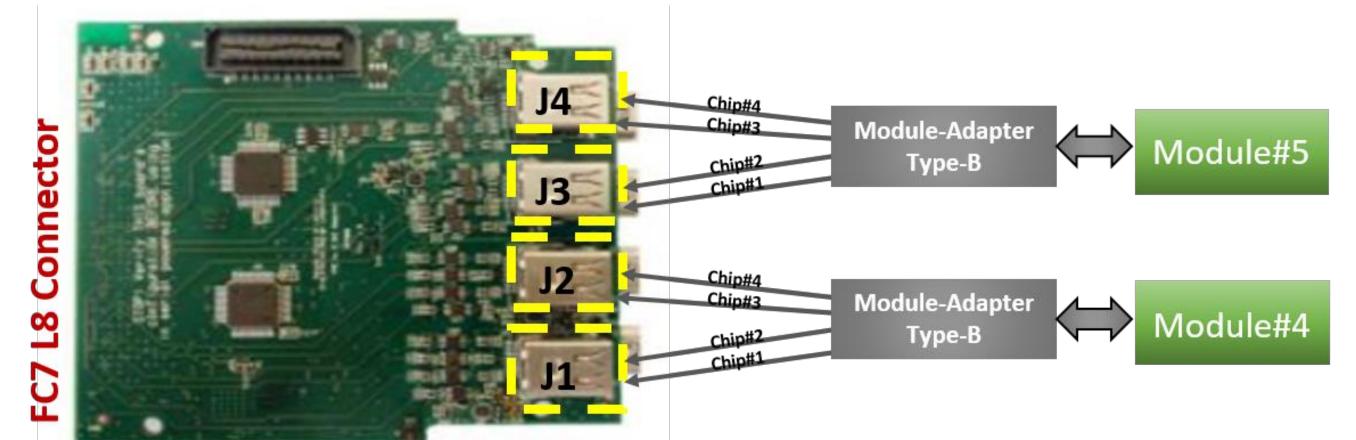
In xml configuration file:

```
<Hybrid Id="0" Status="1">
    <RD53_Files path="./" />
```

Hybrid Id goes from 0 to 7, depending on where you plugged the Mini Display Port

For the CERN-FMC, since it has just one Display Port connector, you just need to use 0 as Hybrid Id





The RD53 Id and Lane need to be configured accordingly to these tables within a module

```
<RD53 Id="0" Lane="0" configfile="CMSIT_RD53.txt">
 <!-- Overwrite *txt configuration file settings -->
 <Settings
```

Possible connections to Quad Modules

In xml configuration file:

Hybrid Id goes from 0 to 4, depending on where you plugged the Mini Display Port

#### **Pixel modules TEPX**

- chip ID 0 <-> lane 0
- chip ID 1 <-> lane 1
- chip ID 2 <-> lane 2
- chip ID 3 <-> lane 3

#### Pixel modules TBPX

- chip ID 4 <-> lane 0
- chip ID 5 <-> lane 1
- chip ID 6 <-> lane 2
- chip ID 7 <-> lane 3

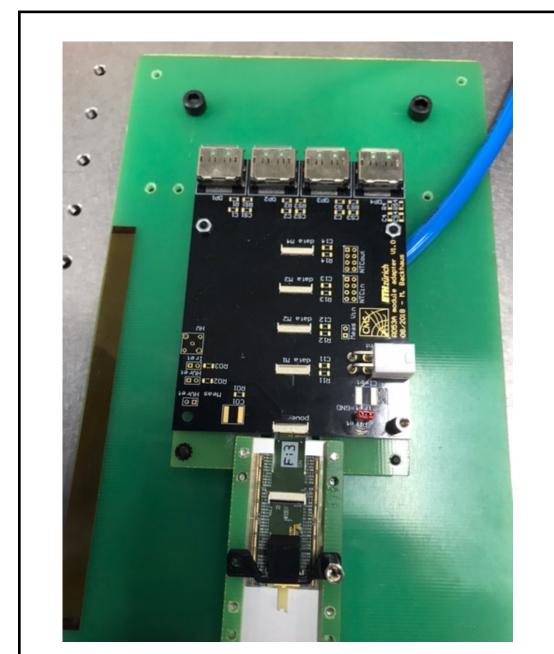
#### Pixel modules TFPX

- chip ID 4 <-> lane 0
- chip ID 2 <-> lane 1
- chip ID 7 <-> lane 2
- chip ID 5 <-> lane 3

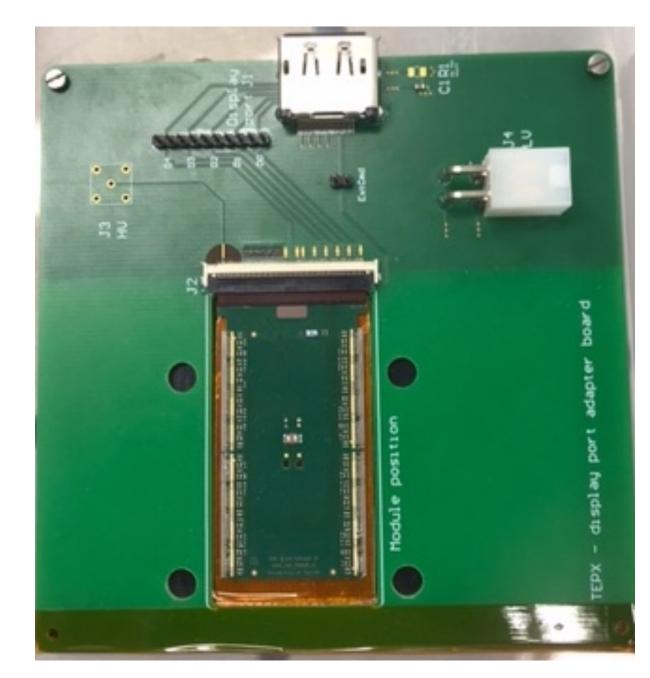
-C7 L12 Connector

# CMS

## Module adapter types







**TEPX Quad Module** 

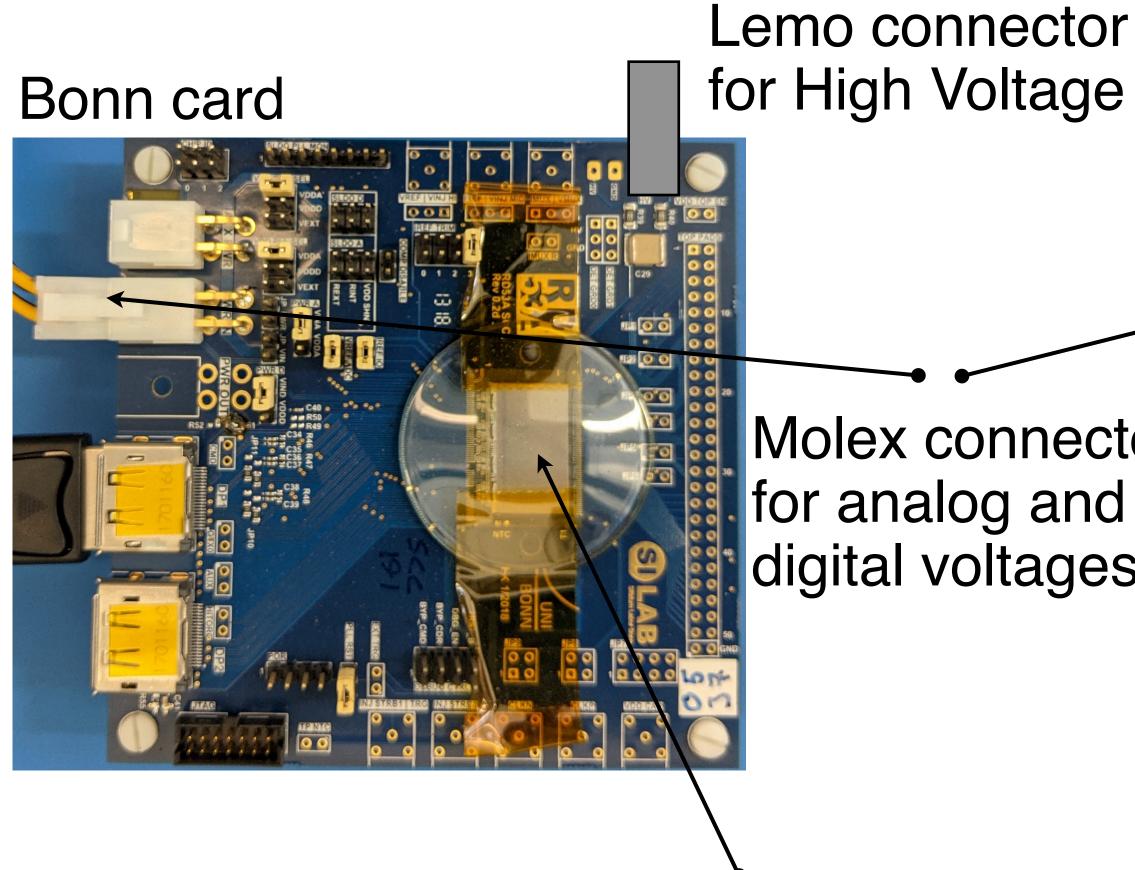


**TBPX Quad Module** 

Power supply for modules: recommended a professional one that can provide ~8A, like Keysight Technologies E3633A

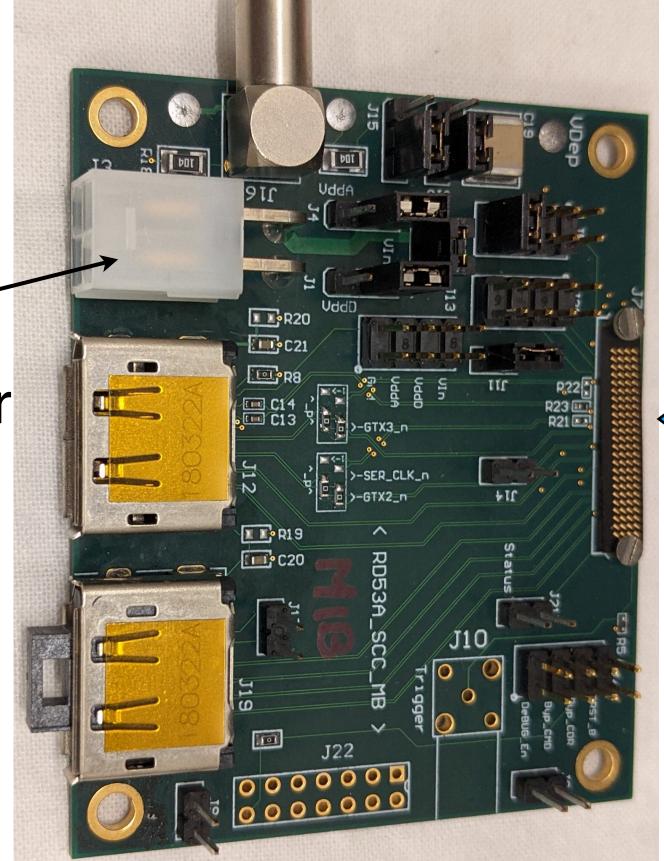
Single Chip Card comes in two flavours: "Bonn card" and "Rice card"

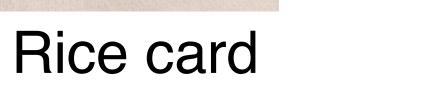
Lemo connector for High Voltage

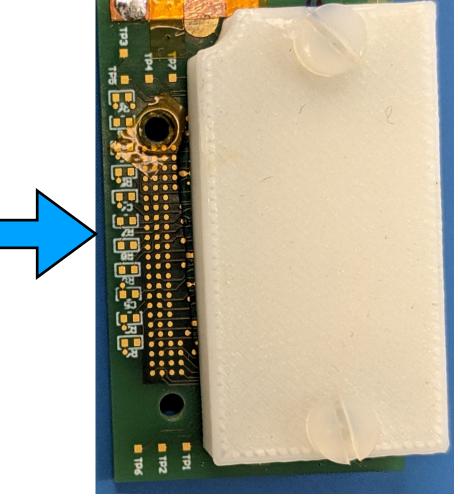


Molex connector for analog and digital voltages

RD53 chip



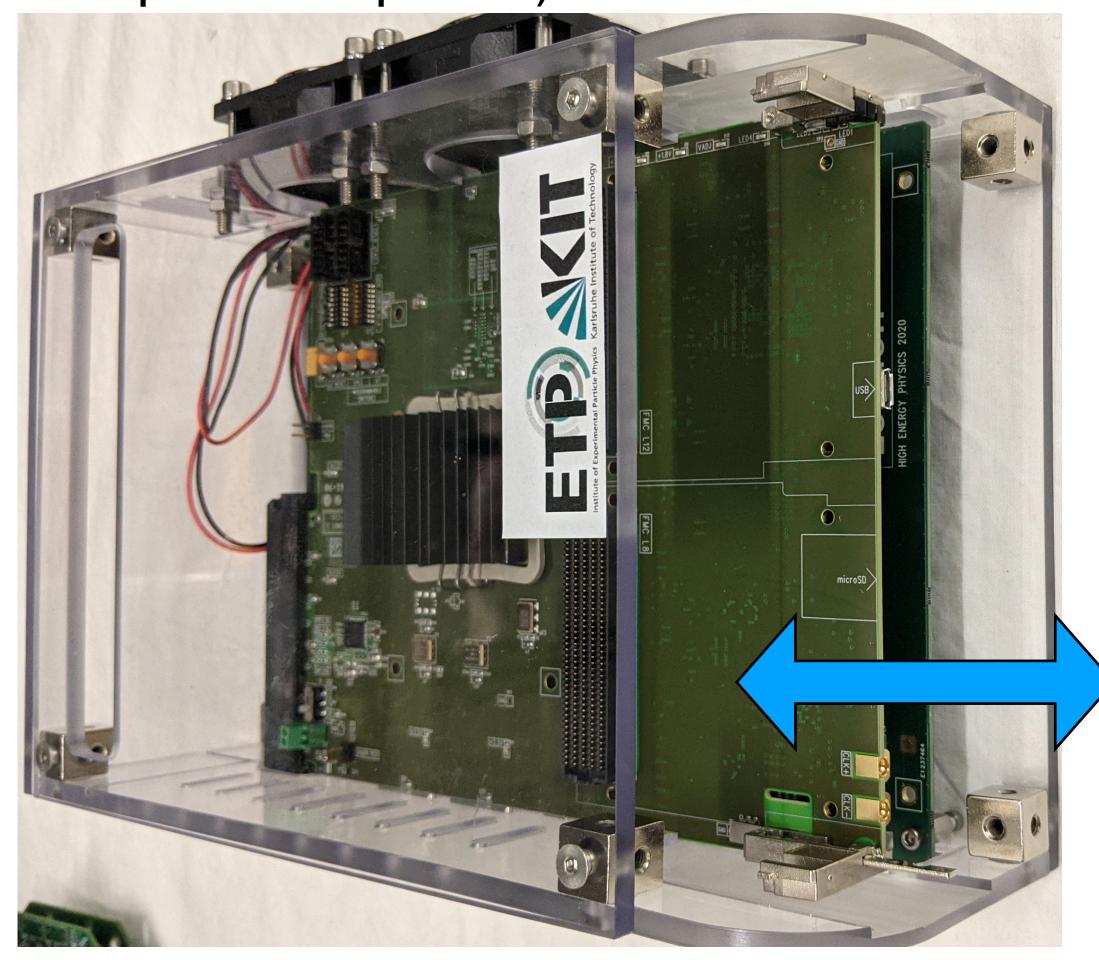




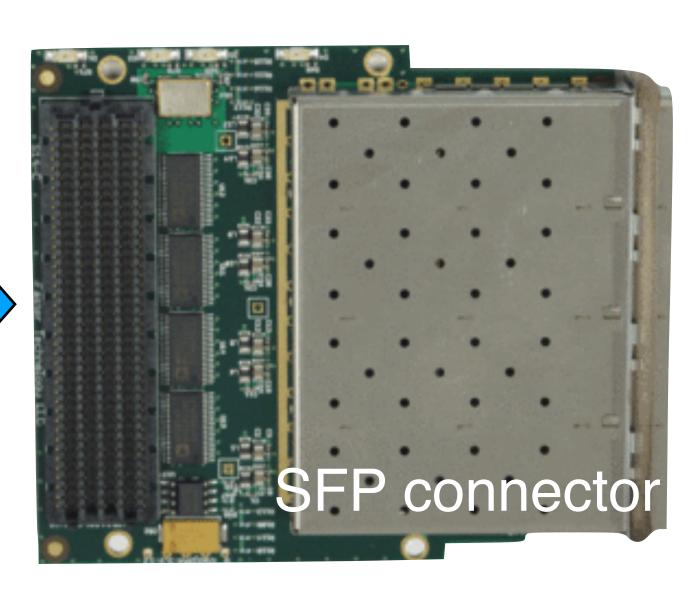
RD53 chip

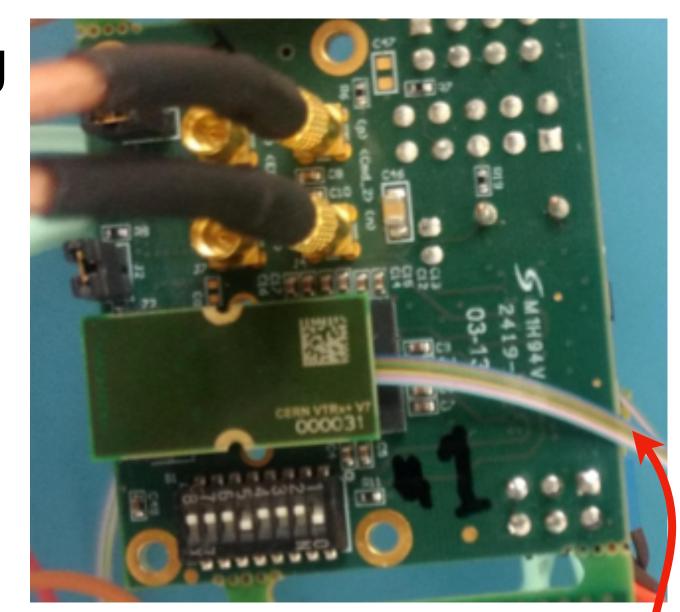
### Optical readout

FC7 nano crate (with IC board that provides power)



Portcard mounting LpGBT chip (Low power GigaBit Transceiver)

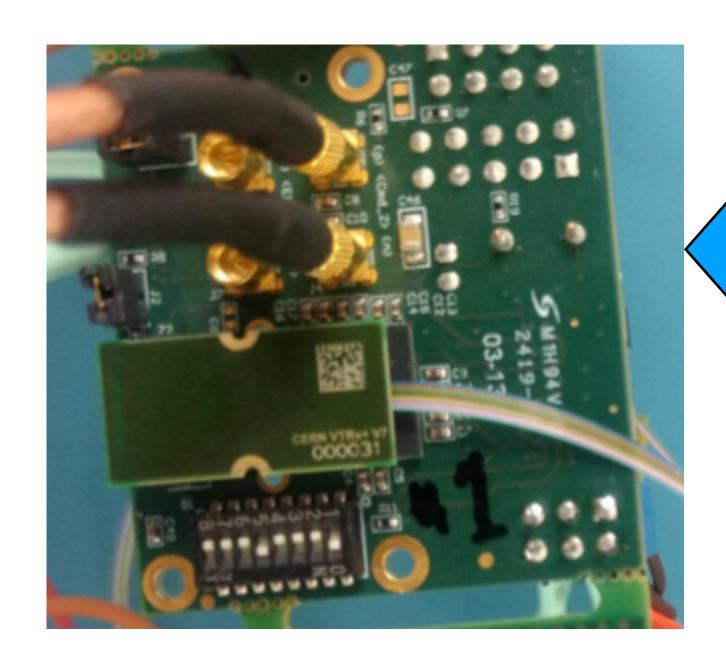




Optical fiber

## Optical readout





Portcard mounting LpGBT chip (Low power GigaBit Transceiver)

MMCX to SMA cable





Adapter board

# Single Chip Card



Display Port to Display Port cable

#### Commercial parts

- DIO5 FMC board (https://www.ohwr.org/project/fmc-dio-5chttla/wikis/home)
- Power supply for FC7 (12 V 6 A)
- Electrical SFP connector (suggested: ABCU-5740ARZ)
- Optical SPF connector (suggested: FS-10GSR-85)