Inner Tracker System

March 2021

Inner tracker Phase 2 requirements

Objective:

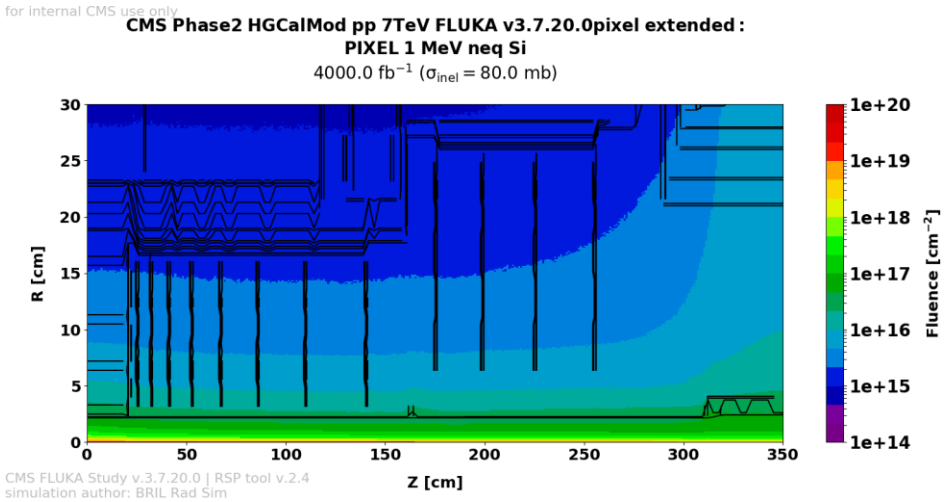
Maintain or improve tracking capability with:

Pile-up 200

Hit Rate >3.2 GHz/cm²

Trigger latency 12.8 us

Unprecedented radiation levels



Innermost layer: 3.5 x 10^{16} n_{eq}/cm^2

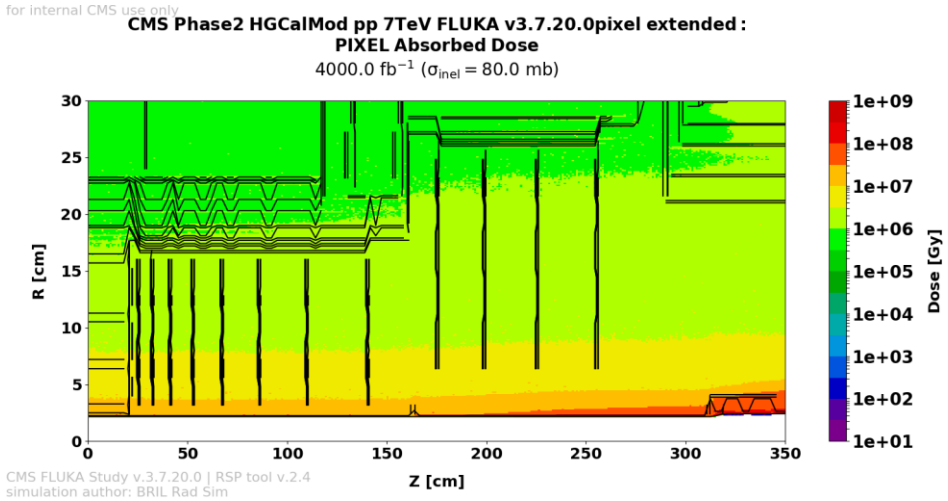
Increased granularity (25x100 um² or 50x50 um²)

Increased detection coverage (|η|≤ 4)

Reduced material budget (light mechanics, services)

Lower detection threshold (new readout chip)

Simple installation and removal

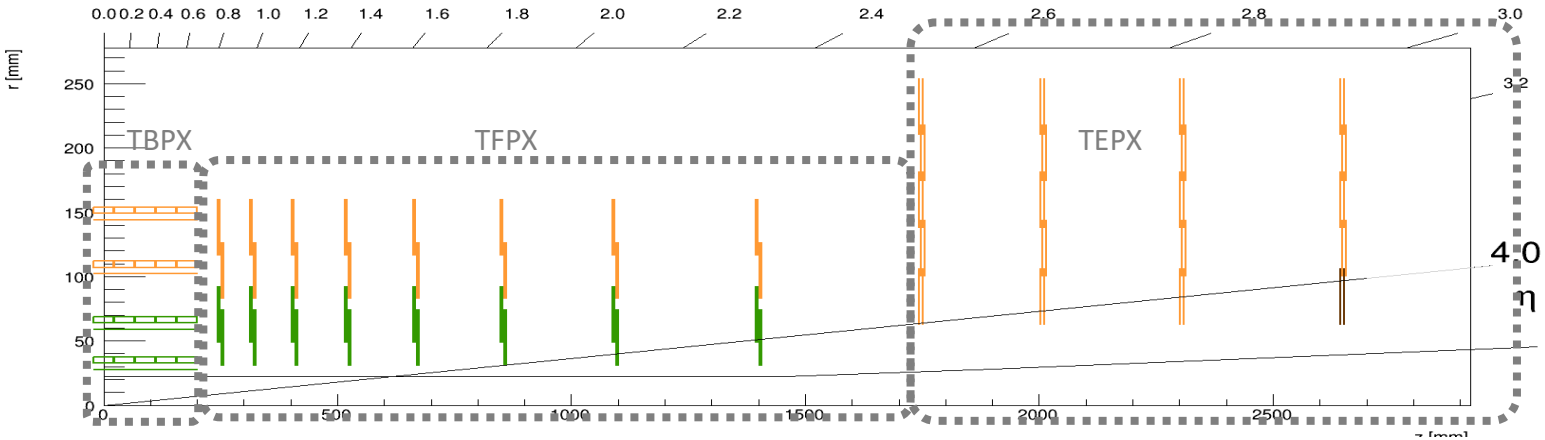


Innermost layer: 1.9 Grad

Inner Tracker Layout: Extension to |η|= 4

Hybrid technology

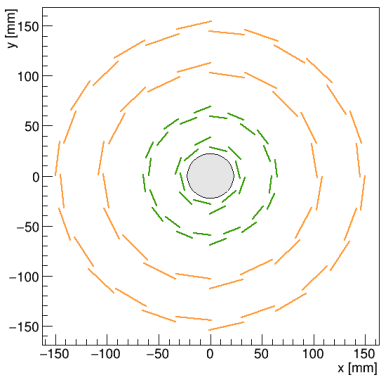
Total active surface of ~4.9 m^2



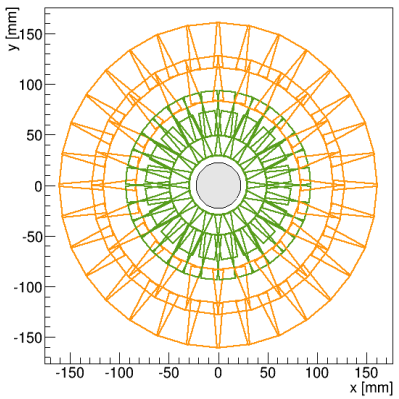
Green for 1x2 modules

Orange for 2x2 modules

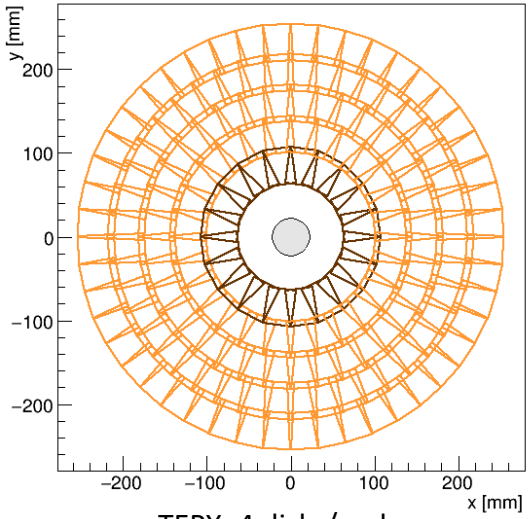
Brown for TEPX D4R1 BRIL



TBPX: 4 layers
4/5 modules per ladder



TFPX: 8 disks/end
4 rings/disk

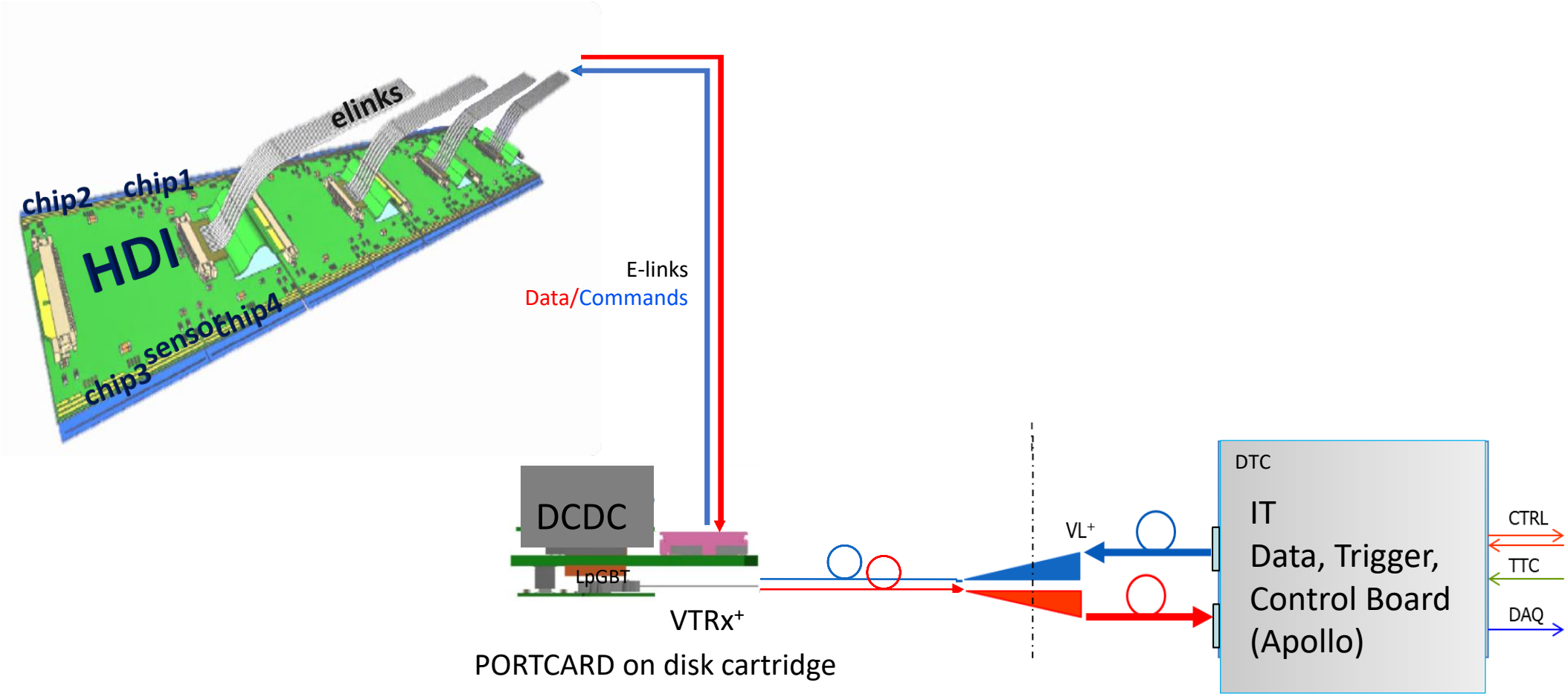


TEPX: 4 disks/end
5 rings/disk

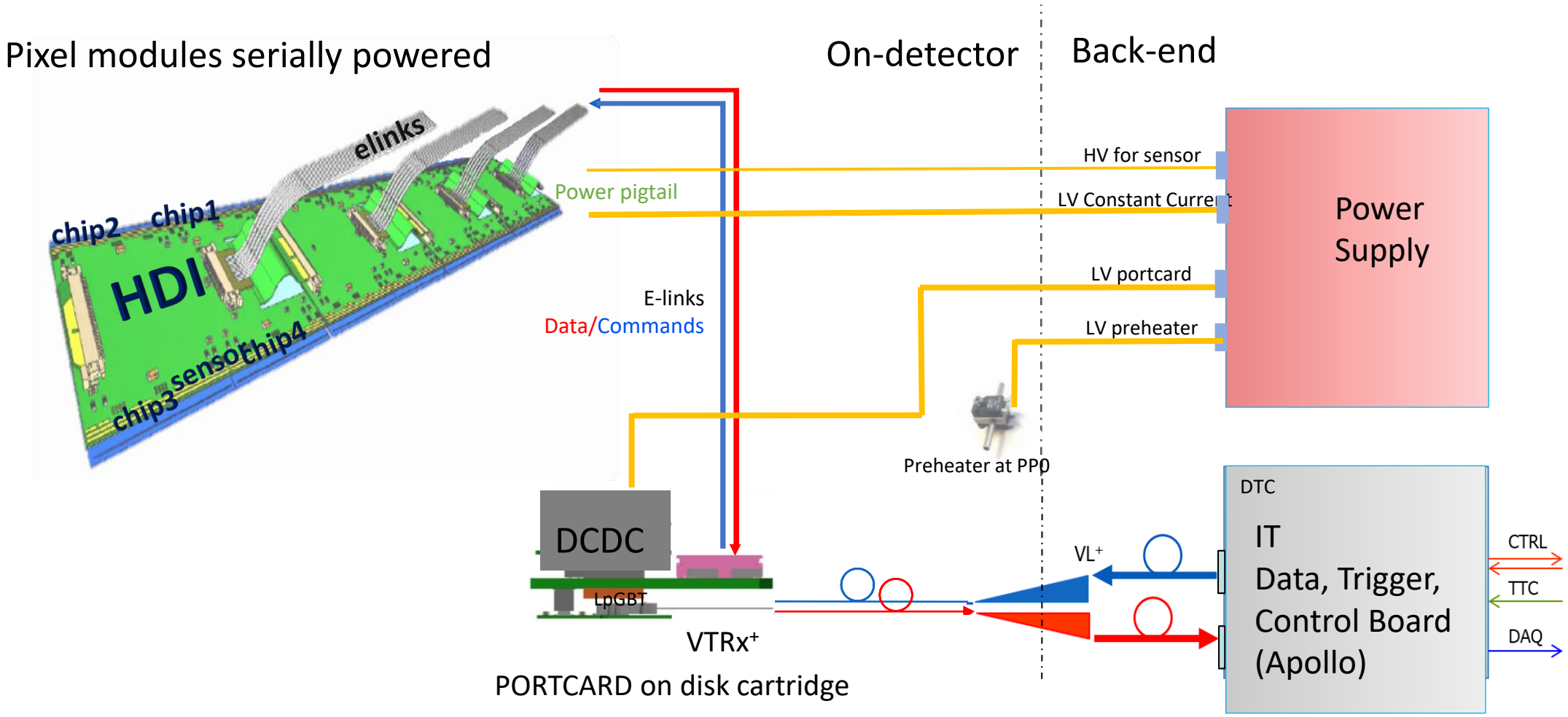
TEPX is a large and powerful luminometer and will receive extra lumi triggers.

First ring of the last disk is fully dedicated to lumi and background monitoring, with independent readout and control.

Pixel Electronics System



Pixel Electronics System



System Architecture: Power

Serial powering is the only viable solution for the IT system ~50 kW on-detector power

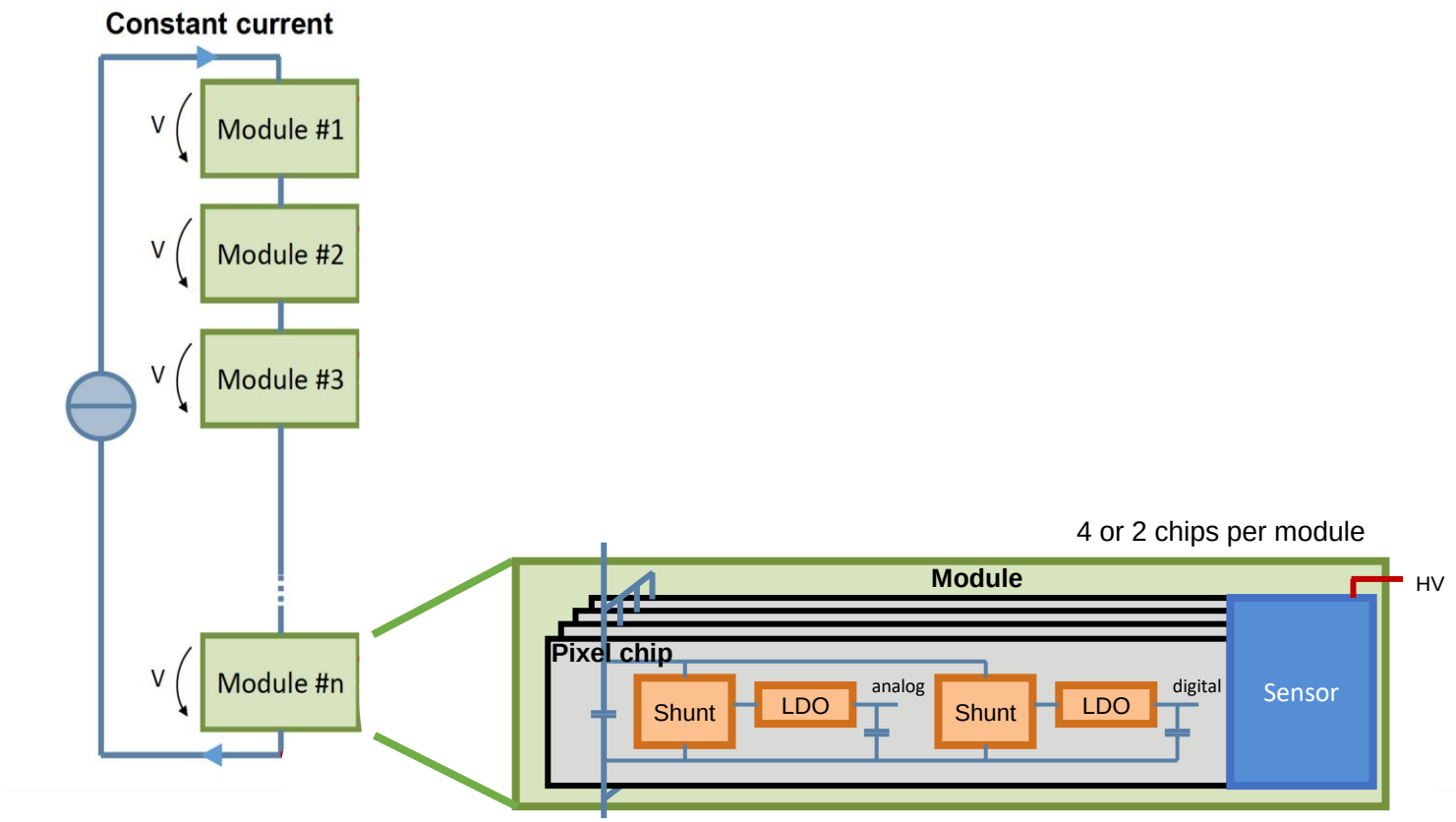
- ✓ Low mass- Integrated on-chip solution
- ✓ Radiation hard

I_{in} constant, enough Iin to satisfy highest I_{load}.
Any extra current gets burnt by shunts.

Input current shared among chips.

Electronics system is segmented in power chains.

No crossing of readout or sensor bias is done among modules of different chains.



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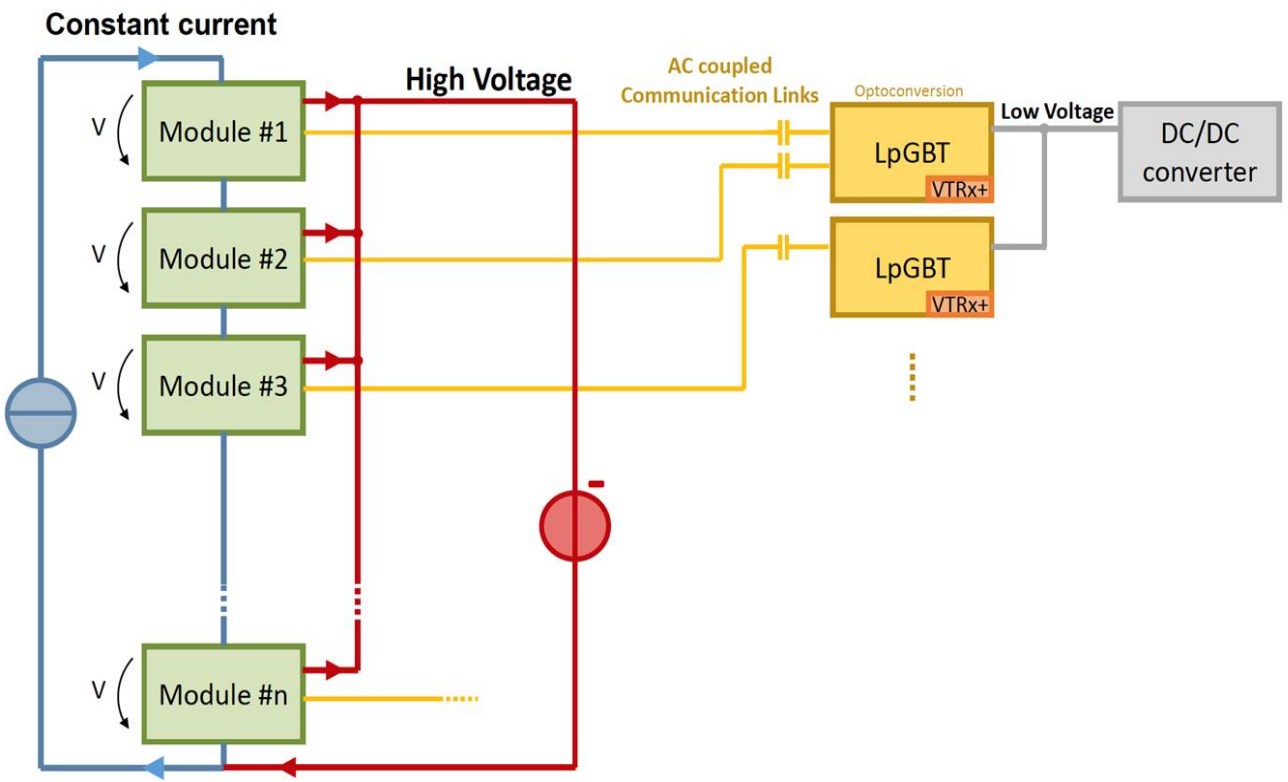
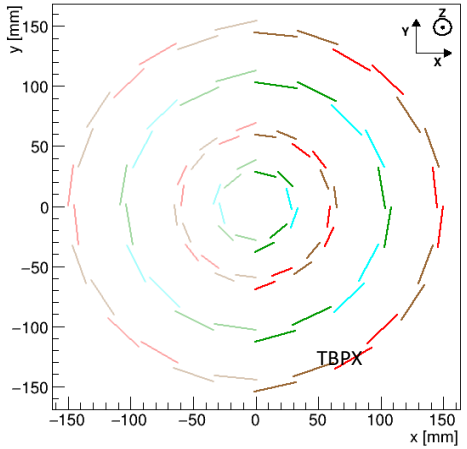


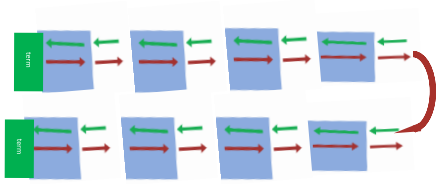
Serial Powering: Max 12 modules/chain

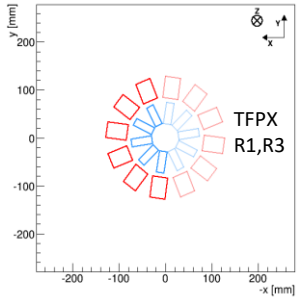
Up to 12 pixel modules serially powered
500 Serial power chains
20% current headroom for stable operation

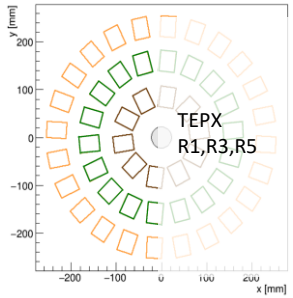
TBPX:
1 chain for 2 consecutive ladders in Phi
8 or 10 modules/chain.

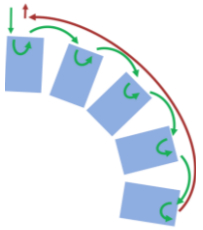
TFPX/TEPX:
1 chain(s) per (X) side /(Z) side of a ring.
5 to 12 modules per chain

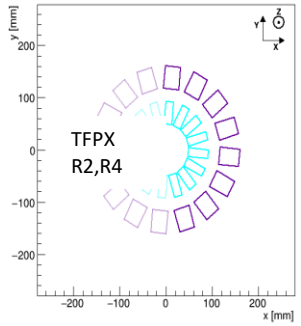


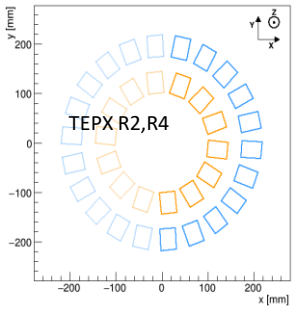




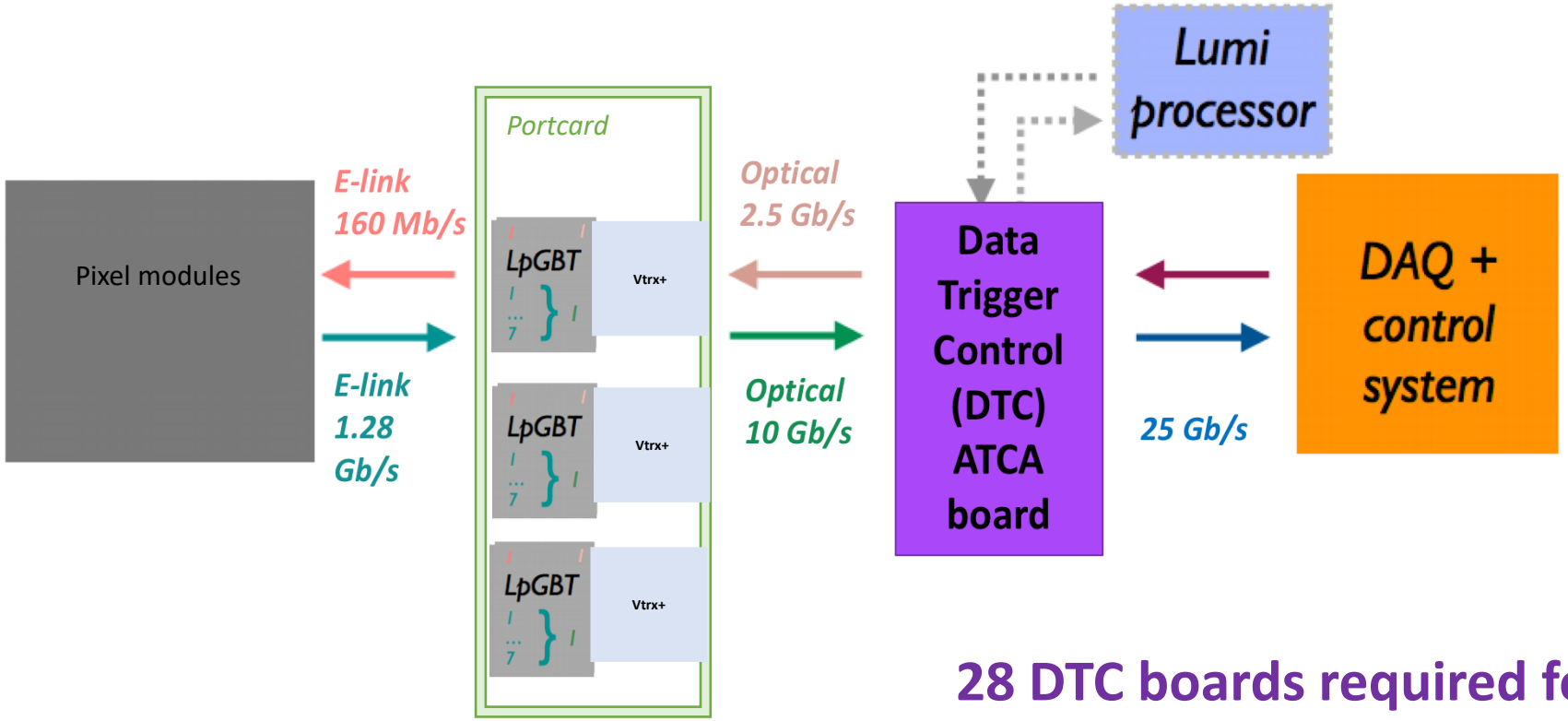








High Bandwidth Readout chain



28 DTC boards required for CMS IT

Inner Tracker

Service Cylinder

Counting Room

High Bandwidth Readout chain: Elinks

~7k readout + 4k control differential electrical links (e-links) for entire system

Various e-link options investigated:

Flex, twisted pair: 0.5 – 1.8m

Objective: Minimize mass for acceptable cable losses

Up to 6 electrical up-links @1.28 Gb/s per module to LpGBT

Data from L1 accept, monitoring info to DAQ, control system

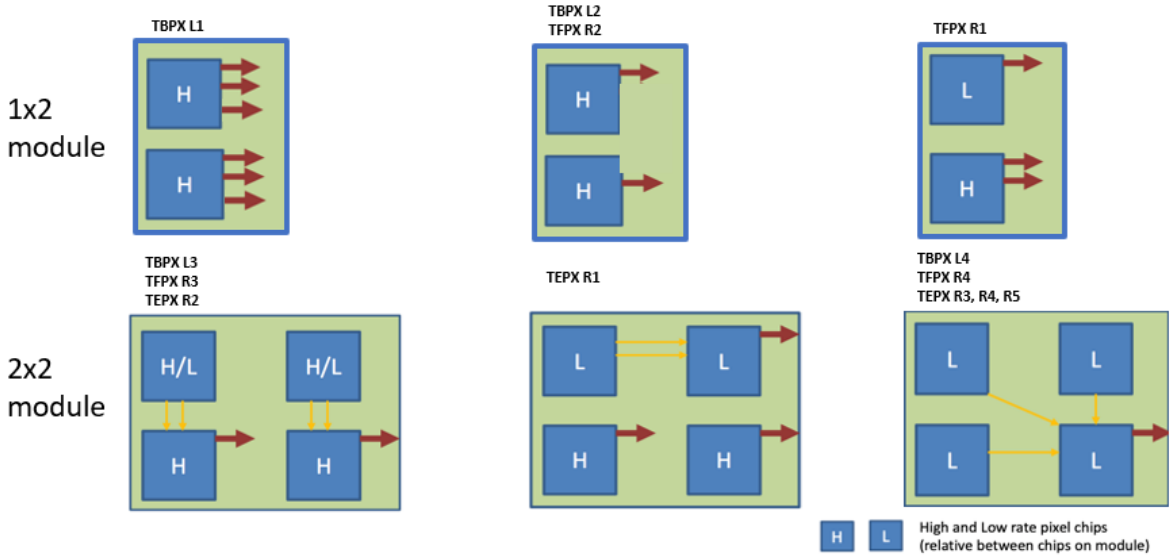
Efficient data formatting to reduce data rates (factor ~2)

25% bandwidth headroom on e-link occupancy

One electrical down-link @160 Mb/s per module from LpGBT

Clock, trigger, commands, configuration data to modules

#Readout links VS module location



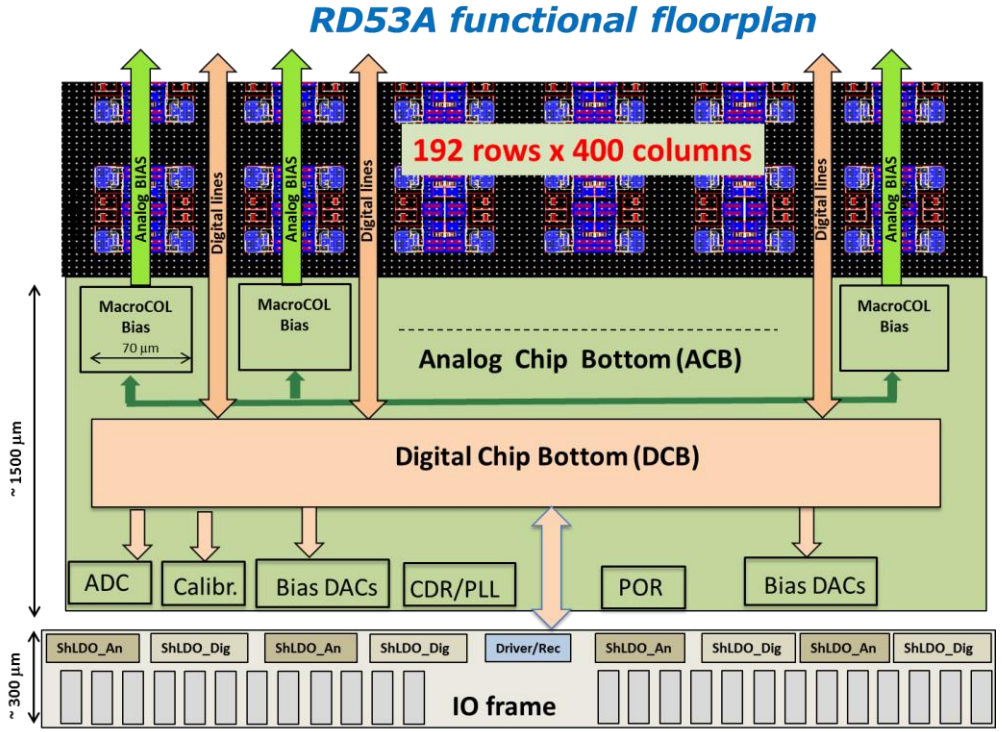
Next generation pixel chip: RD53 chip

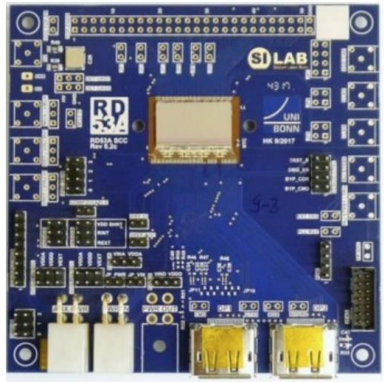
Developed by RD53 collaboration (ATLAS & CMS)
65 nm CMOS technology
Analog islands In a digital sea
Designed to be radiation hard up to 500 Mrad

RD53A chip (~ ½ size of final chip) features:
50 x 50 μm^2 pixels
3 Analog Front-End for low threshold operation (<1ke-)
2 digital architectures
Analog chip Bottom featuring ADC, PLL, Bias DACs

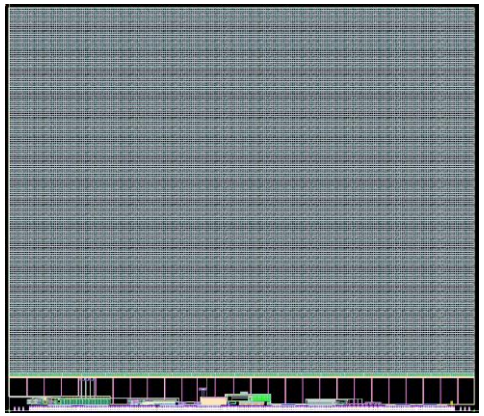
Current status:
Chip is fully functional
RD53A is meeting specifications
Linear Front-End chosen for CMS readout chip 2020
Core design of RD53B common for the two experiments – ATLAS chip submitted in 2020

Next milestone:
About to submit CMS Readout chip (CROC)





RD53A Single Chip Cards (SCC)



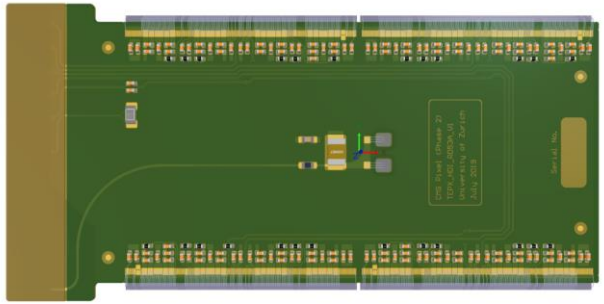
CROC floorplan
Size (including seal-ring): 21.6 mm x 18.6 mm

Pixel Module development

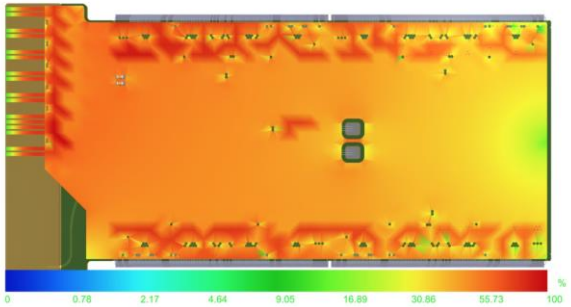
High Density Interconnect (HDI) contains only passive components (routing of signals, power, bias)

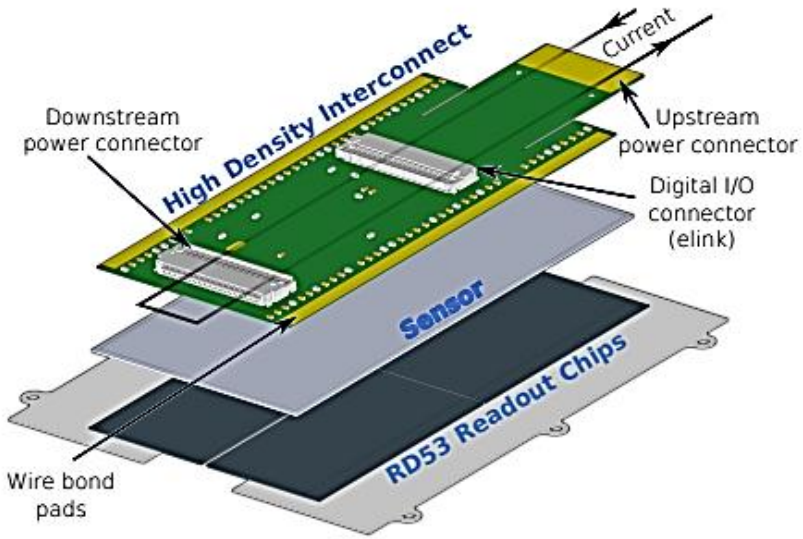
Development of module design, assembly tools and procedures is ongoing

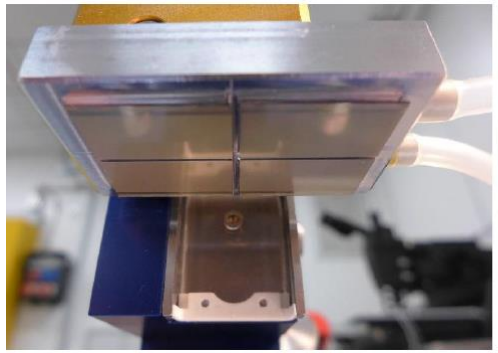
HDI for 2x2 and 1x2 RD53A modules available and operational
Digital modules (no sensor) used extensively in system tests
First RD53A modules with sensor arrived in 2020

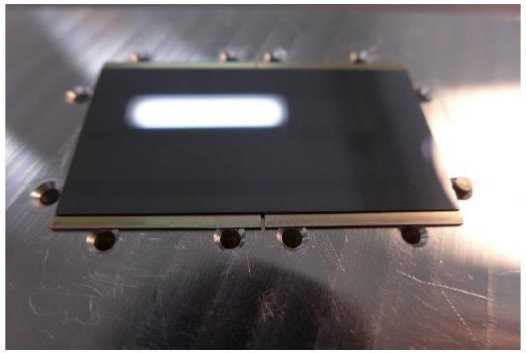


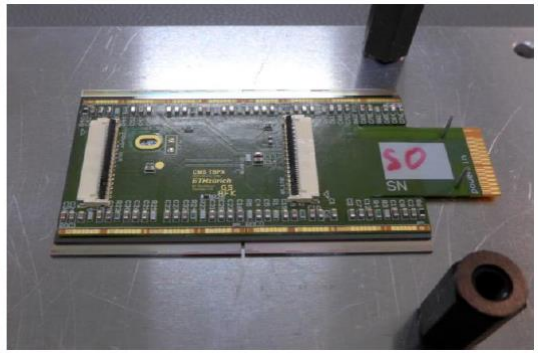
Current density in the middle HDI layer: return line







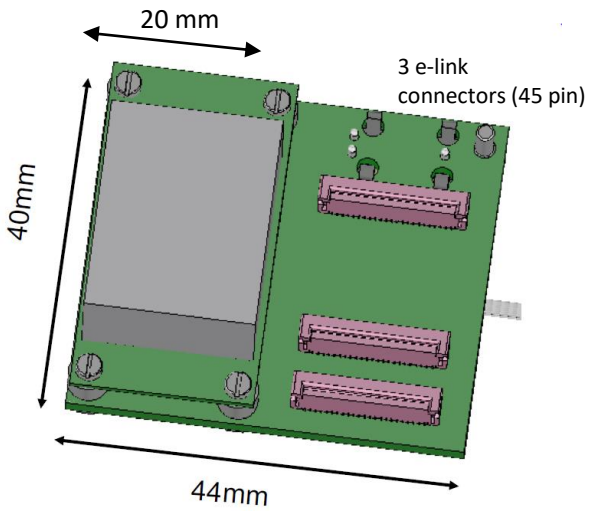


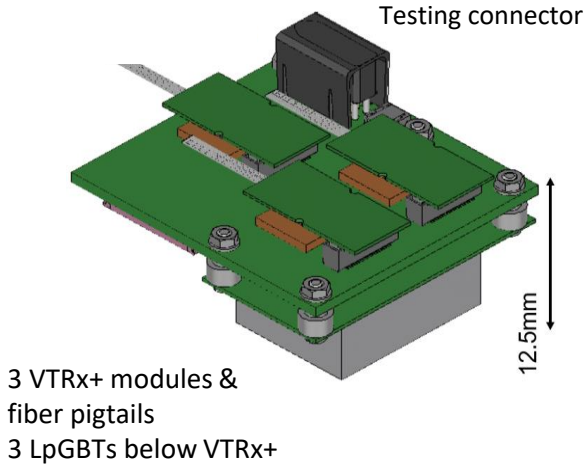


Portcard development

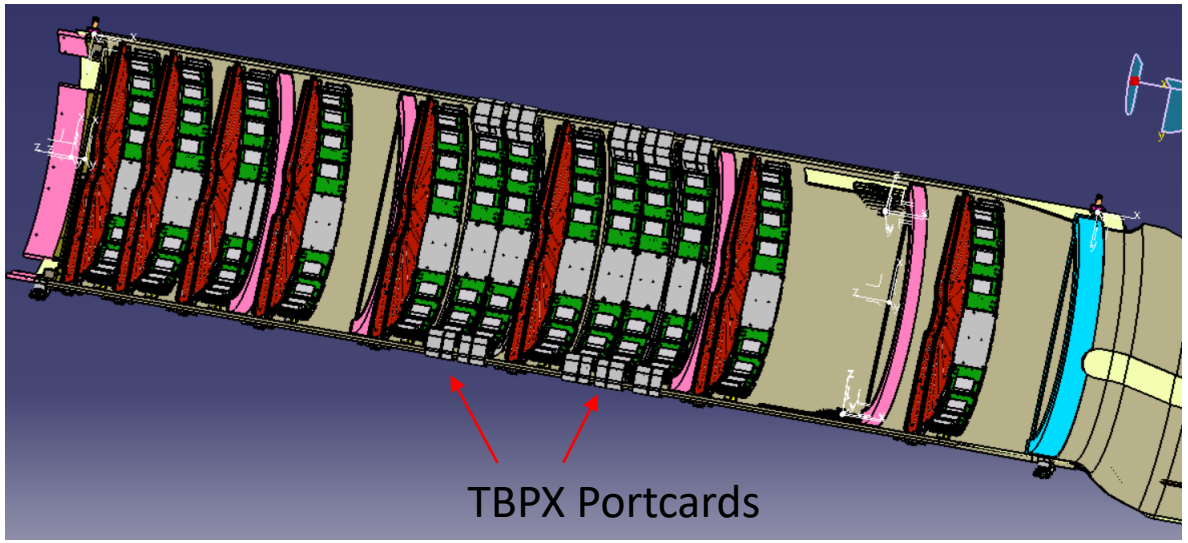
552 portcards to readout/control CMS IT

Portcard designed in 2020:
3 Kyocera 6841 elink connectors
3 Low-power Gigabit Transceiver (LpGBT)
3 Versatile Link+
powered by a mezzanine with a pair of cascaded DC-DC converters (similar to OT powering scheme)



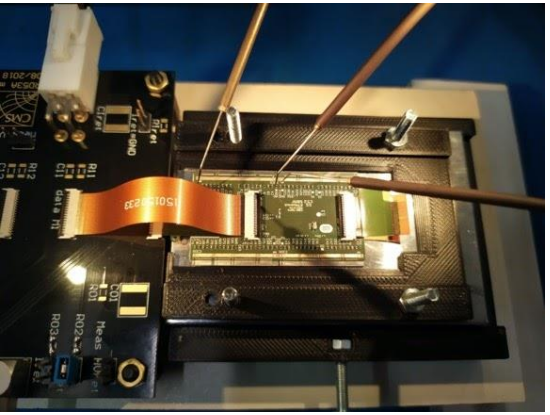


Demo Portcard (2019)
2 elink connectors
1 LpGBT
1 Versatile Link+
Extra I2C connector for lpGBT configuration
Debugging features

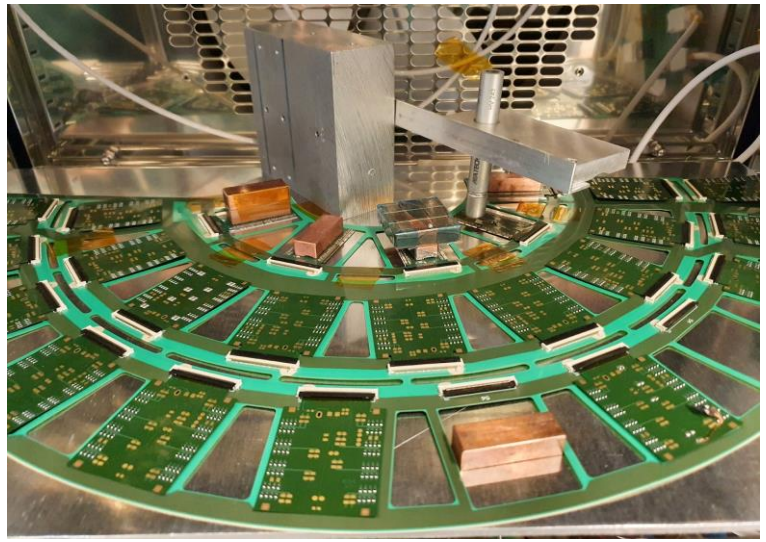


Test Setups with RD53A modules & demo portcard

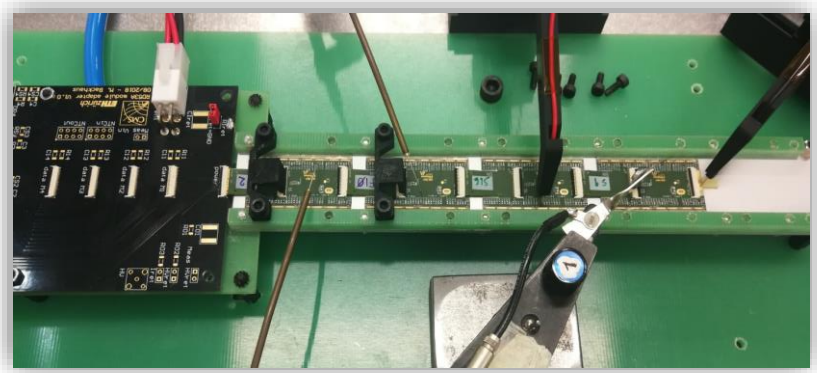
Quad module

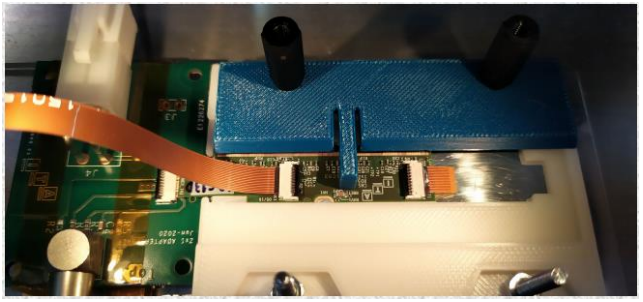


TEPX system test



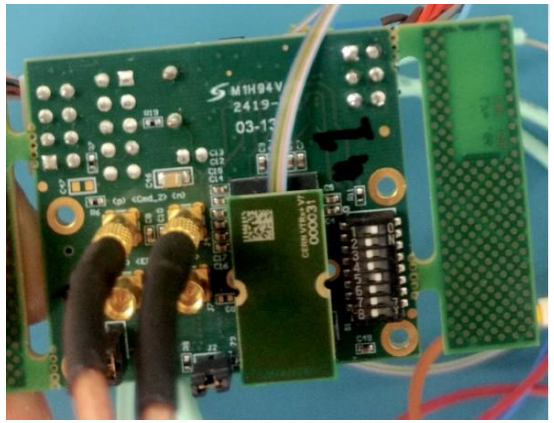
TBPX system test





Double module

TFPX system test



Demo Portcard