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## **【601】 Development of an advanced hybrid MOSFET/tunnel FET platform**

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High power consumption represents a major bottleneck for conventional transistor technologies (MOSFETs), due to the inability of further reducing supply voltage while simultaneously limiting the off-state leakage current. This limitation can be overcome by Tunnel FETs, a novel transistor concept based on the quantum-mechanical band-to-band tunneling. During my PhD research, I demonstrated the first hybrid technology platform combining III-V Tunnel FETs and MOSFETs with a scalable process and suitable for large-scale semiconductor manufacturing. Such low-power technology platform paves the way to future energy efficient electronics, with the ultimate goal to reduce the carbon footprint of the ICT industry.

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