Microchannel cooling

Oscar Augusto on behalf of

LHCb VELO Upgrade and CERN PH-DT groups

University of Manchester

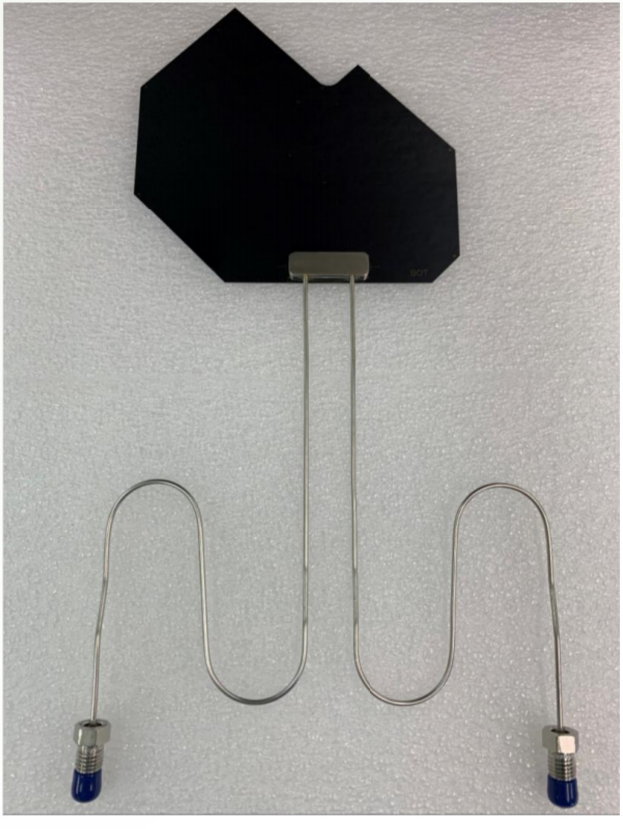
Forum on Tracking Mechanics 2021

17/05/21

Outline

- Layout and manufacturing
- Bare substrate
- Connector
- Attachment of the fluidic connector
- Substrate
- Production
- Final remarks

Microchannel cooling substrate



Layout

Race track like layout (500 µm)

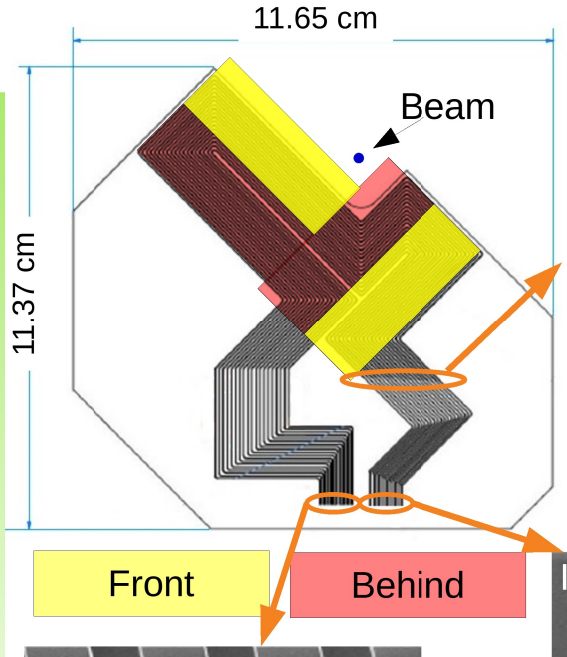
Restrictions:
- 60 x 60 µm² (40 mm long)
- length: 40 mm long

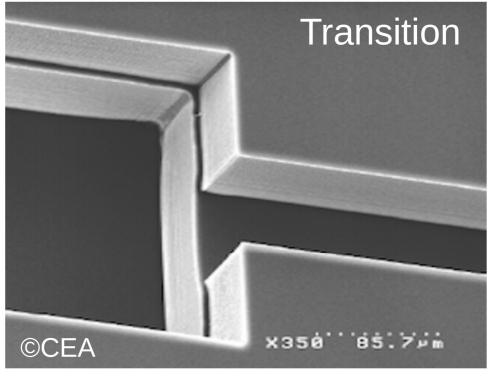
Main channels:
- dimensions: 120 x 200 µm²
- length: 220 mm long

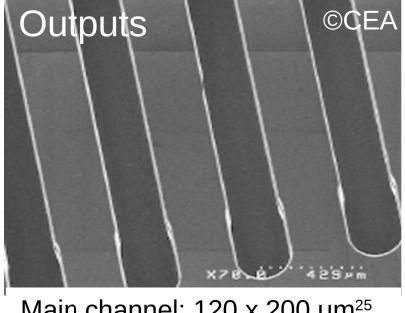
19 channels with approximately same total length (~30 cm)

Every channel has its own inlet and outlet hole (200 x 400 µm²)

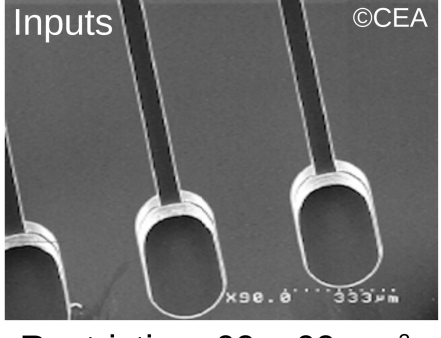
The CO_2 distributions among the channels is done by the connector







Main channel: 120 x 200 µm²



Restriction: 60 x 60 µm²

Advantages and disadvantages

Advantages

1) Minimum material budget (500 µm Si)
2) Homogeneous material distribution
3) No CTE mismatch with the respect to the ASICs
4) High thermal efficiency
   a) 140/240 µm Si between the coolant and electronics
   b) Power dissipation up to 50W with nominal flow while module power < 30W
   c) Very high thermal conductivity (Si 150W/m.K)
   d) Very low temperature gradients over the substrate (couple of degrees)
5) Fast response to changes in power dissipation (low mass + evaporative cooling)
6) CO2 has high latent heat

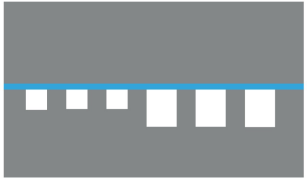
Disadvantages

1) More fragile than more conservative approaches:
   (a) More robust than initially expected specially after the module assembly
2) Main contribution to the material budget comes from the fluidic connector (Invar)
3) High pressure validation due to evaporative CO_2 cooling (up to 186 bar)
4) Relatively high cost
   (a) Alternative techniques (e.g.:buried channels [1][2])
   (b) Potential reusability [3]

Manufacturing at CEA LETI

Courtesy of CERN EP-DT group

Etching 550 µm, double side polished Si
(60 µm ± 3 µm, 115 µm ± 6 µm)



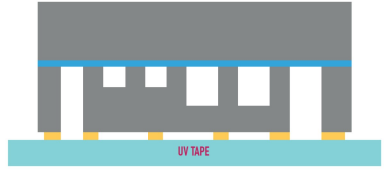
bonding of cap wafer with 400 nm at the bonding interface

thinning of cap wafer to 240 µm (790 µm total thickness)

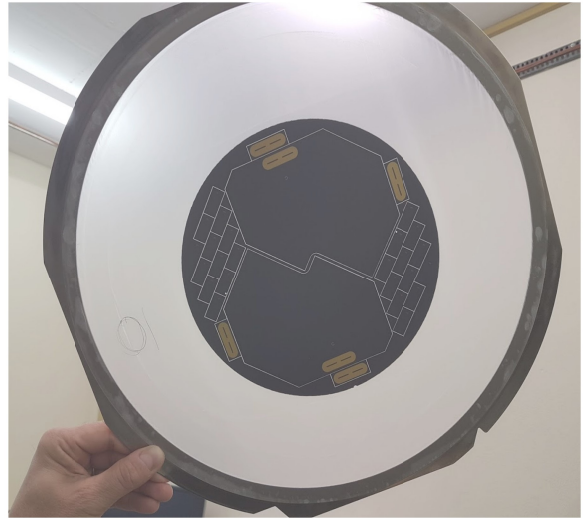
thinning of channels wafer to 260 µm
(500 µm total thickness)

Metalization: Ti(200nm), Ni(350nm), Au(500nm)

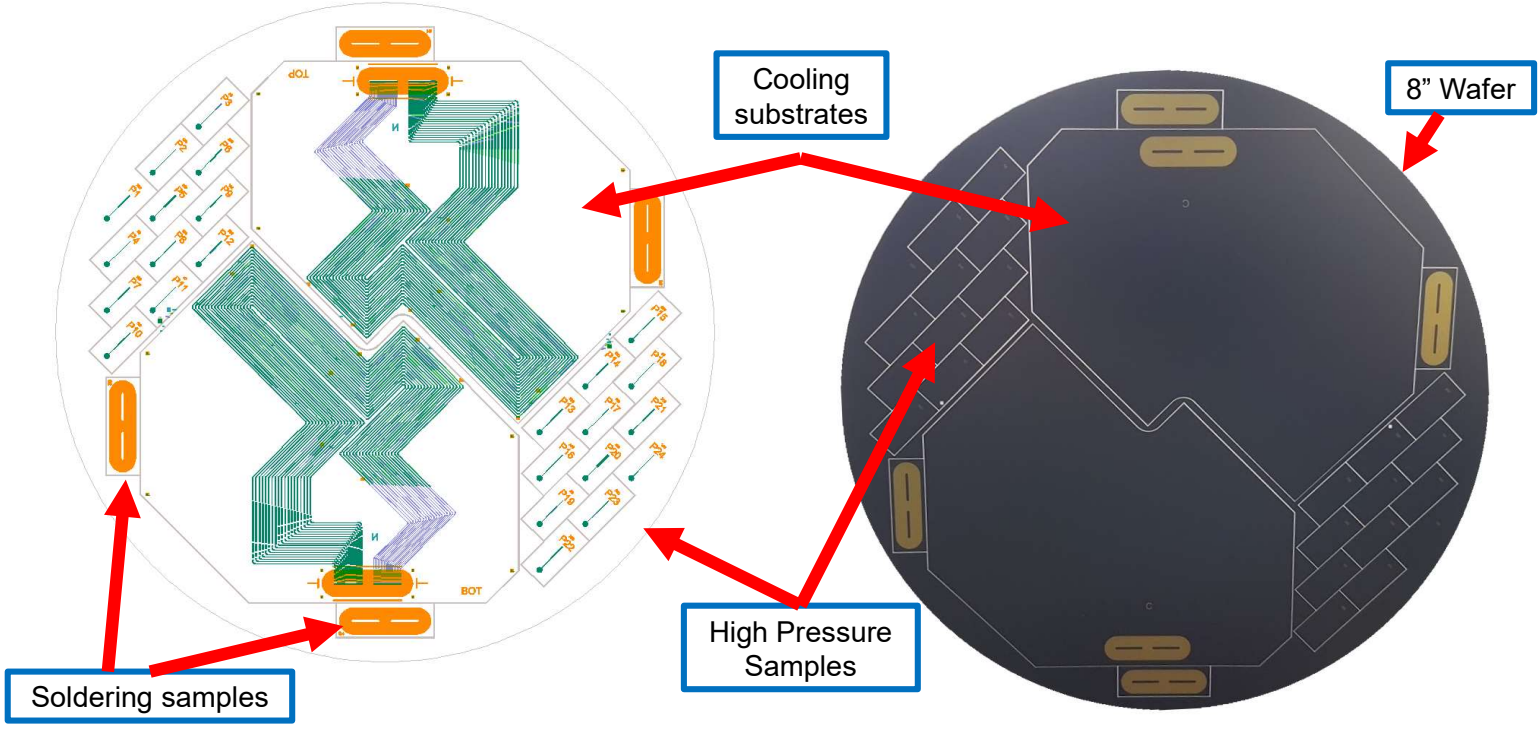
Etching of inlets and outlets



Dicing by plasma etching

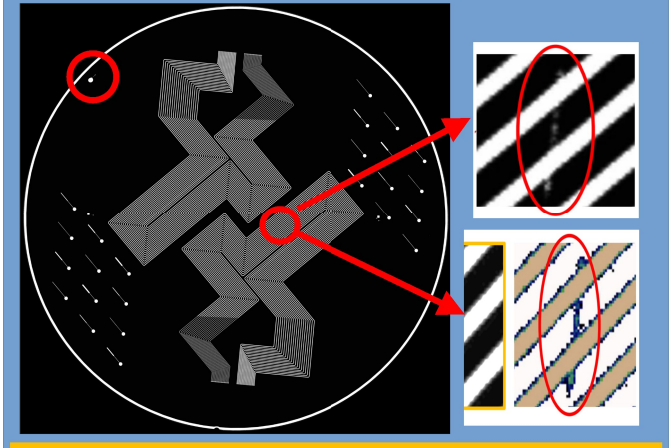


Wafer design



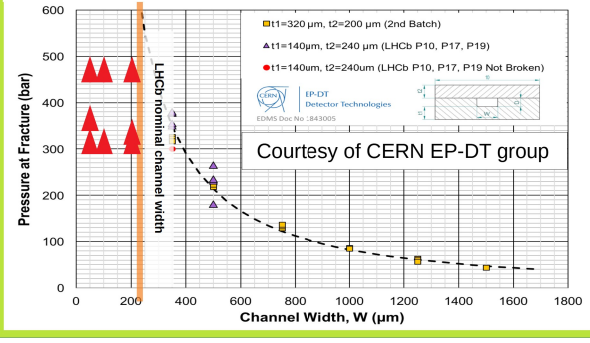
Bare substrate quality control

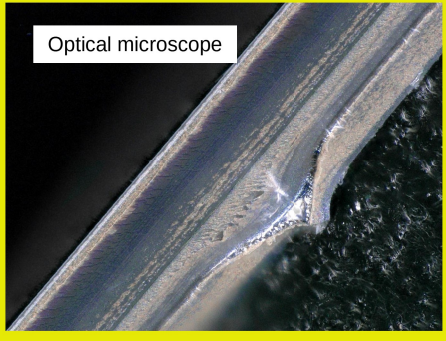
Bonding (Scanning accoustic microscope)

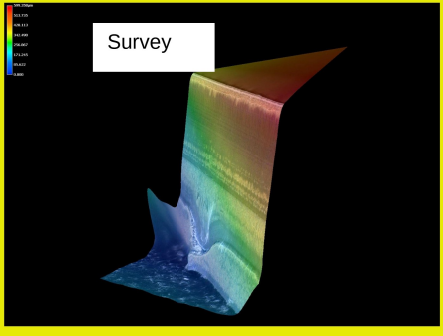


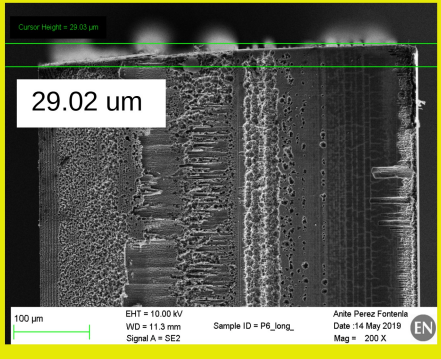
Larger areas means reduced resistance to high pressure

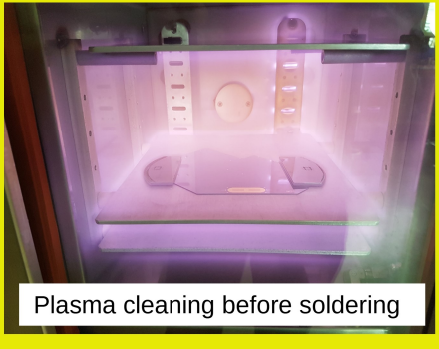
Resistance to high pressure







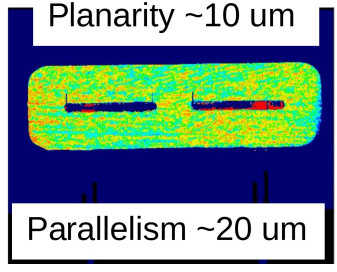


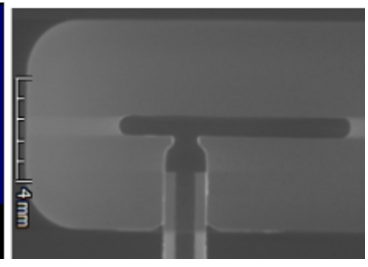


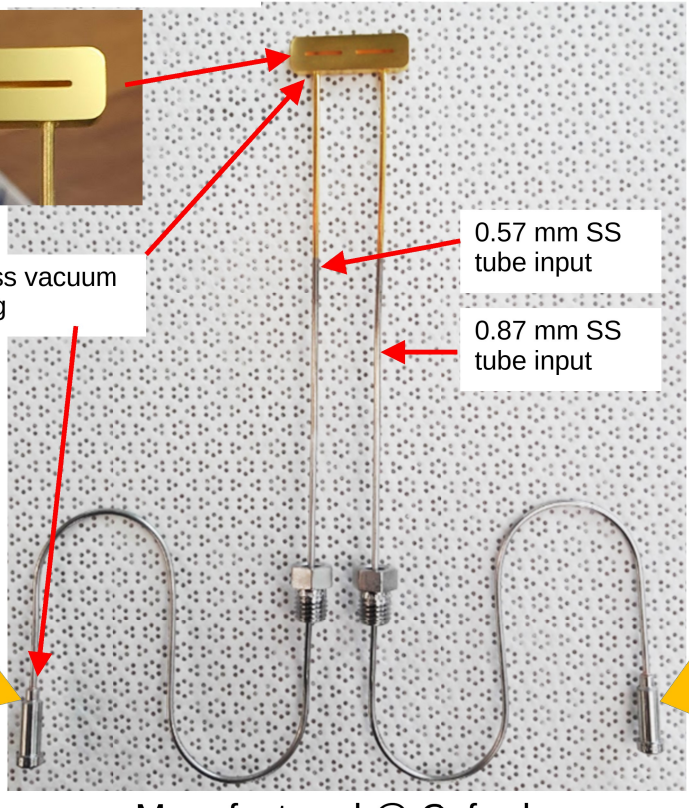
Fluidic connector

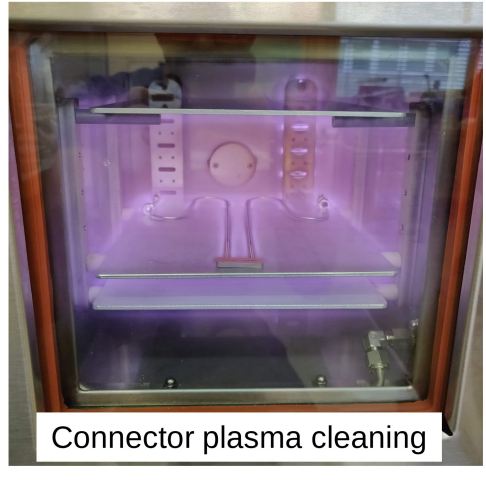
Invar 36 + Ni + Au metalization @ CERN

Brazing X-ray









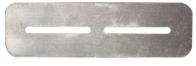
Manufactured @ Oxford

Fluxless fluidic connector soldering

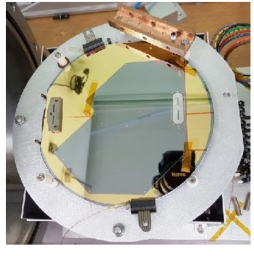
More information [1][2]

Fluxless process to avoid long term corrosive effects in the cooling system

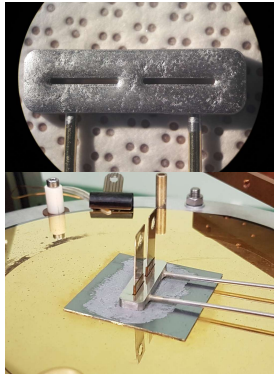
Silicon pretinning

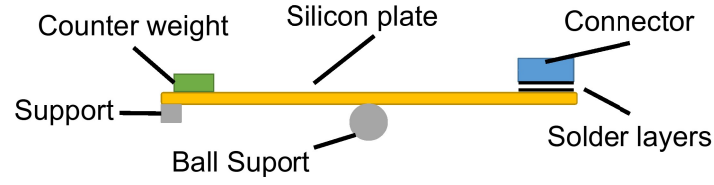


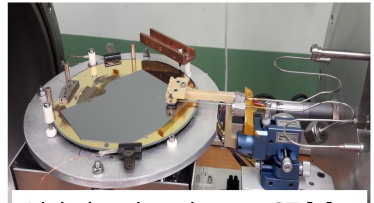
Preform 62Sn36Pb2Ag
100 [µm]



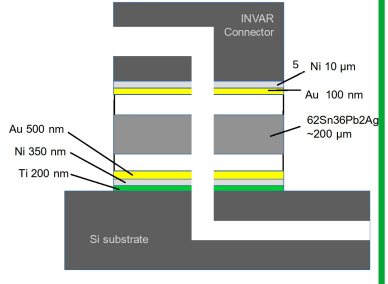
Connector pretinning

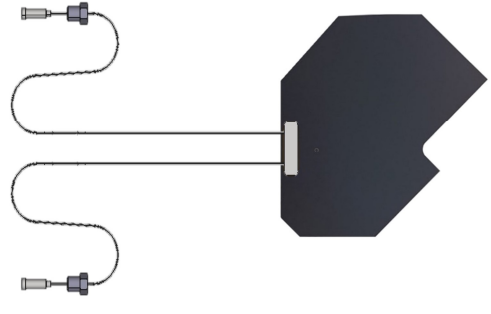






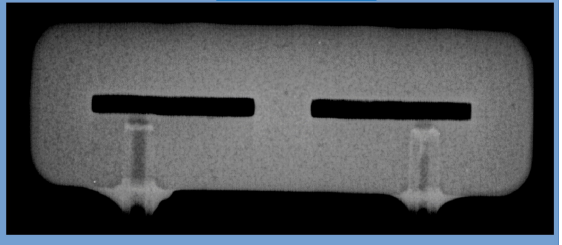
Light heating plate – ~27 [g], 8”, metallized silicon wafer



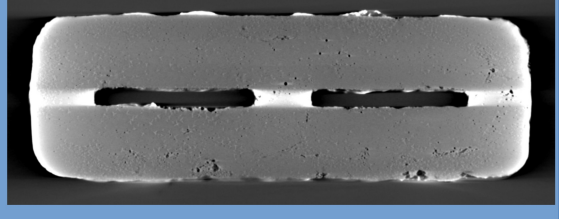


X-ray tomography (Zeiss Metrotom@CERN)

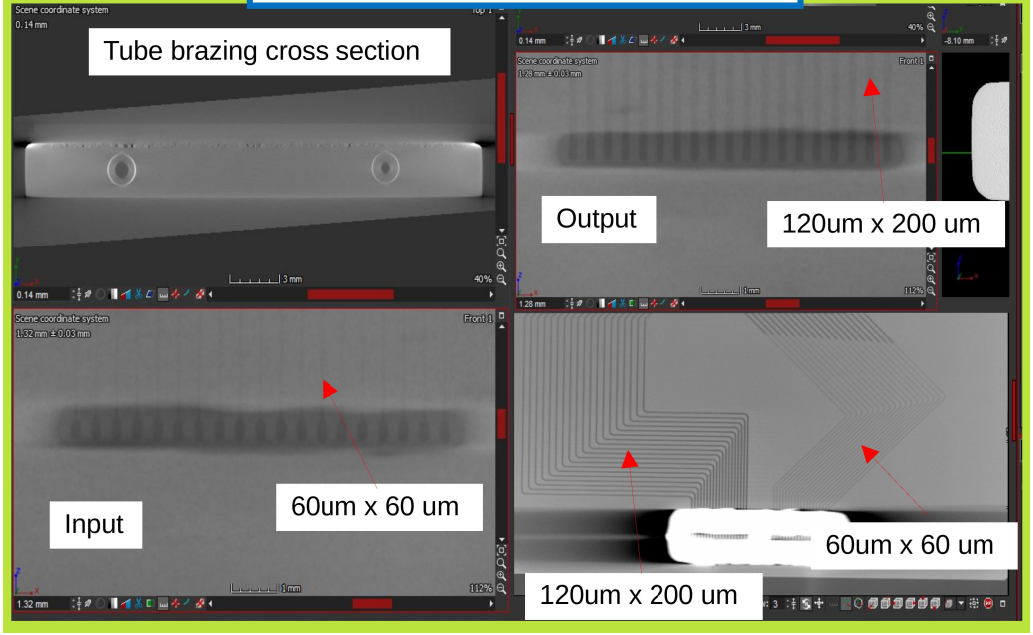
X-ray



3D X-ray tomography

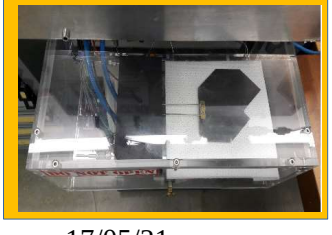


3D X-ray tomography



Substrates Q&C

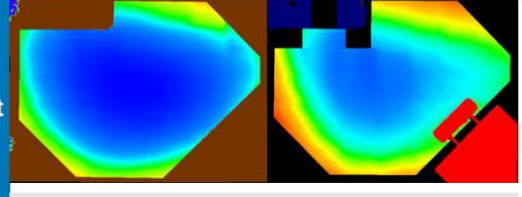
High pressure test up to 186 bar



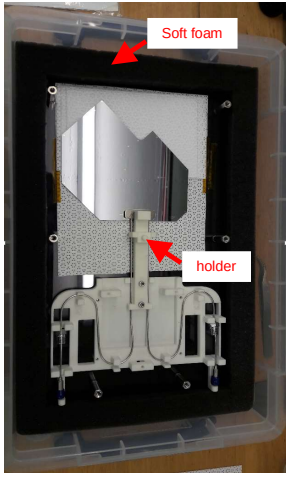
Helium leak test (vacuum inside)

Adixen ASM 142

High pressure helium leak test (60 bar)

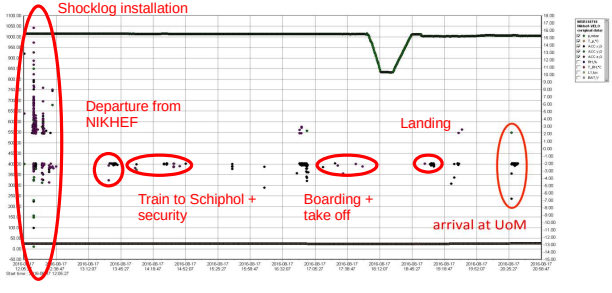
	before soldering	after soldering
planarity measurement		
min.	-60 µm	-50 µm
max.	+26 µm	+25 µm
variation	86 µm	75 µm

Transport per person



- Two level box can carry two microchannels at time
- Several transports during R&D phase without issues
- Transport by plane or car

Example of transport by personnel with up to 5g

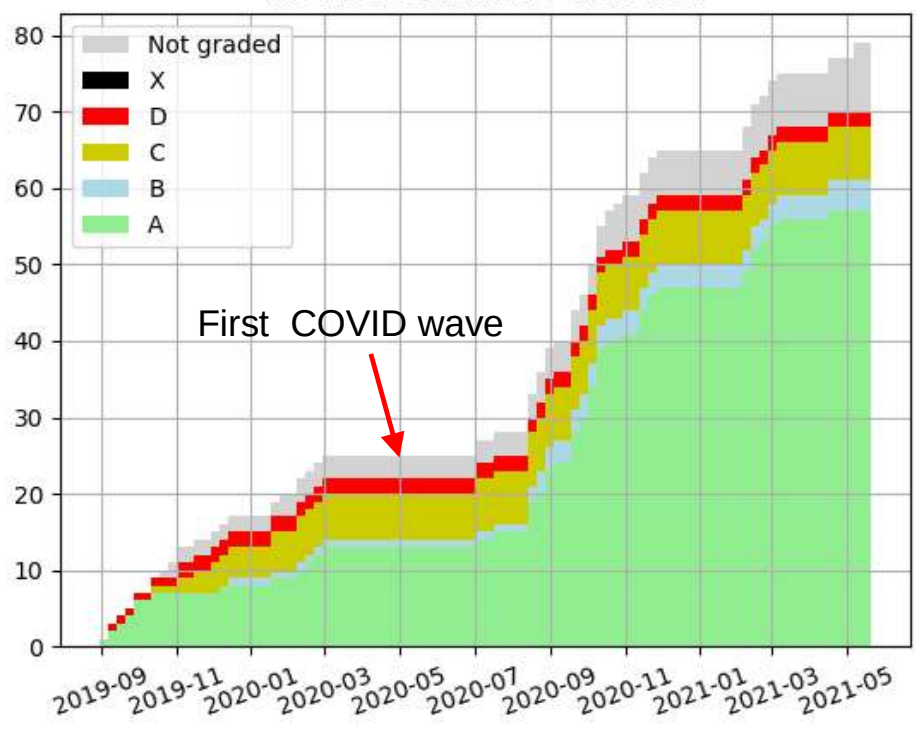


COVID

Transport by consolidated truck or plane

48 cooling plates transported without casualties even though the transport is significantly harsher (> 20g)

Production Evolution



Typical rate of 1-2 plates per week

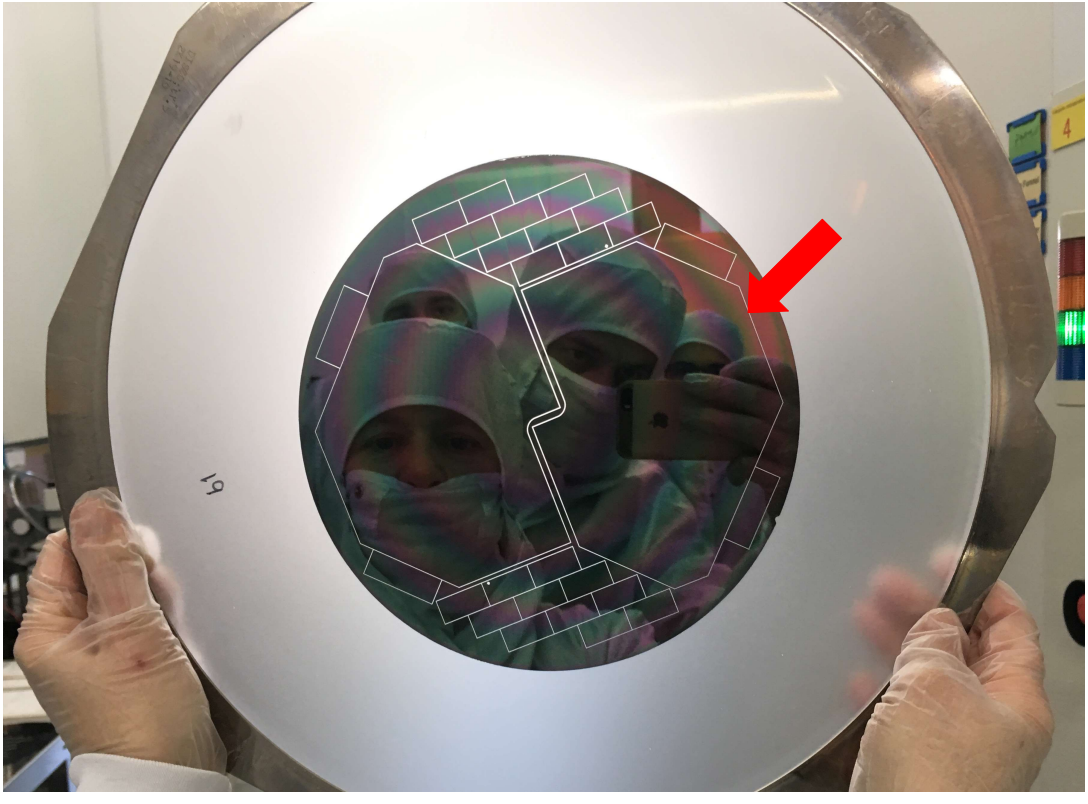
Overall yield of around 87% for detector level plates (A and B)

In total, 79 plates were processed after the R&D period

Potential to recover R&D plates if necessary

Final remarks

- The evaporative cooling through microchannels in silicon has several advantages such as minimal material budget, no CTE mismatch and great cooling performance
- After the substrate manufacturing, the most challenging aspect related to this technique is the attachment of the fluidic connector
- Most of the production time was focused on the components preparation and inspections.
- The covid outbreak brought the additional challenge of the shipping without the personnel which was overcame successfully through *standard courrier* with a robust packaging
- Currently, the 61 detector level cooling plates have already been produced (52 needed for the detector) and extra plates are being prepared



Thank you for your attention!

VELO upgrade Module Assembly

On behalf of the LHCb VELO group.

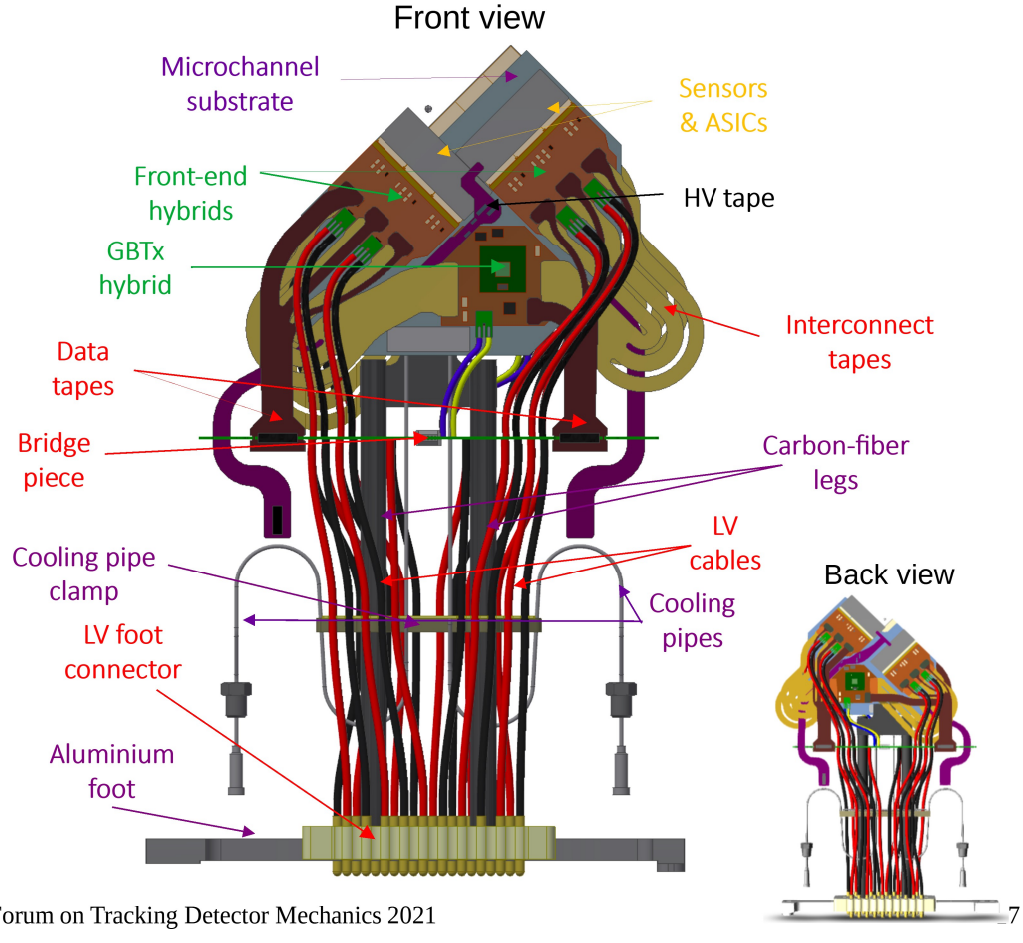
Gianluca Zunica

VELO Modules Assembly

Outline:

- Two construction sites:
  - Manchester
  - Nikhef
- Bare module: Microchannel substrate + structural components
  - Substrate flatness
- Tile glueing
  - Tile position
  - Tile flatness
  - Glue thickness
- Hybrid glueing
  - Front-End, GBTx hybrids
  - Hybrid position
- HV tapes
- Wirebond
  - Pull test
- Tapes & cabling: Low Voltage foot connector & cables, bridge piece, interconnect & data tapes

Electrical tests

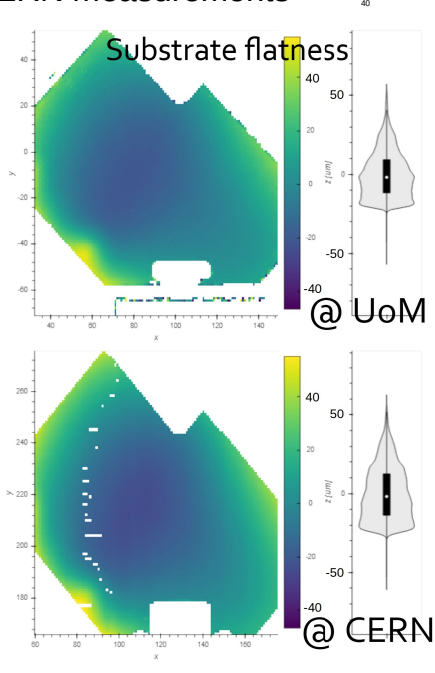


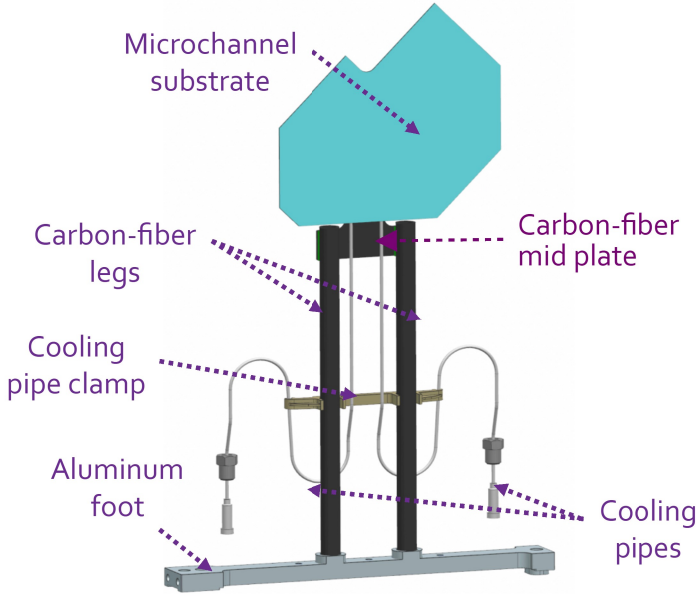
Bare Module

MicroChannel (MC) substrate (with soldered cooling pipes & connector) assembled with

- Carbon Fiber Legs
- Carbon Fiber midplate
- Aluminium foot

  - Measure MC flatness & compare with CERN measurements





One day needed for assembly (glue curing time)

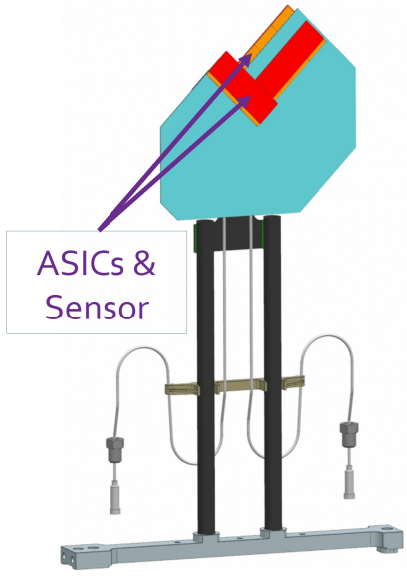
Tile gluing

Tiles (sensor+3 bump bonded asics) attachment to MC substrate is a crucial step:

- the glue layer is the only interface between the MC and the tiles: crucial for heat dissipation (30W in vacuum at operation conditions per module).

Glue requirements :

- good thermal conductivity, radiation hard, good ageing properties, good mechanical properties, ease of deposition, good match with silicon CTE



- Glue choice: Stycast 2850FT with catalyst 23LV: epoxy based adhesive (resin + filler mixed with liquid catalyst)
  - Good thermal conductivity: 1.1 W/mK
  - Radiation hard, good ageing properties
  - Good CTE –> can absorbe components Thermal expansion
  - Cons: hygroscopic catalyst

Tile gluing: pattern optimisation

Extensive R&D carried out to optimise glue patterns:

- Target thickness: 80 µm –> good heat transfer & thermal dilatation absorbtion
- Target evenness: ±40 µm –> uniform glue layer == uniform heat dissipation
- Target coverage: 70% of the asic
- No air bubbles trapping when pressing down (air axpansion in vacuum+heat)
- Avoid splillage in-between asics –> cause electronic noise

Glass samples to observe patterns after pressing down

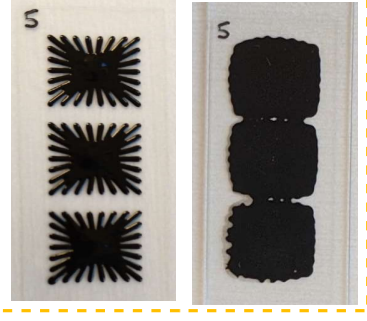
First pattern

Snake pattern:

- Good coverage
- Prone to air trapping

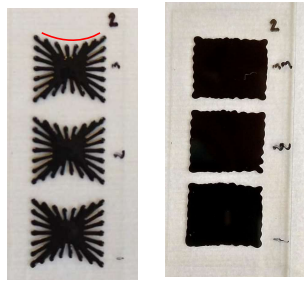
Star pattern:

- Good coverage
- No air trapping
- Prone to spillage



Hourglass star pattern:

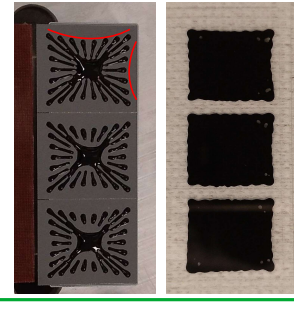
- Good coverage
- No air trapping
- No spillage



Optimised pattern

Add bowing to all sides:

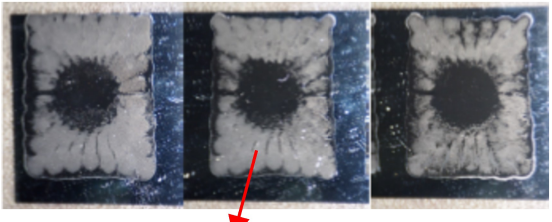
- Control spillage in both directions



Catalyst hygroscopy

Catalyst is hygroscopic –> layer of humidity deposit on the glue patterns before pressing down

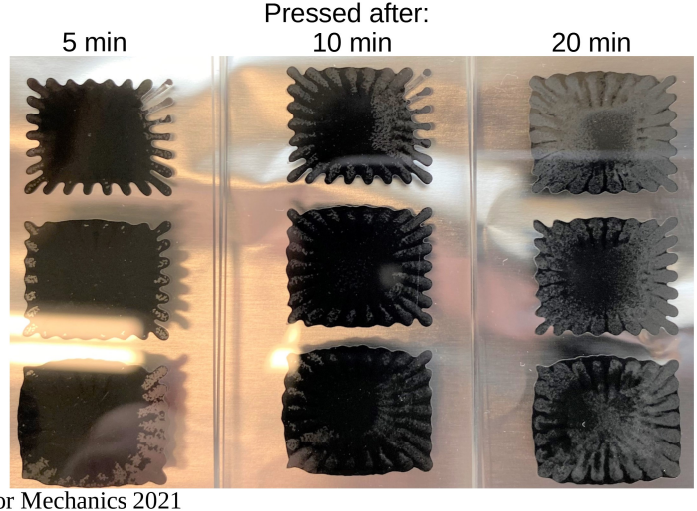
- Could weaken the bond causing failures during the detector lifetime
- The issue materialise only with ageing



Whitish area: water layer between surface and glue

Extensive R&D carried out

- Prepare and age glue patterns
- Understand how long does it take for the glue to get damp
- Come up with a solution “easy” to implement within the tile gluing procedure

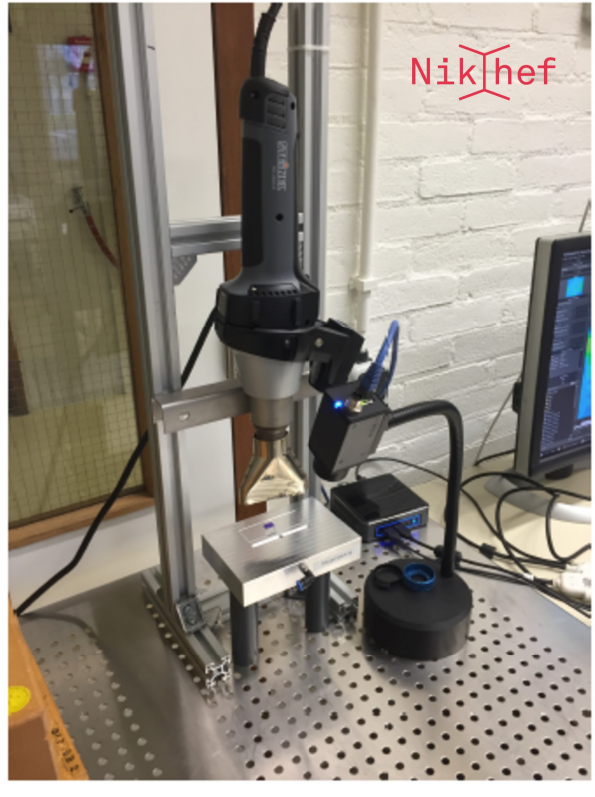


- Dispensing procedure (4-5 min) is too long to avoid humidity absorbtion

Heat treatment

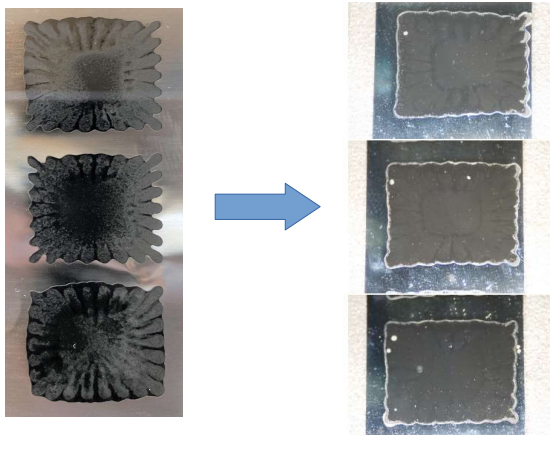
The solution:
- blow hot air onto the freshly deposited patterns

- Heating at 60°C for 1 minute removes most of the humidity



No heat treatment

1 min heating

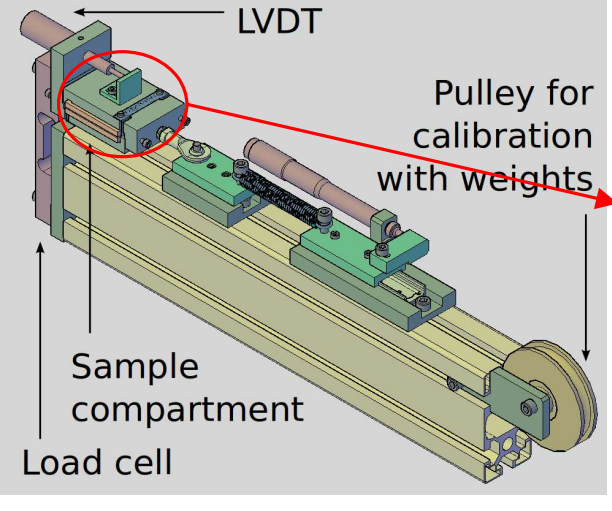


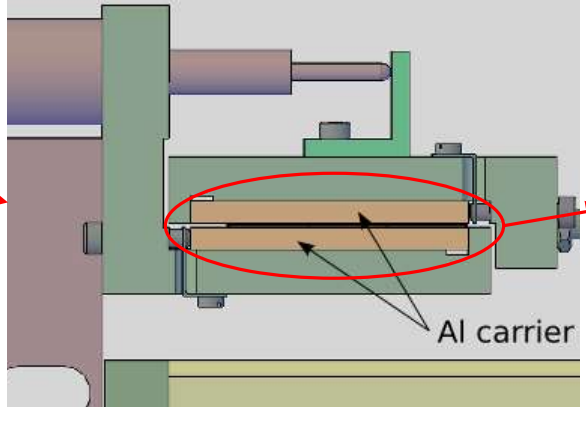
- Confirm goodness of results with Shear force and Cantilever (peel) tests

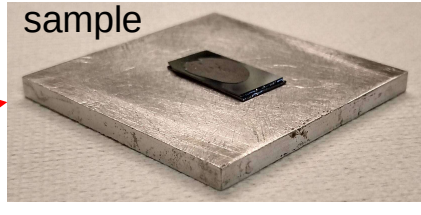
Shear Test

Shear test:

- Applied shear force up to 20N, measure displacement at max load, age in oven and repeat
  - Max displacement <10 μm
  - No effect due to ageing (up to 2 years)
  - All samples survived







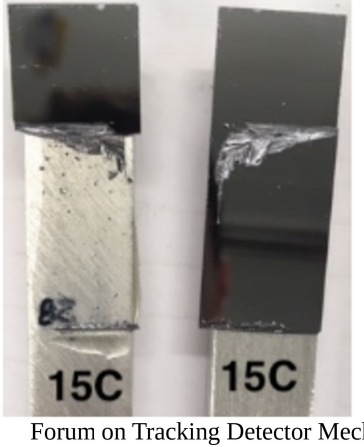
Cantilever test

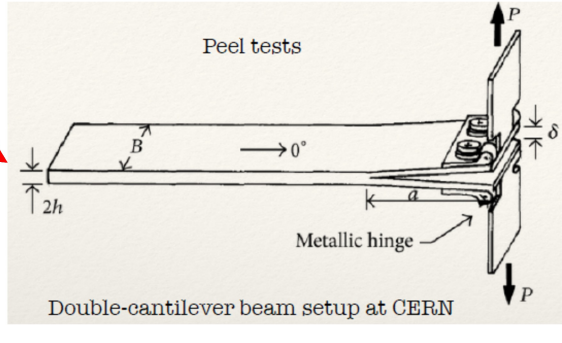
Cantilever (peel) test:

- Apply force to one end of the sample, age, repeat
- Applied force up to 500 N, no break & no ageing effects !
  –> extremely good adhesion

Sample Name	Radiation[MRad]	Age time [H]	Thermal Cycles	Num. DCB test	DCB outcome	DCB max force [N] for the last test
11C	—	621	0	5	No break	499
12C	300	621	0	5	No break	498
13C	—	621	0	5	No break	500
14C	600	621	0	5	No break	501
16C	—	505	811	4	No break	502
17C	—	505	811	4	No break	501
15C	—	528	811	1	Broken in Araldite	319
18C	—	528	811	1	No break	498

Only breakage observed in the araldite interface

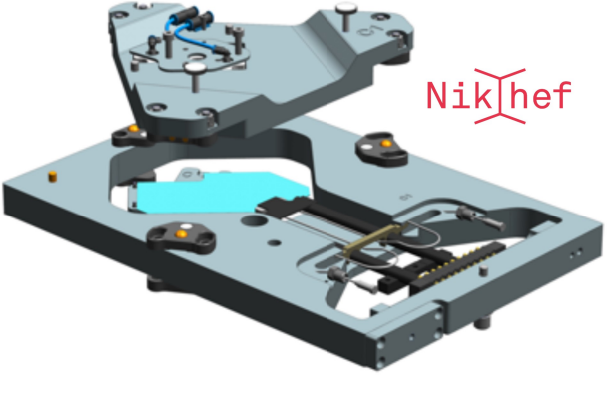


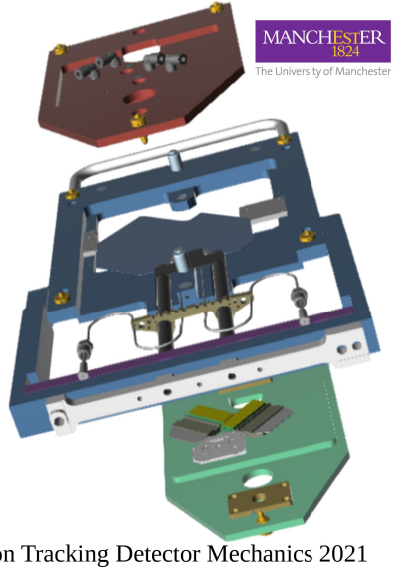


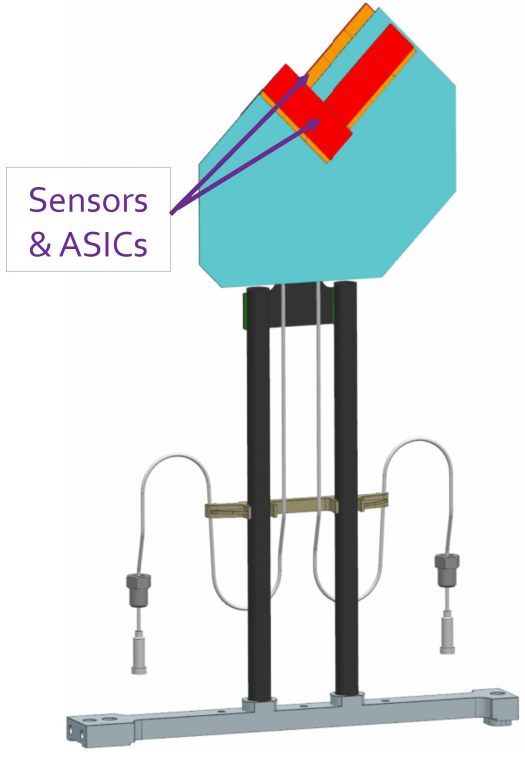
Tile gluing

Gluing procedure:

- Align tiles (precision required <±30 μm) on jigs
- Mix and deposit glue via robot dispenser
- Heat treatment
- Press onto microchannel
- Different approaches for construction sites:
  - Nikhef: pick-and-place machine, 2 tiles at the time
  - Manchester: assembly stages and jigs, 4 tiles at the same time





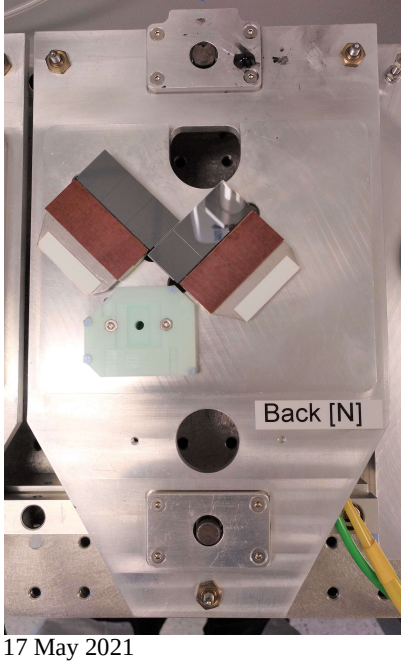


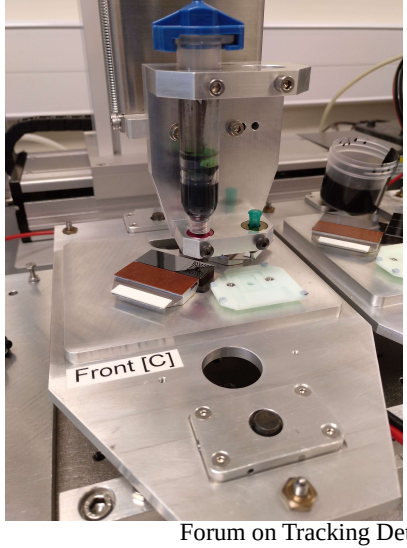
Tile gluing

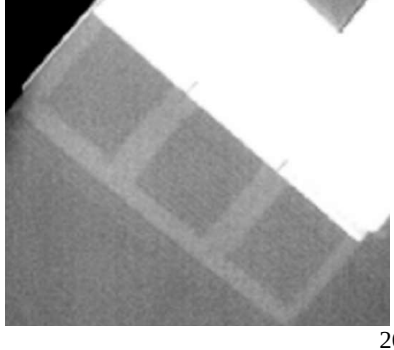
Pattern dispensing:

- Mix glue (5 min, 1000 RPM) with planetary mixer
- Monitor glue viscosity & decide dispense speed/pressure
- Deposit glue via robot dispenser
- Optimised pattern: hourglass star

Viscosity (mg)	Speed (mm/s)
95 - 100	12.1
90 - 95	11.5
85 - 90	11.0
80 - 85	10.3
75 - 80	9.7
70 - 75	9.0
65 - 70	8.4
60 - 65	7.8



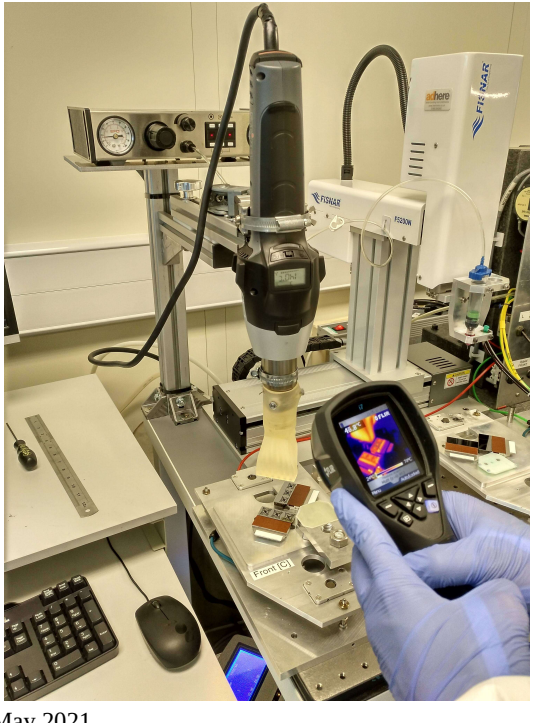


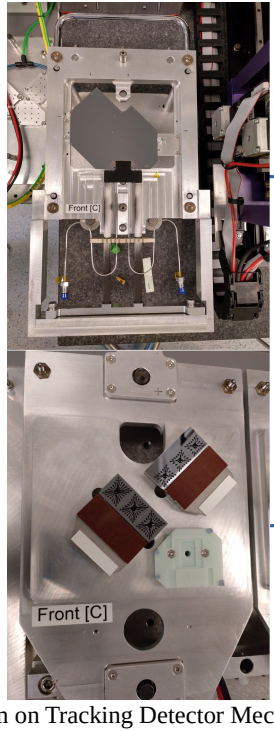


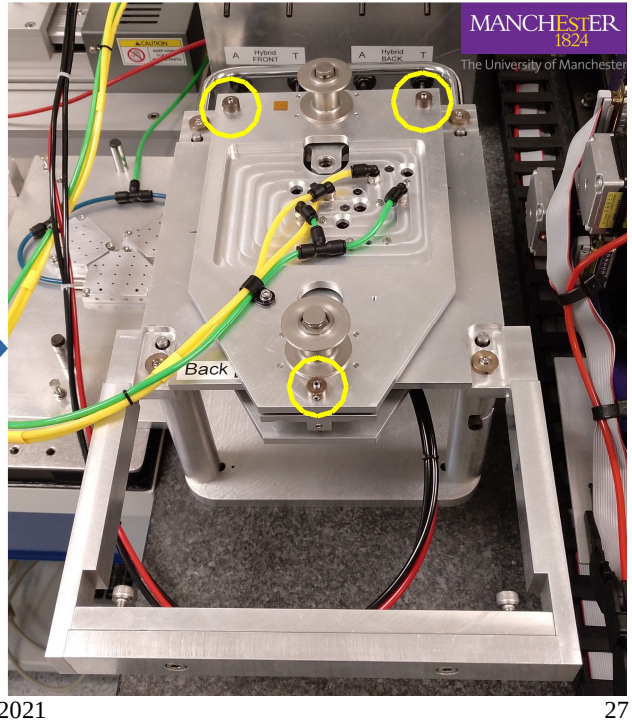
Tile gluing

- Heat treat patterns for 1 minute @60°C –> Remove humidity from glue surface

- Press onto microchannel
  - Distance ensured by 3 micrometric screws
  - Press down within 1 minute to prevent humidity re-absorbtion

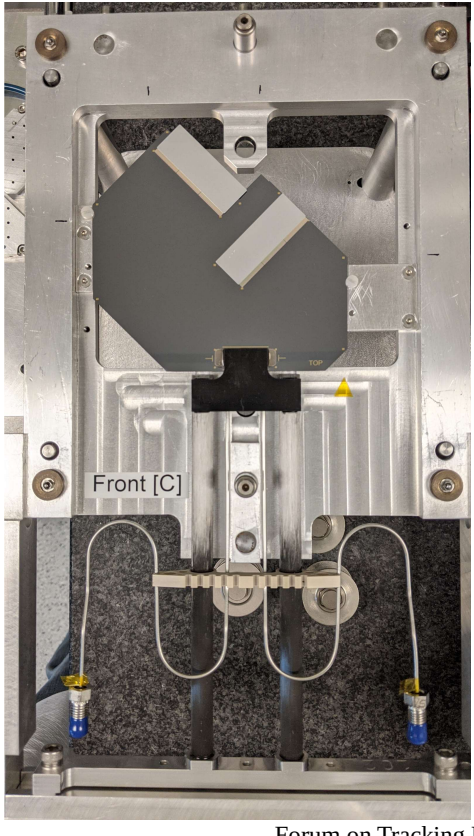


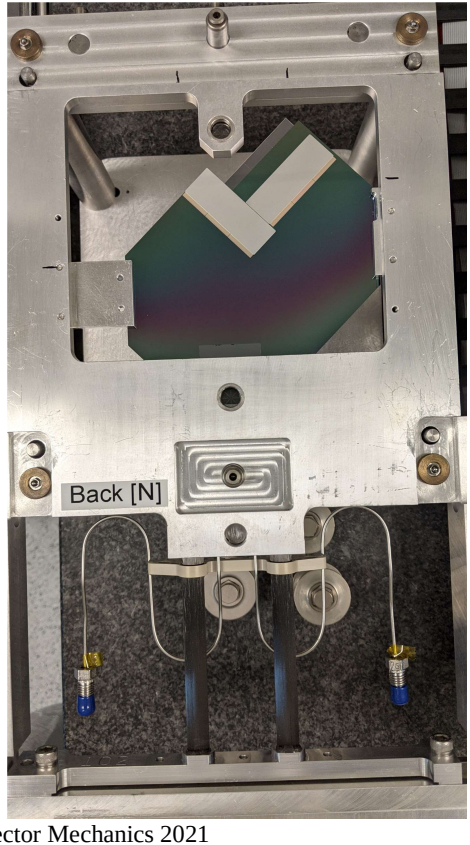




Tile gluing

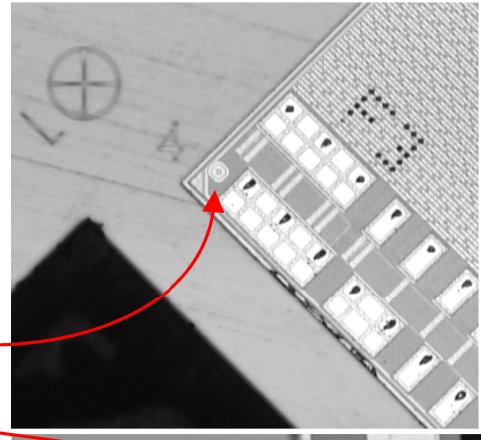
Let glue glue cure for 1 day





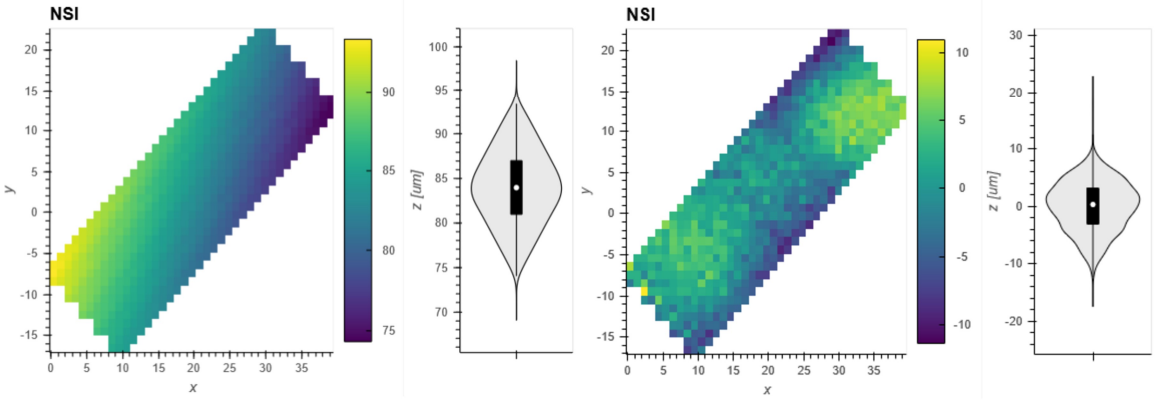
Tiles metrology

- Tile positioning:
  - Target precision <30 µm
  - Sensor & asic fiducials

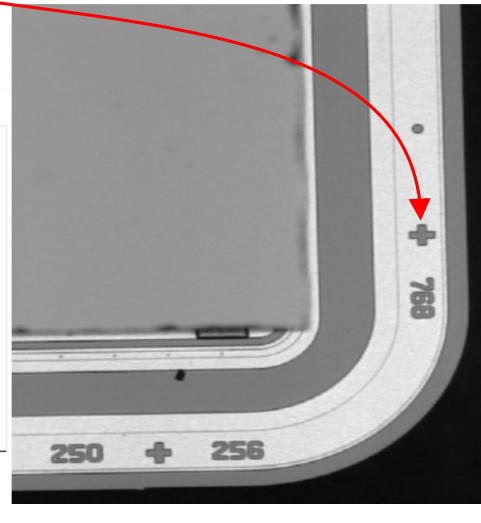


- Target Glue thickness: 80 µm
- Target Tile flatness: ±20 µm

Glue thickness



Tile flatness

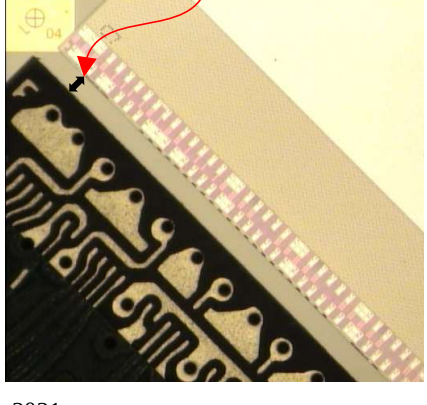


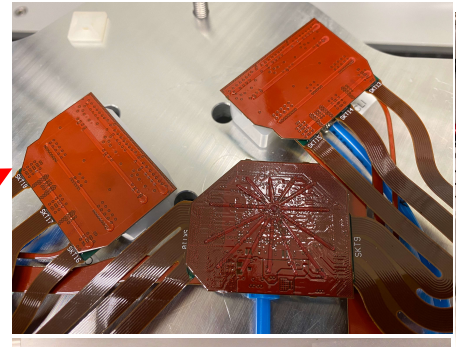
Hybrid gluing

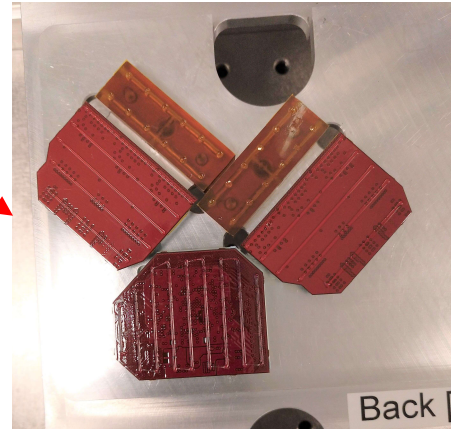
Glue the 4 Front End and 2 GBTx Hybrids (both sides):

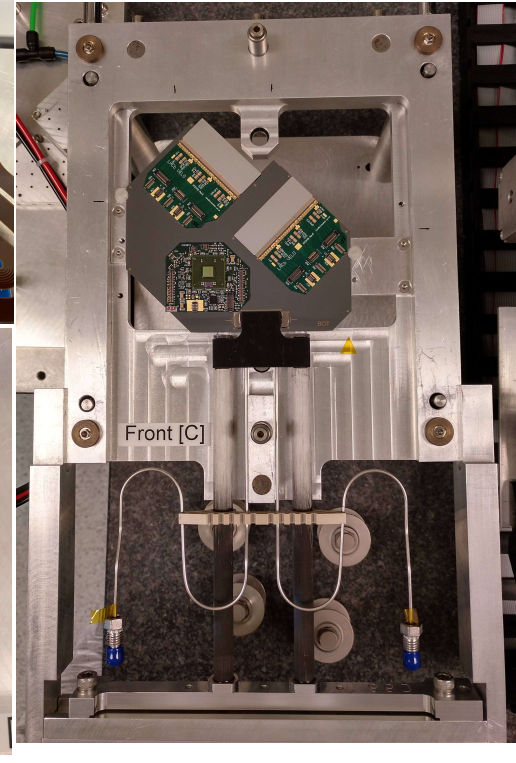
- Precision required < 100 μm
- Dispense glue (Loctite 5145)
- Nikhef: assembly hybrids and cables then glue all toghether
- Manchester: attach all hybrids, assembly tapes/cables at later stage

- Check FE hybrids positioning







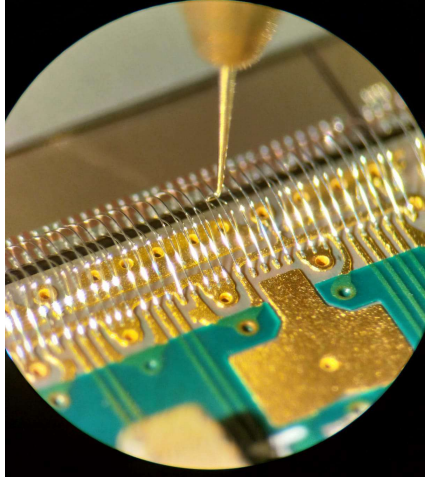


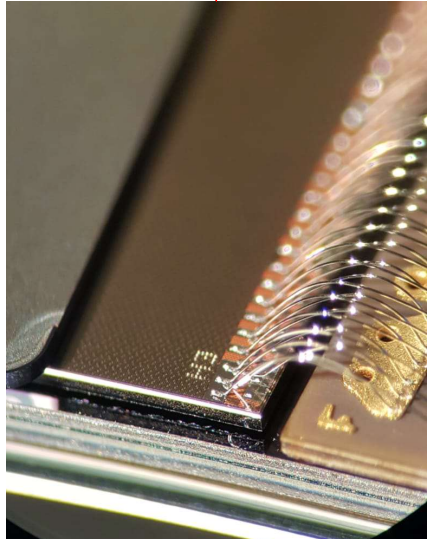
Procedure time: 1 day (glue curing time)

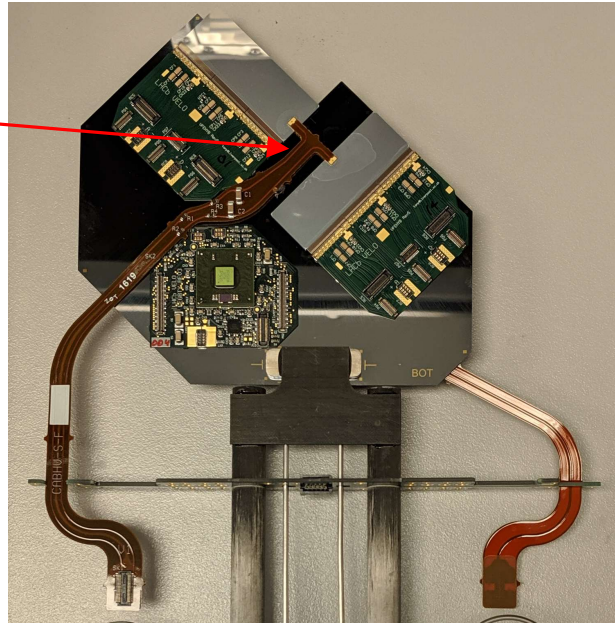
Wire bonding

Both sides:

- Glue HV tape
- Wirebond FE hybrid to asic
  - 140 per asic
  - 1680 per module
- Pull sacrificial bonds
  - 4 per asic







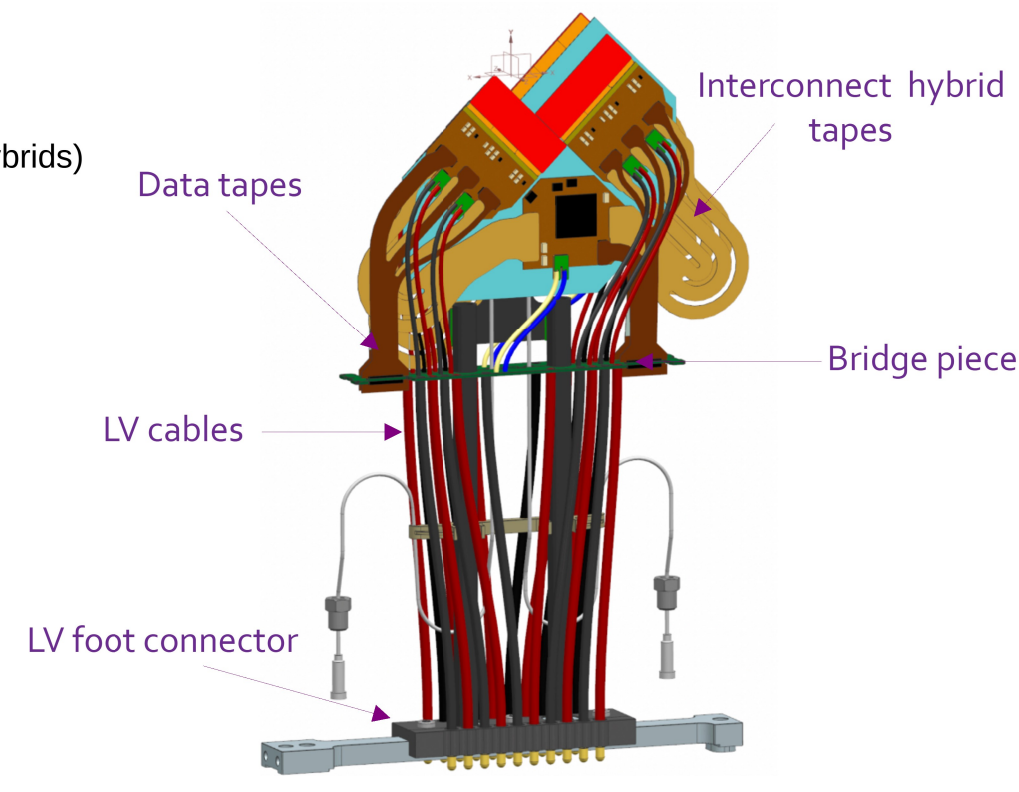
Record break strenght

- Assign grading
- Ideal target: all break strenght > 5 g

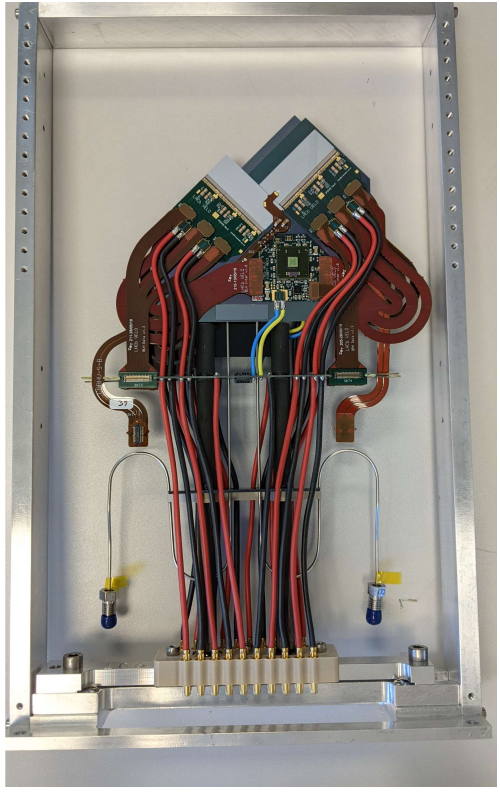
Tapes & cables

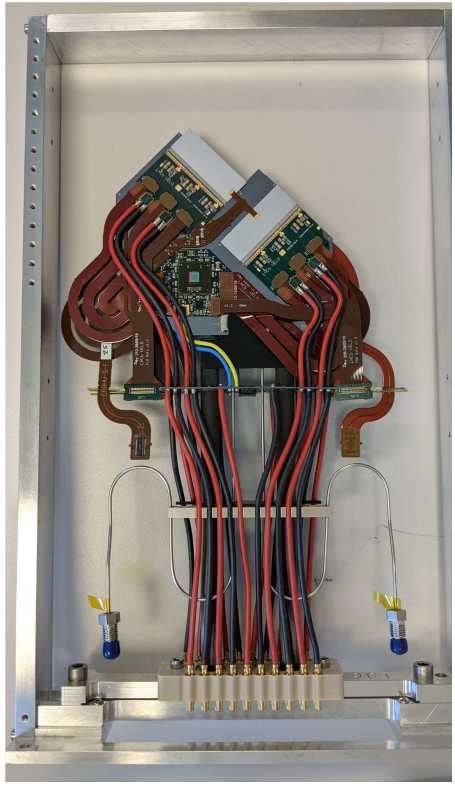
Assemble (Manchester procedure):

- Interconnect tapes (FE to GBTx hybrids)
- Data tapes
- Bridge piece
- Low Voltage (LV) cables
- Low Voltage foot connector



Assembled Module

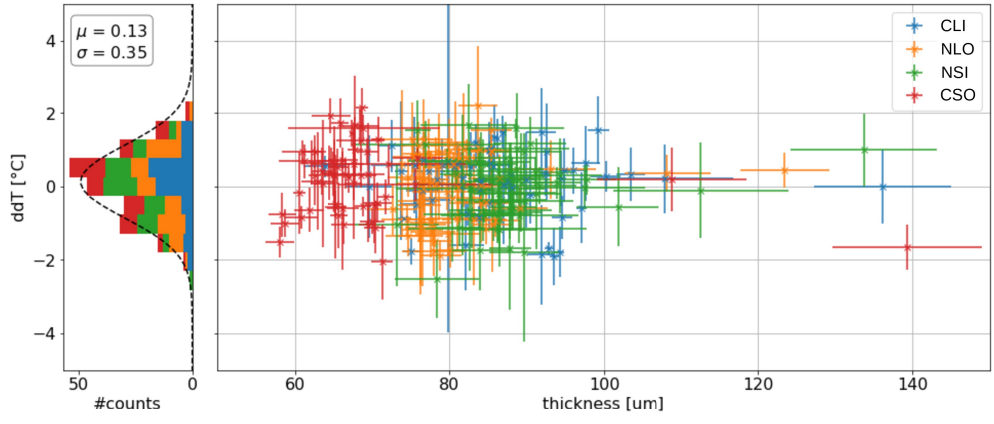




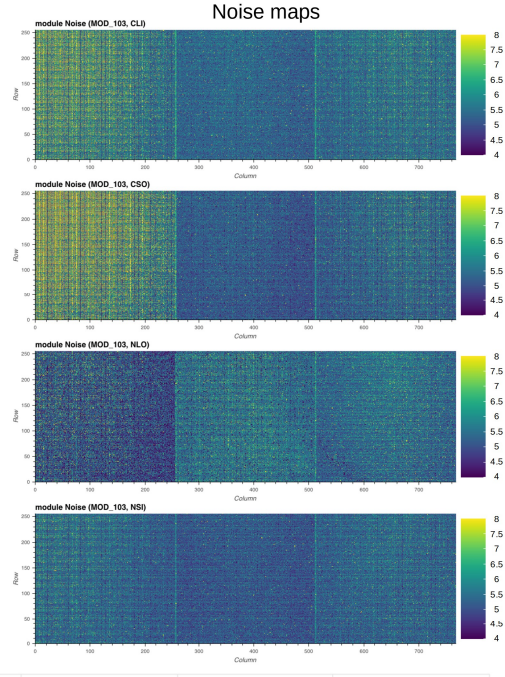
Electrical Tests

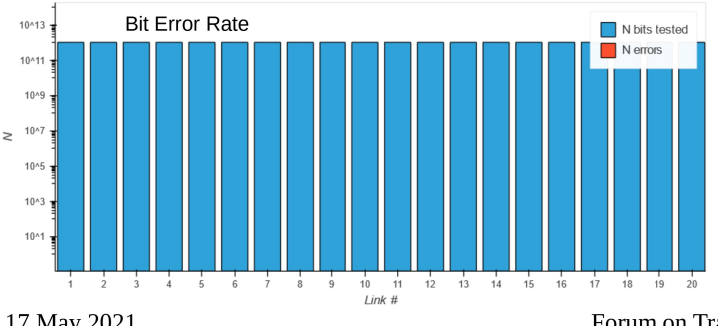
- All modules are tested for electrical and cooling performance before and after Thermal Cycling (TC)

Cooling performance

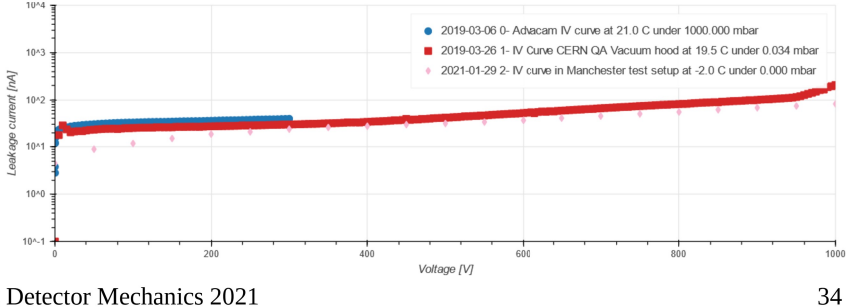


Noise maps





Leakage Current



Conclusions

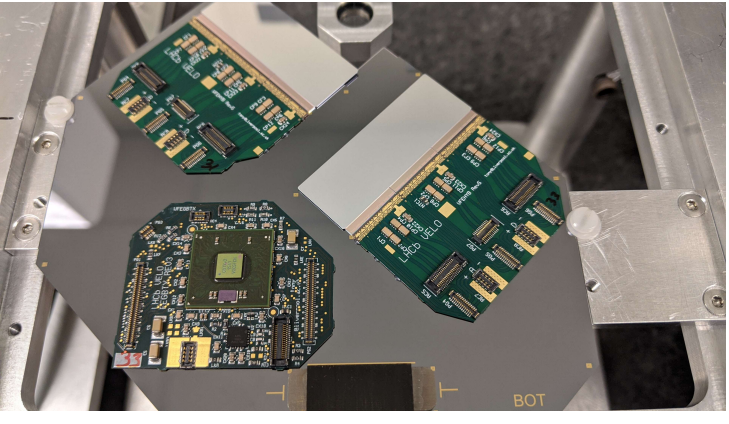
- Module assembly proceding smoothly
- All assembly steps followed by metrology and grading
- Special care put into glue layer quality
  - Crucial for module heat dissipation and mechanical soundness
  - Extensive R&D effort to address glue issues and procedure optimization
  - Shear and Peel test campaign to assess bonding quality
- Final Electrical tests to ensure the module works as intended

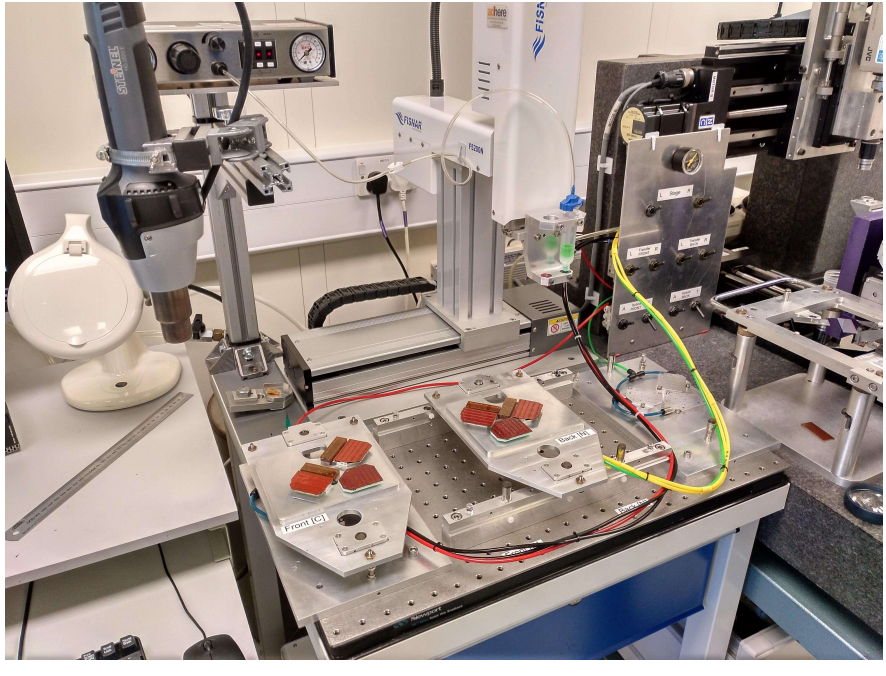
Consistent performance before and after termal cycling

Backup slides

View of the hybrid gluing setup in Manchester: robot, jigs, turnplate (right)

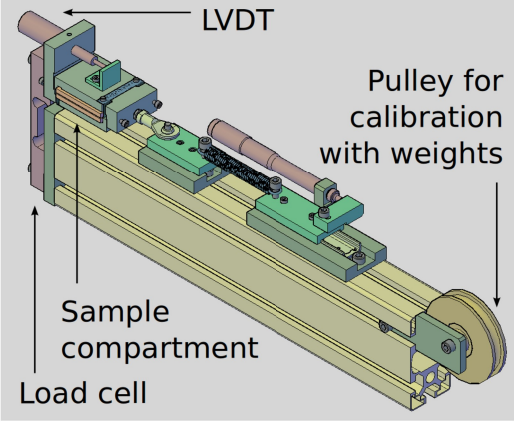
Glued Hybrids

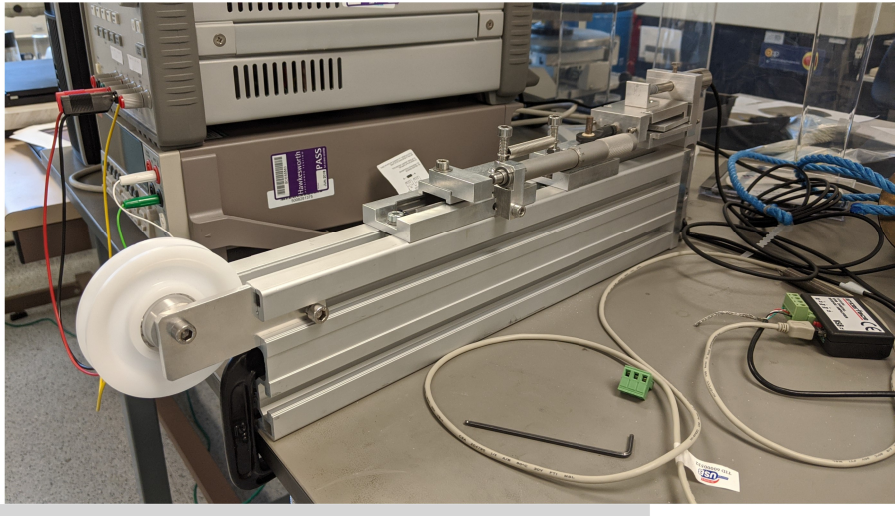


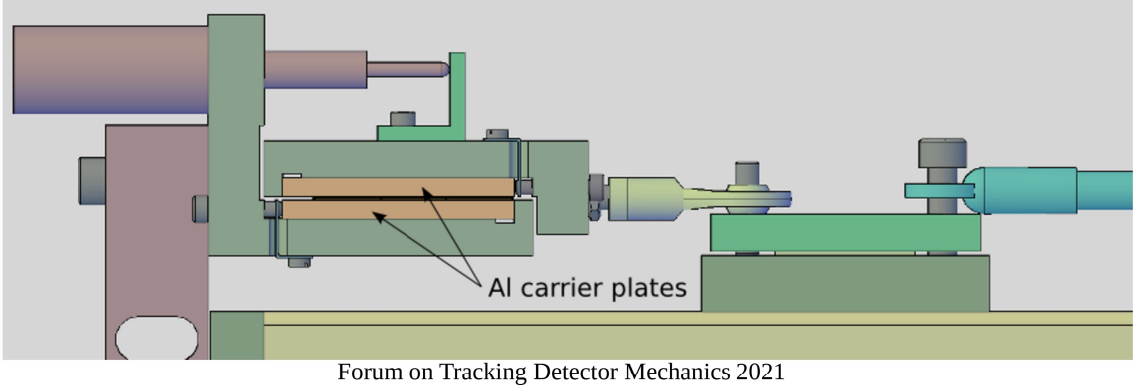


backup

Shear test setup







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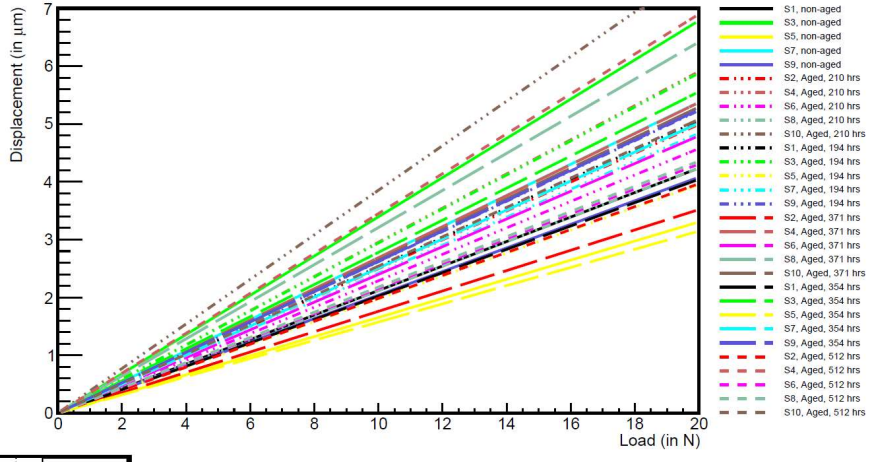
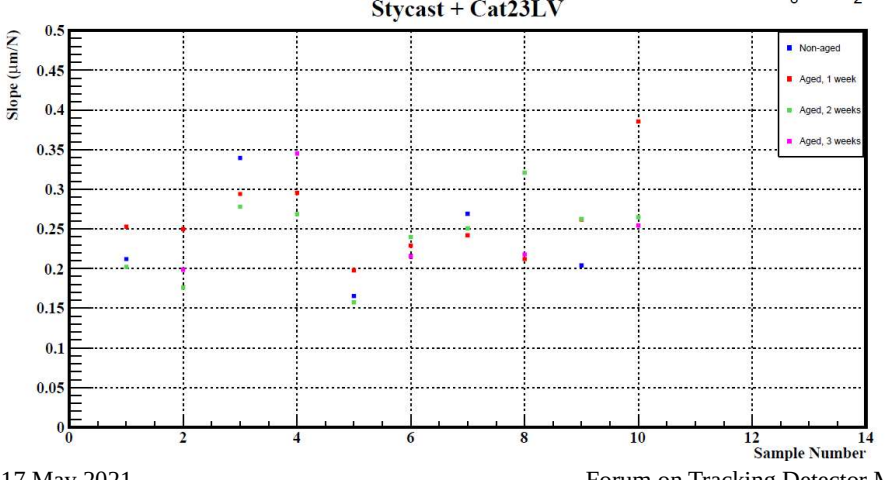
Shear test results





backup

Module grading

Bare module

Substrate Flatness
Grades (within η_{25} & η_{75})
- A (±50 µm)
- B (±75 µm)
- C (±100 µm)
- F (outside)

Wire bonding grading??

Tile gluing

Glue Thickness
Grades (mean ± 2 · stdev)
- A (-40 µm, +120 µm)
- B (-30 µm, +150 µm)
- C (-20 µm, +180 µm)
- F (outside)

Tile Flatness
Grades (mean ± 2 · stdev)
- A (±20 µm)
- B (±40 µm)
- C (±60 µm)
- F (outside)

Tile placement
Grades (Δx, Δy)
- A (< 30 µm)
- B (< 45 µm)
- C (< 60 µm)
- F (outside)

Mechanical performance

IV scan
Grades (result interpretation – IV behaviour)
- A (all OK)
- B (minor issues)
- F (major issues)

Thermal performance scan
Grades (ΔT of ASICs)
- A (all < 5 °C)
- B (all near beam < 5 °C)
- C (one near beam < 7 °C)
- F (any > 7 °C)

Displacement measurement
Grades (max displacement)
- A (< 100 µm)
- B (< 150 µm)
- C (< 200 µm)
- F (outside)

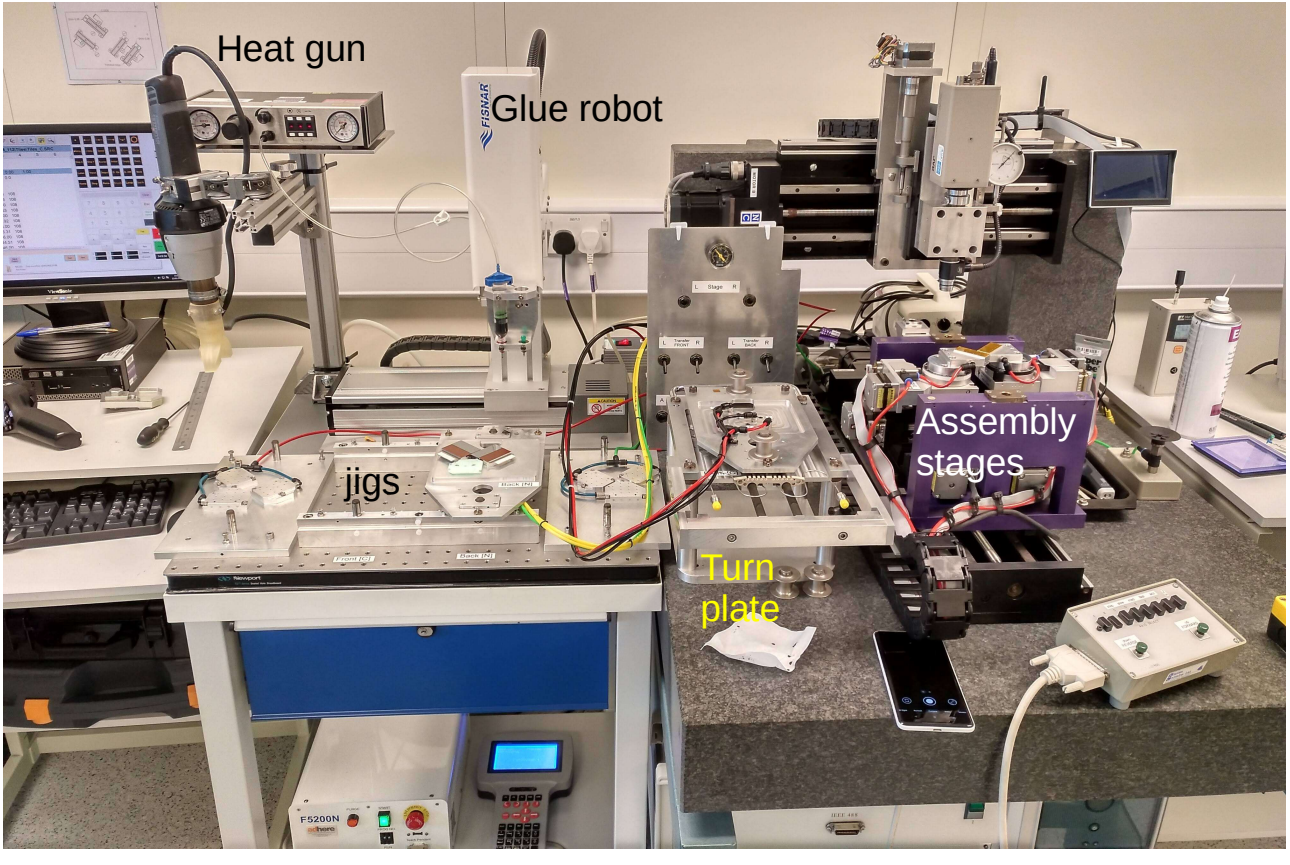
Communication performance

Equalization scan
Grades (result interpretation – noise, pattern and mask)
- A (all OK)
- B (minor issues)
- F (major issues)

PRBS test
Grades (BER per link)
- A (all < 10^{-12})
- B (any, different tape > 10^{-12})
- C (any, same tape> 10^{-12})
- F (any > 10^{-10})

backup

Tiles assembly setup



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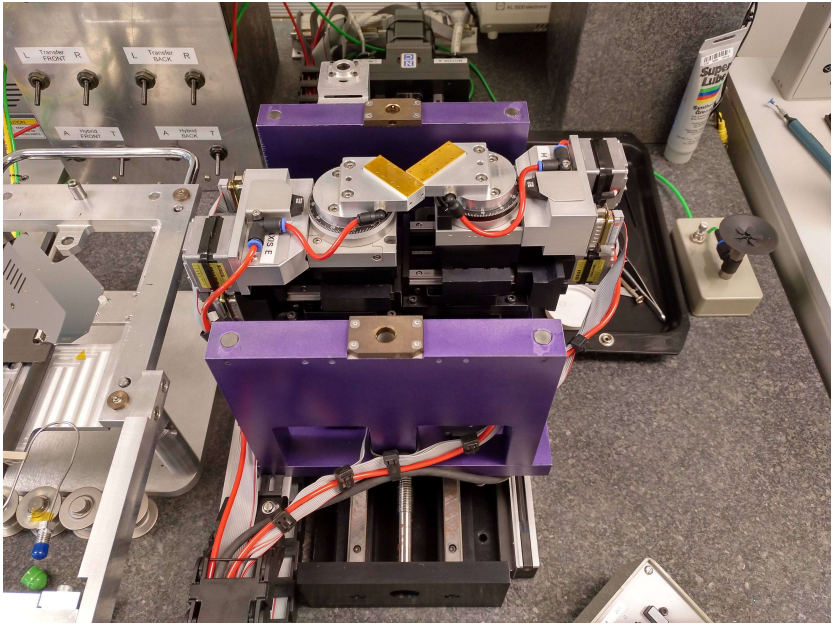
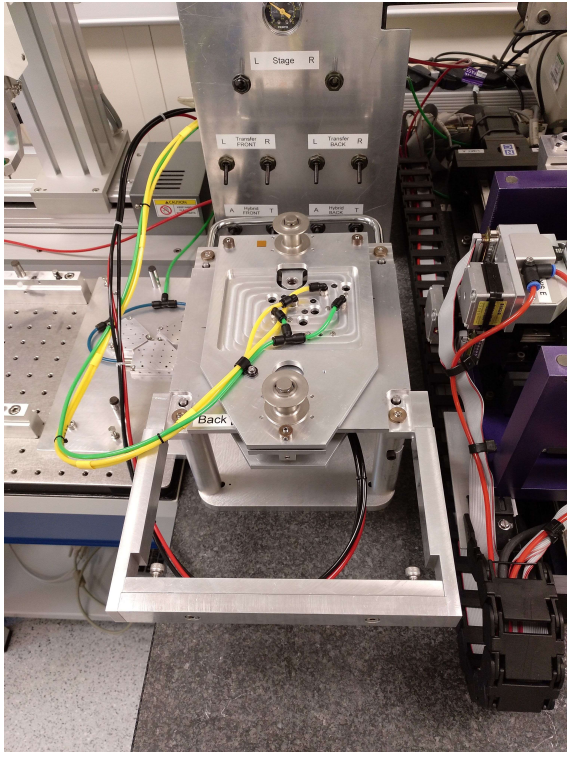
Assembly stages

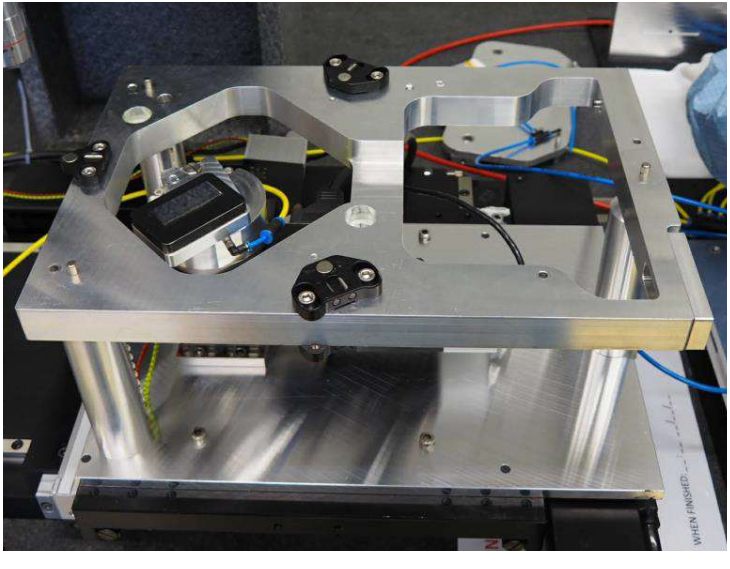


Turn plate + jig

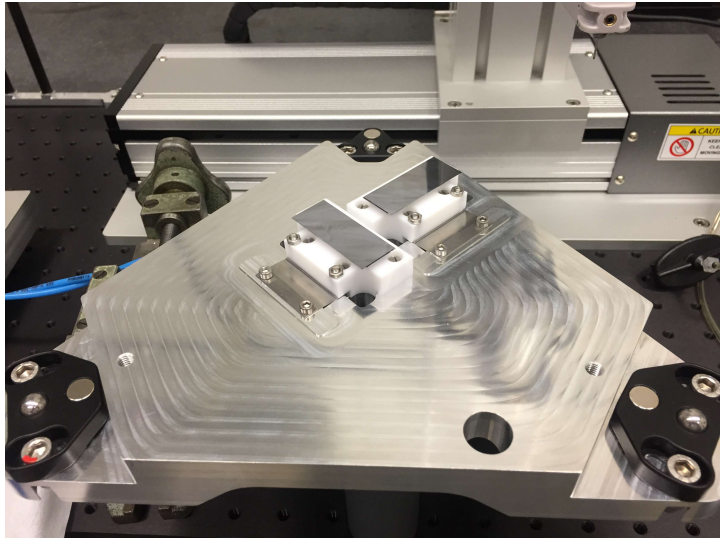


backup

Turn jig in pick&place machine



Transfer jig



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Cooling performance