FCAL detectors

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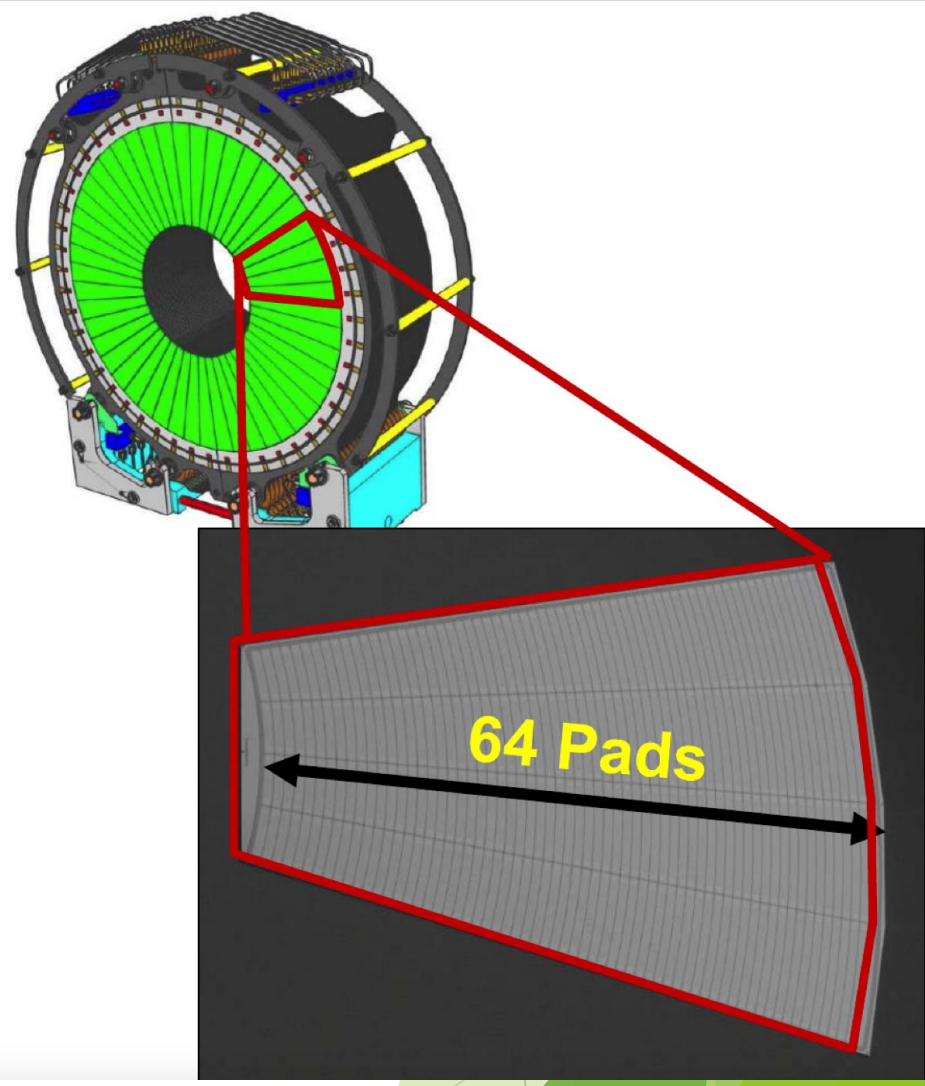
aim of the collaboration

- Build a luminosity detector for the future accelerator:
  - Sandwich tungsten-silicon
  - Ultra compact (1mm in between the tungsten planes)
  - 30-40 layers
  - Fast electronic with high dynamic range
  - Low power consumption
- Last year, we decided to provide the ECAL of the LUXE experiment

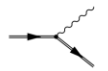
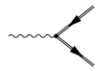
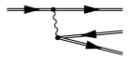


The Laser Und XFEL Experiment (LUXE) experiment at DESY

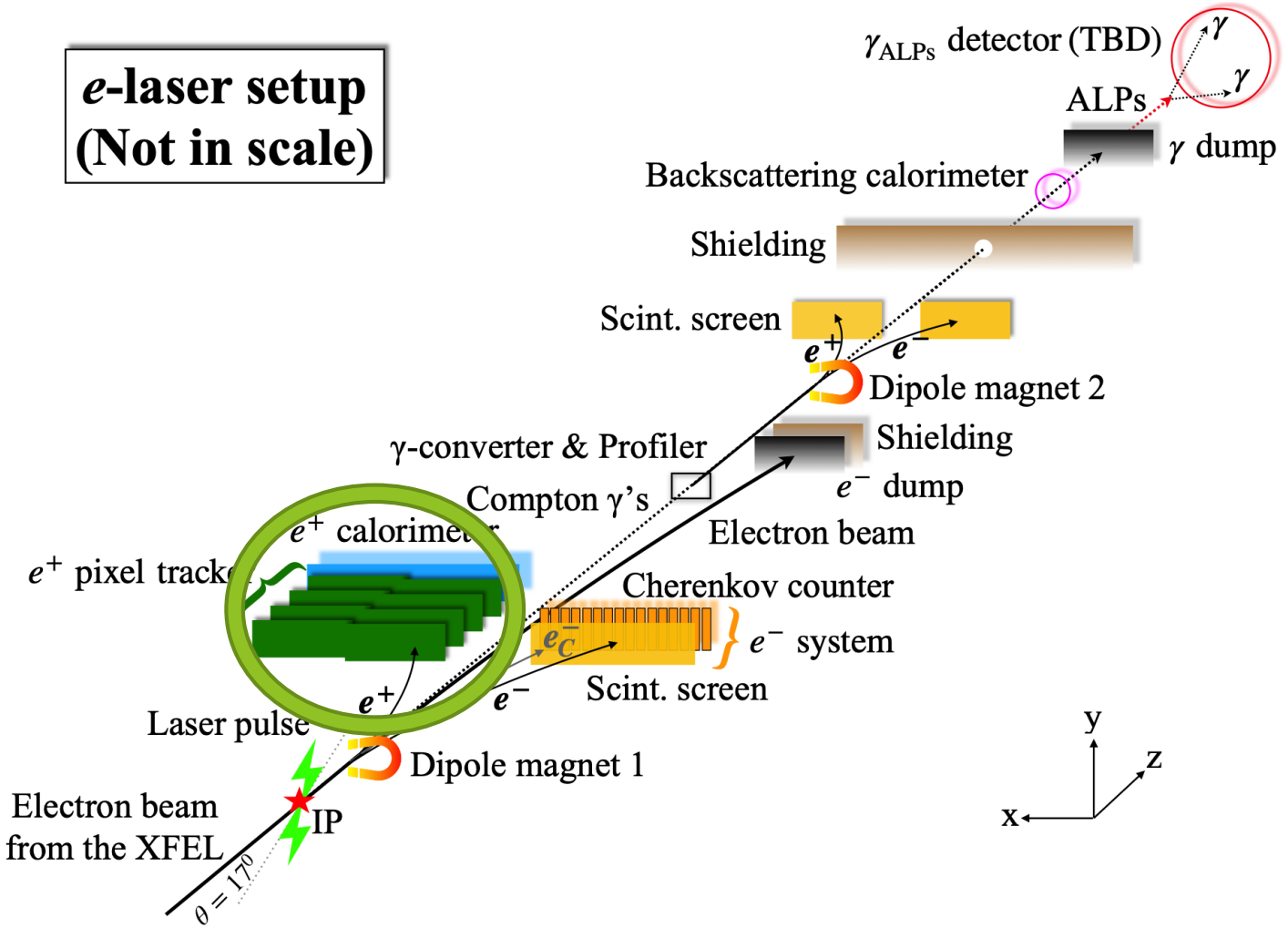
- Interaction between :
  - High energy electron beam (16.5 GeV, **10 Hz**)
  - Powerful laser (40TW/1.2J -> 350TW/10J, **1Hz**)

- Aims :
  - Probe physics at high E field strength at and beyond the Schwinger limit (sparking vacuum) ➔ positron production rates
  - Precise measurements to compare with calculations
  - Search for new physics beyond the Standard Model with intense photon beam from Compton scattering (ALP)

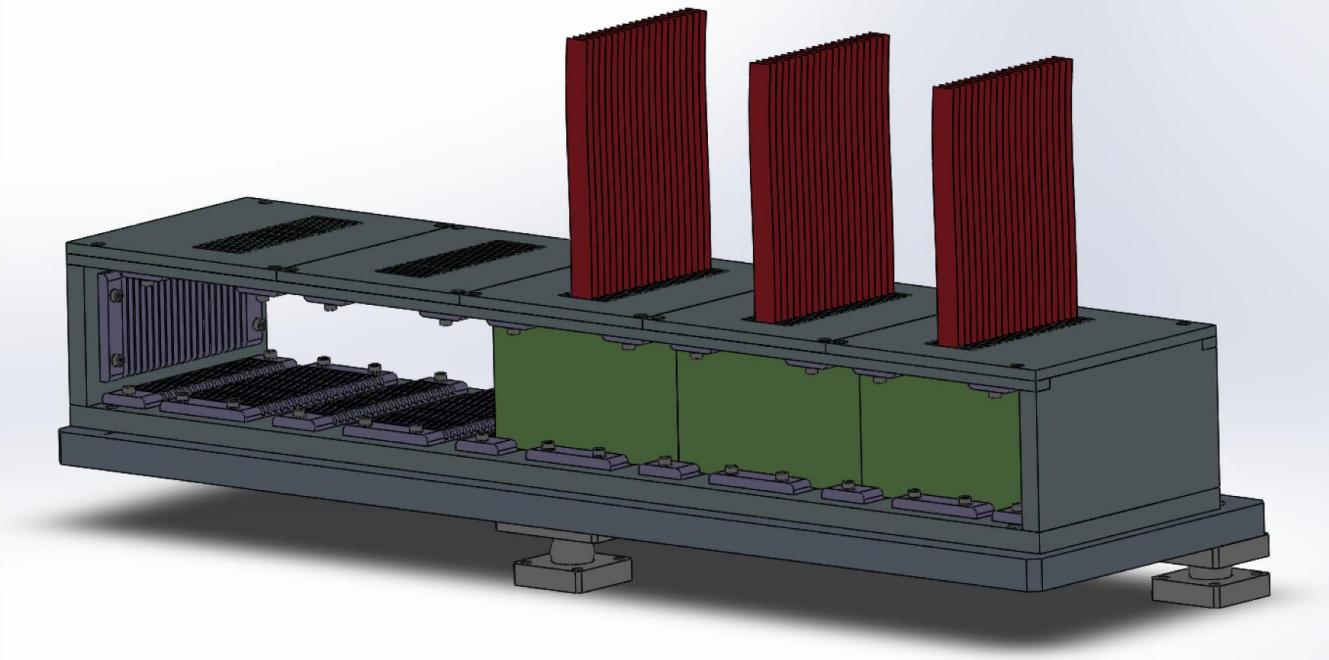
Signature : e^+e^- pair

LUXE Candidate Processes		
	Non-linear Compton	$e^{\pm} \rightarrow e^{\pm} + \gamma$
	Non-linear Breit-Wheeler	$\gamma \rightarrow e^{-} e^{+}$
	Non-linear trident	$e^{\pm} \rightarrow e^{\pm} + e^{-} e^{+}$

Set up of the experiment

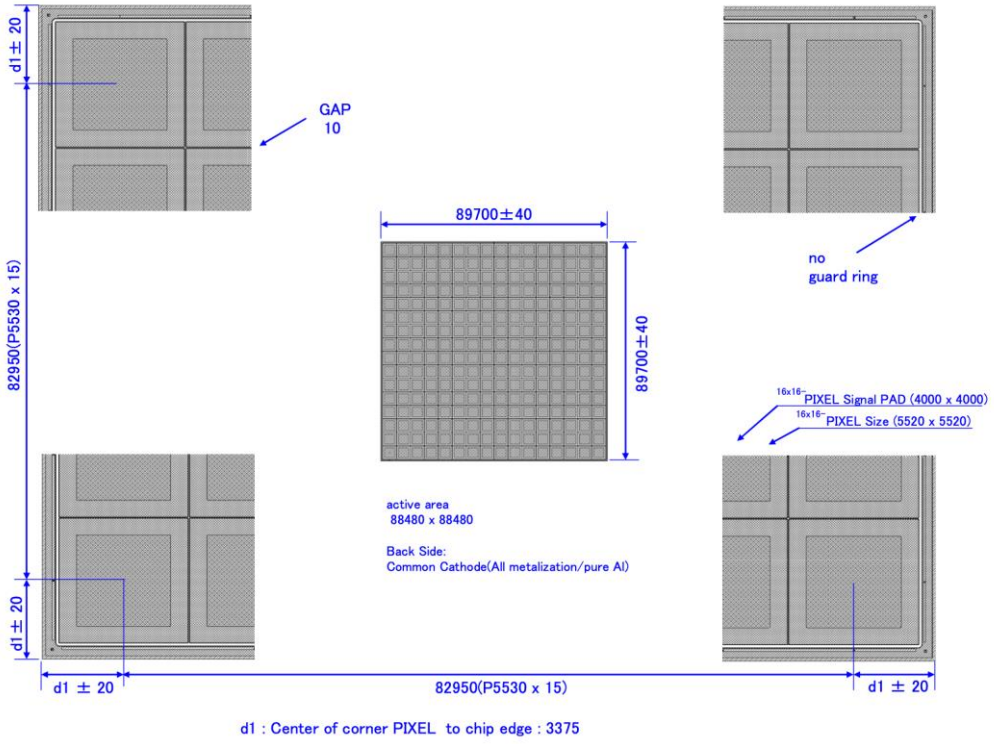


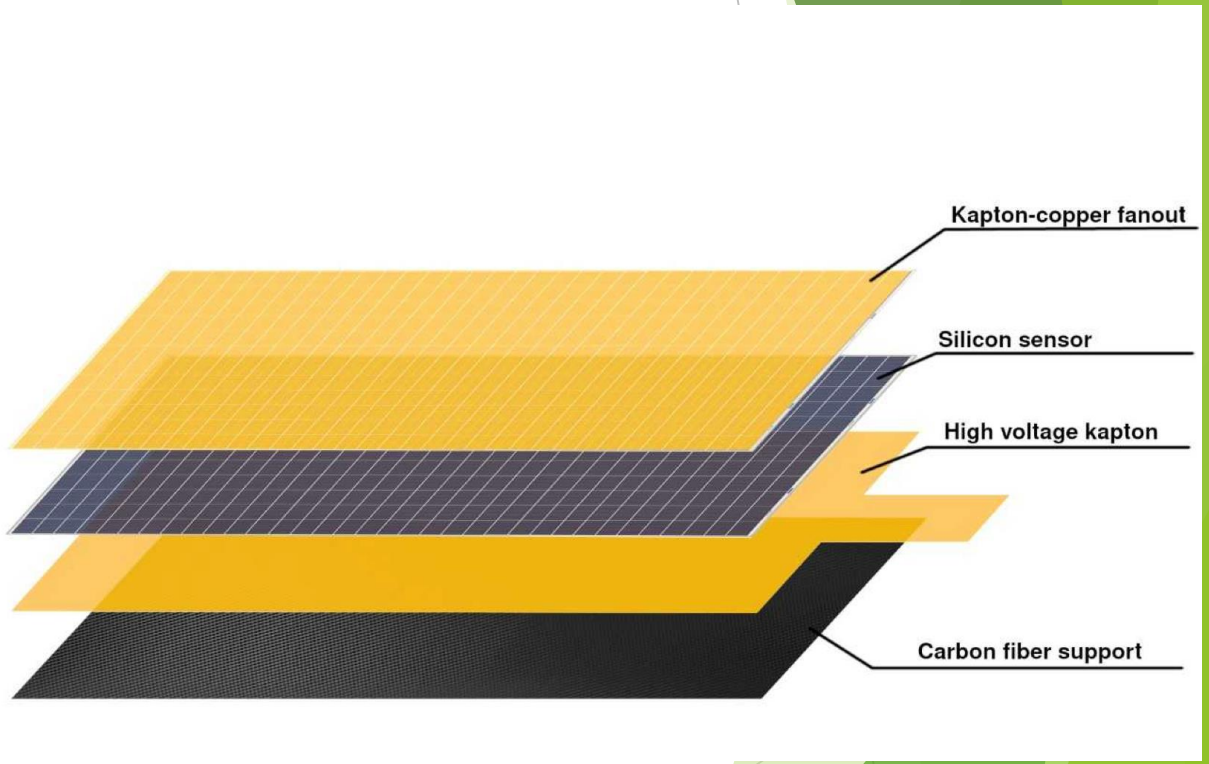
Structure of the Ecal



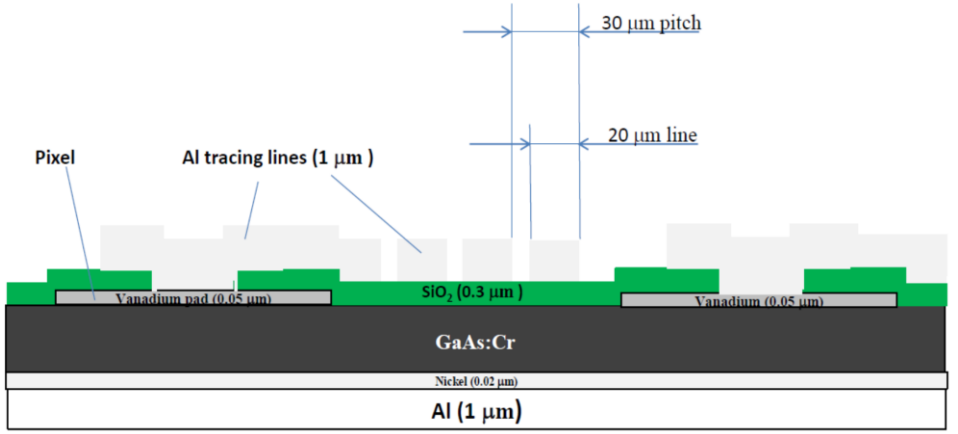
- Sandwich between:
  - Tungsten plane ($1X_0$~3.5mm)
  - Sensor (5x5 mm2 pads) ~150 channels
- 20 layers
- Front face ~55x5 cm2
- Compact in order to maintain the radius of the em shower : 1 mm between tungsten plane

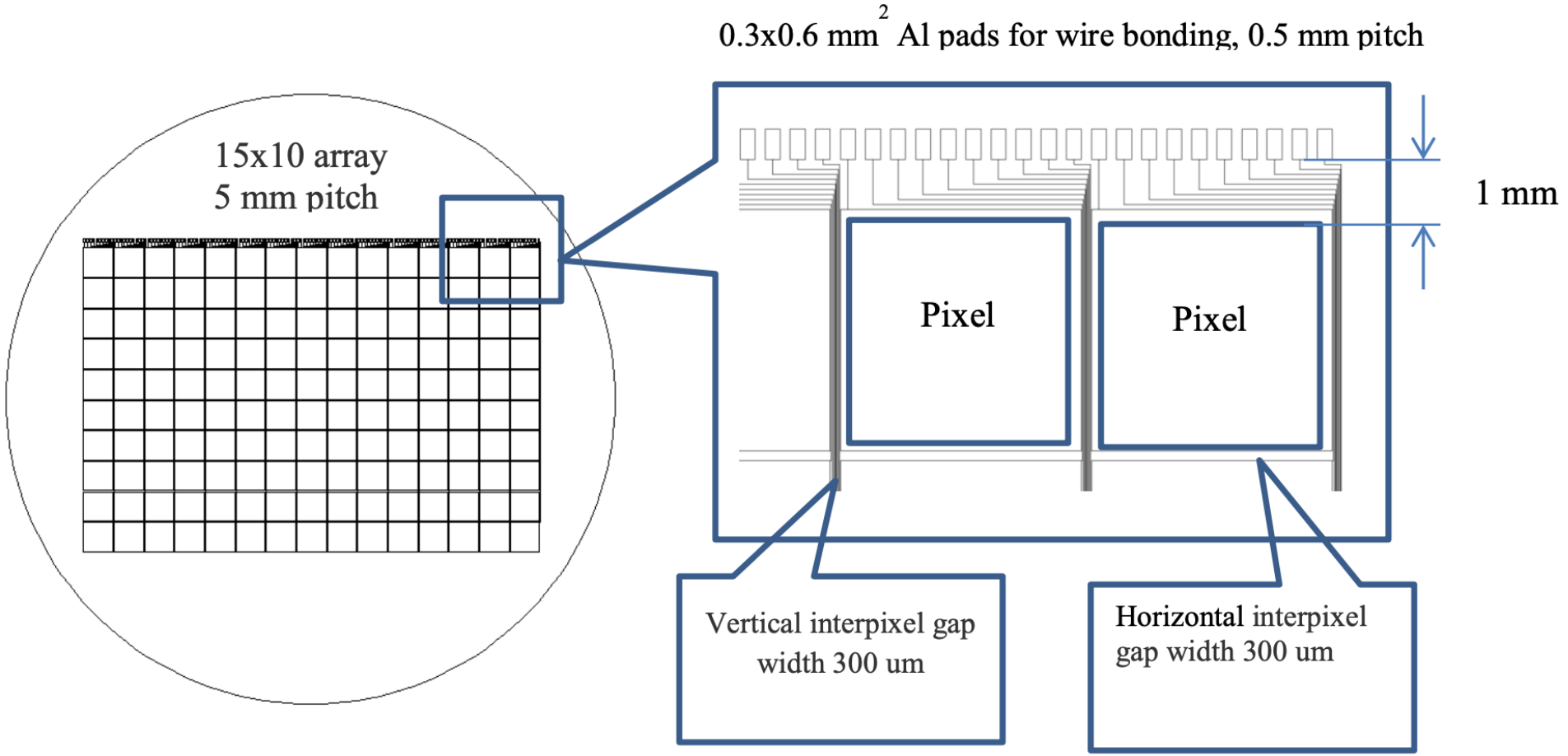
Silicon : wafer of 500 um





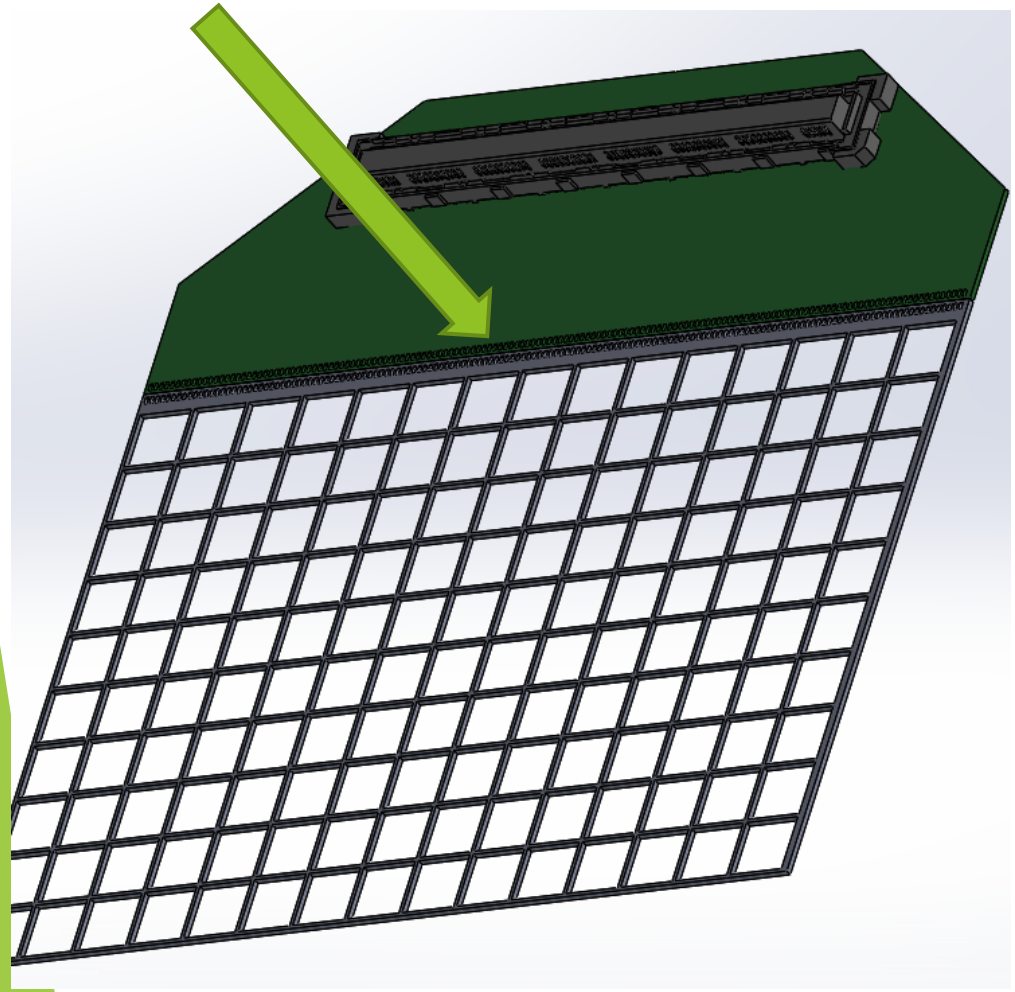
GaAs : wafer of 500 um

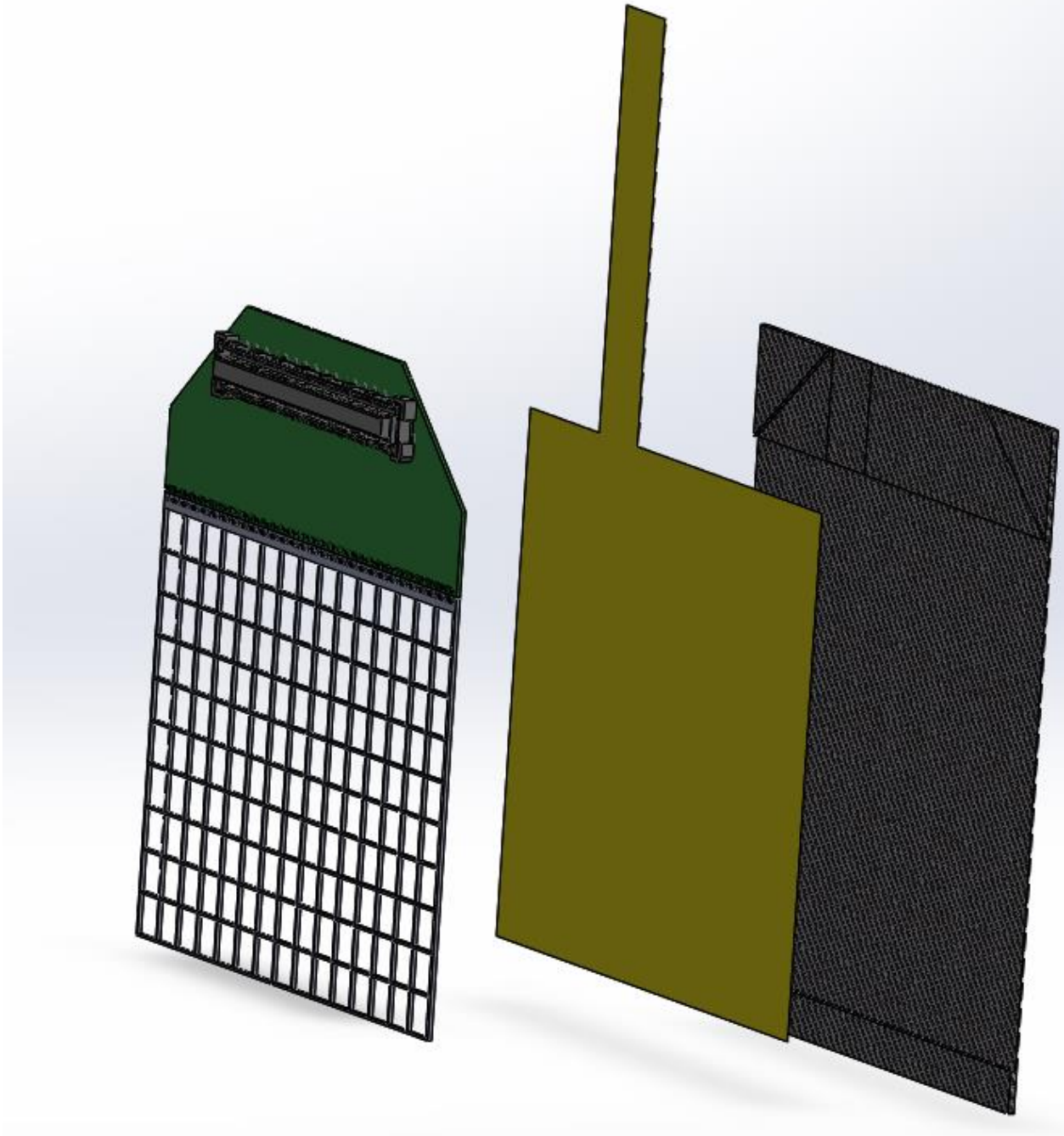




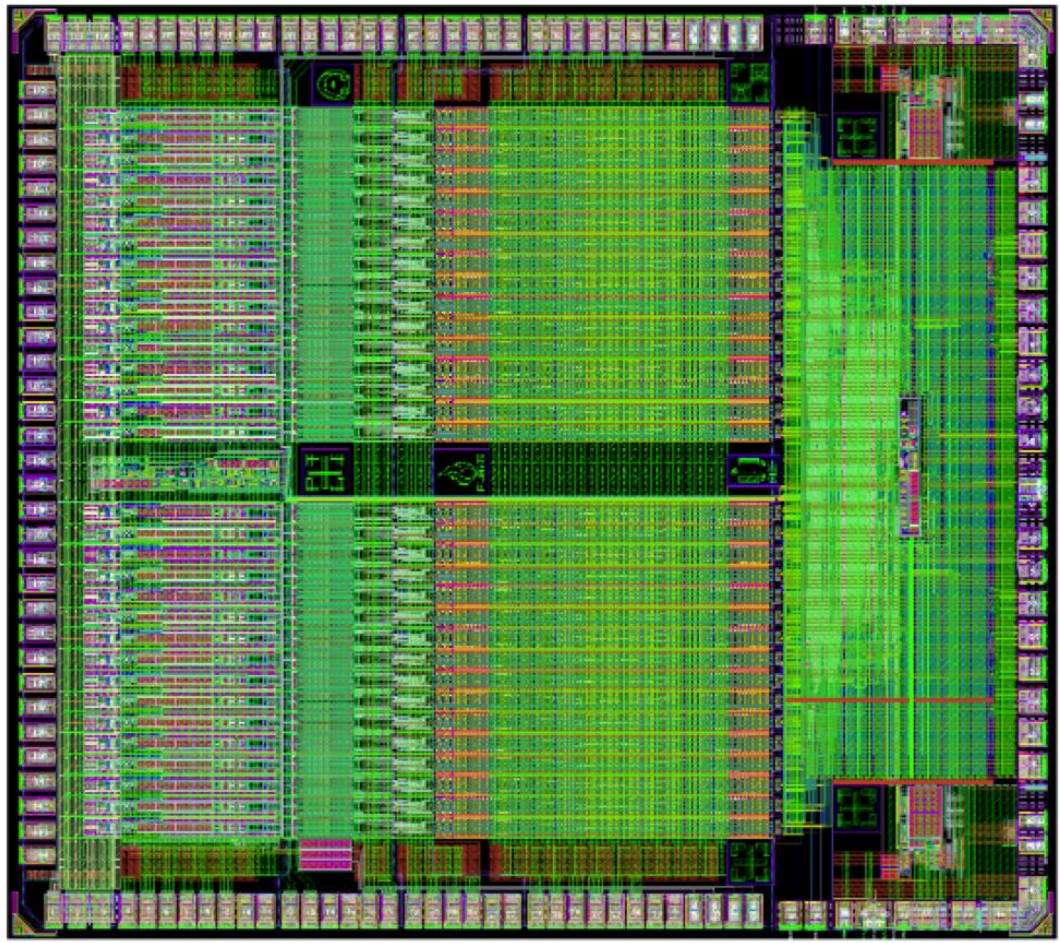
GaAs

Bonding out the fiducial volume



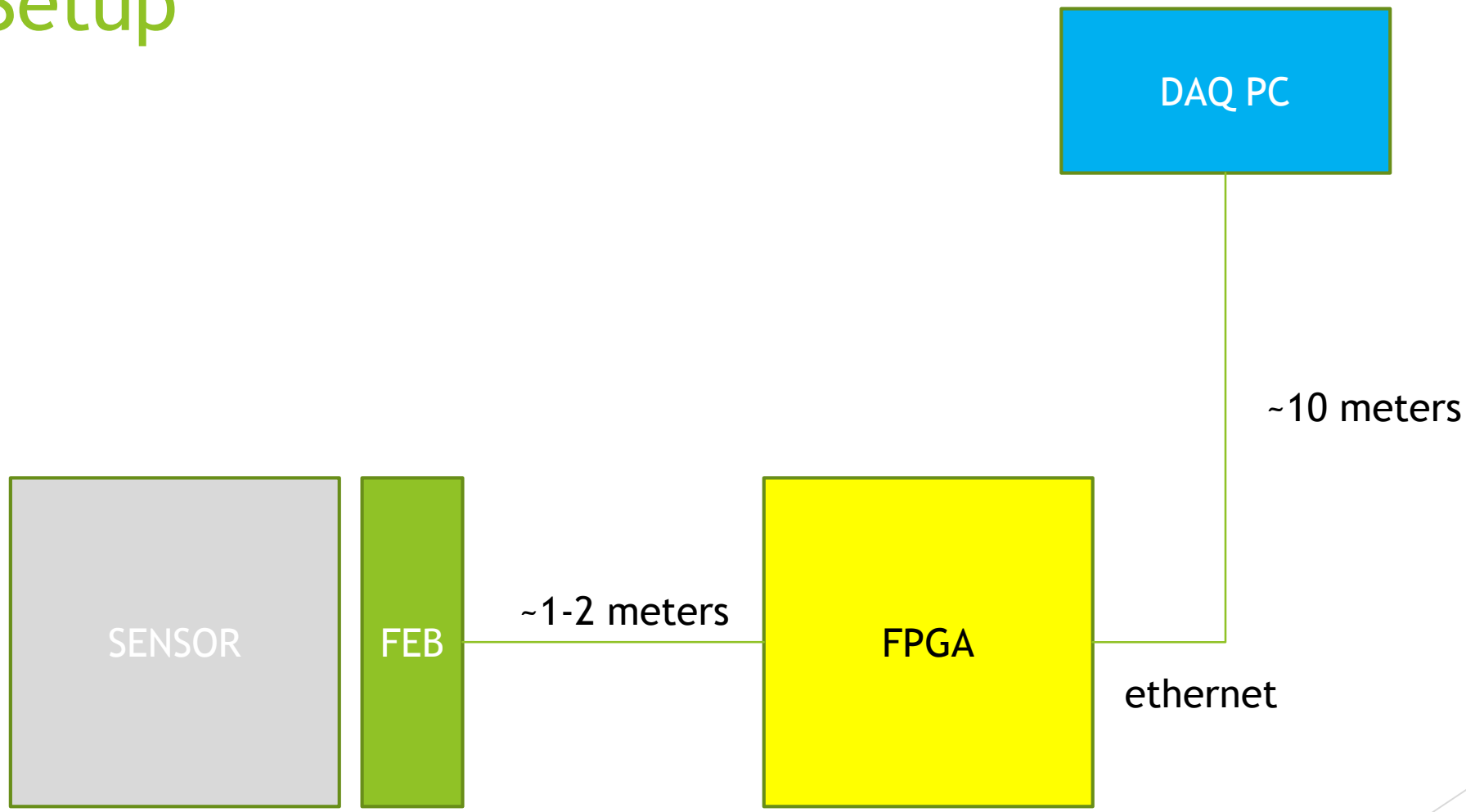


Readout ASIC : FLAME



- 32 mix mode channel comprising:
  - Variable gain front end
  - 10 bit SAR ADC with sampling rate up to 50MSps
  - Ultra low power consumption
- Mutli-phase PLL based fast serializer
- Fast SST driver
- Two 5.2 Gbps links to the FPGA (we need ~5 FLAME per sensor)
- From FPGA to DAQ : zero suppressed and trigger so rate depends on the occupancy and event rate

Setup



Possible to transfer wifi the signal ?

- From FEB to FPGA ?