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Book of Abstracts

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A 3D FPGA Track Segment Seeding Engine Based on the Tiny Triplet Finder

Author: Jinyuan Wu[1]

[1] *Fermi National Accelerator Lab. (US)*

Corresponding Author: jywu168@fnal.gov

An exercise of implementing and testing a 3D track segment seeding engine core based on the Tiny Triplet Finder in a low-cost FPGA device is reported. The seeding engine is designed to preselect and group hits (stubs) from cylindrical detector layers to feed subsequent track fitting stage. The seeding engine consists of a Hugh transform space for r-z view and a Tiny Triplet Finder for r-phi view to implement 3D constraints. The seeding engine is organized as a pipeline so that each hit is processed in a single clock cycle. Test results show that the seeding engine operates as expected.

Summary (500 words):

In most track segment recognition tasks, the first stage, track segment seeding (i.e., grouping the first a few detector layer hits belonging to a track) is one of the most time or silicon area resource consuming operations (not only in online trigger systems but also in offline data analysis). A track segment finding scheme called Tiny Triplet Finder featuring small FPGA resource usage was developed for Fermilab BTeV project. Today, it becomes possible to further utilize more compact FPGA resources such as multipliers (instead of purely using logic elements) to implement the Tiny Triplet Finder with even better resource usage efficiency.

On the other hand, in high luminosity detectors, segment seeding in 2D (in r-phi or r-z plane only) becomes insufficient, since the probability of finding fake segments becomes too high. To reduce fake rate, 3D segment seeding with both r-phi and r-z constraints becomes necessary. Since the Tiny Triplet Finder uses significant less resources than typical implementation methods, it enables the possibility to implement 3D track segment engines with reasonable sized FPGA. The FPGA 3D track segment seeding engines can be used in either online trigger systems or as a co-processor for offline analysis acceleration.

We have exercised implementing a 3D seeding engine core with a 10x256-cell Hugh transform space for r-z view and a 128-bin Tiny Triplet Finder for r-phi view in an Altera Cyclone 5 FPGA (5CGXFC5C6F27C7N) and tested in an evaluation module. In time domain, the seeding engine uses 225 clock cycles to process an event (BX) with 112 cycles to fetch Layer 1 and Layer 3 hits into Hugh transform space and next 112 cycles to pass the Layer 2 hits through the Hugh transform space and Tiny Triplet Finder for 3D coincidence, plus 1 cycle to reset the engine for next event. Up to 112 hits per layer are allowed for each event and a new event is allowed to connect to the previous event seamlessly. (The number of clock cycles, 225 is chosen based on 18x multiplexing in time domain in current arrangement of CMS TFP assuming core clock runs at 500 MHz).

Hits are generated in an idealized detector with diameters and lengths the same as the CMS Outer Tracker PS layers. Each engine core processes a range of detector area 10 degrees x 240 cm. Each event contains 10 good tracks (PT>2GeV/c) plus up to 102 random hits per layer which is higher than the HL-LHC operating condition. The acceptances in various stages are chosen to be as wide as possible so that the final good track acceptance is better than 99%. Under this condition, the fake hit rejection rate is still better than 80%.

The Hugh transform lookup tables and the Tiny Triplet Finder coincidence map are geometry dependent and they are specified with two ROM initiation files and a VHDL file. These files are generated automatically in simulation, which allows accurate coincidence implementation and flexibility of applying the firmware for different detectors and accommodate offsets due to misalignment.

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Isolated USB Programmer for LpGBT (UPL) for the ATLAS-HGTD upgrade

Authors: Liangliang Han[1]; Jie Zhang[2]; Lei Zhang[1]

[1] *Nanjing University (CN)*

[2] *Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)*

Corresponding Author: hanliangliang_1_2@163.com

The CERN developed radiation-tolerant data transmission chip lpGBT will be used on the peripheral electronics board (PEB) of High Granularity Timing Detector (HGTD) in ATLAS. In order to configure the lpGBT on the PEB, we designed a dedicated isolated USB programmer. Compared with the 2 existing lpGBT configuration toolkits, piGBT and CERN USB-I2C dongle, the programmer has very good cross-platform compatibility, electrical isolation performance and compact dimensions, which make it a better choice for PEB configuration.

Summary (500 words):

The increase of pileup will be one of the main challenges in the High-Luminosity LHC. Therefore, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade to mitigate the pileup effects caused by the increasing luminosity of proton-proton collision. The collisions that are very close in space but well separated in time can be distinguished with the high precision timing information provided by HGTD.

The Peripheral Electronics Boards (PEB) are located at the peripheral area of HGTD, and serve as a data transmission bridge between the front-end detector modules and DAQ system, the luminosity system as well as the detector control system. The CERN developed radiation-tolerant data transmission ASIC lpGBT plays a very important role in the data transmission of the PEB.

We designed a dedicated isolated USB programmer, which will be used to configure the lpGBT on PEB in the future. The motive of this design is that the 2 existing lpGBT configuration tools, piGBT and CERN USB-I2C dongle, are not suitable for the configuration of the lpGBT on PEB. For example, the piGBT has large size while the CERN USB-I2C dongle is platform-dependent and no GPIOs available. Moreover, neither of them considered electrical isolation, which is required for PEB configuration.

This design uses the FT232H ASIC chip, which can do the conversion between USB protocol and I2C protocol. Following the FT232H ASIC chip, an I2C isolator is used to electrically isolate the I2C signals from the host side and detector side. Then a GPIO expander and a level shifter can extend more GPIO ports and shift the 3.3 voltage level to lpGBT voltage level respectively. The power supply is also isolated with a power isolator. And the board has only 1 power source, which is the 5V voltage from USB. In addition, a dedicated connector is used, which can match with the connector on PEB.

Therefore, the programmer board has the characteristic of electrical isolation for both signal and power supply. The PEB under configuration would not be interfered by the host side since there are no direct electrical connection between the 2 sides. For example, the high surge voltage from the host side doesn't affect the PEB as well as electrical noises. Another feature of the board is good cross-platform compatibility. The FT232H ASIC chip provides multi-platform supported USB driver, which can work on the operating systems such as Mac OS, Linux, Windows7/8/10, Windows XP, and so on. Moreover, many programming languages such as C++, C#, Python, etc, can be used to control the USB driver.

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Monolithic pixel sensor with 25µm x 35µm pixel size and high time resolution implemented in 180nm technology

Authors: Hui Zhang[1]; Ivan Peric[2]

[1] *Karlsruhe Institute of Technology (KIT)*

[2] *KIT - Karlsruhe Institute of Technology (DE)*

Corresponding Author: hui.zhang@kit.edu

A monolithic pixel sensor named HVMAPS25 has been implemented in a 180nm HVCMOS technology. The pixel size is 25μm x 35μm. The pixel electronics contains a fast and low power charge sensitive amplifier, comparator, threshold tune DAC and a digital circuit that measure the arrival time of the hit with 10 bit resolution, <10ns bin width, and the amplitude (ToT) with 6 bit resolution. The sensor is implemented in a commercial process of TSI Semiconductors on 200Ωcm substrate. Deep p-well has been used for isolation of the pixel electronic from the sensor substrate. The design and measurement will be presented.

Summary (500 words):

The monolithic particle pixel sensor HVMAPS25 has been implemented in the 180nm HVCMOS technology of TSI Semiconductors. The signal charge collection electrodes are small n-wells (2 μm x 4μm) embedded in the high resistivity p-type substrate. The sensor n-wells are AC-coupled to the amplifiers and the can be biased with 10V with respect to the p-substrate. In this way the sensor substrate is partially depleted.
The pixel size is 25 μm x 35 μm. The pixel electronics (NMOS and PMOS transistors) are placed in shallow p- and n-wells and these wells are embedded in the deep p-well used as potential barrier for signal electrons. In this way, we prevent signal loss that could happen if signal electrons drift towards shallow n-wells of PMOS transistors.
The pixel electronics contains a fast and low power charge sensitive amplifier, comparator, threshold tune DAC and a digital circuit that measures the arrival time of the hit with 10 bit resolution and the amplitude (time over threshold) with six bit resolution. Time resolution better than 10ns can be achieved. The current < 1μm for the pixel amplifier.
The sensor could be applied in a vertex detector of some future experiment such as CLIC.
Digital periphery, placed at the bottom of the chip, consist of two blocks, one is the synthesized digital part RCU.
We have performed tests of the overall functionality, measurements of the amplitude response, threshold scan and threshold tune measurements and tests with radioactive sources. The attached figure illustrates the measurement of the digitized amplitude (time of the threshold) versus injected test charge. More measurements and more design details will be presented.

Trigger / **10**

Integration and commissioning of the ATLAS Muon-to-Central-Trigger-Processor Interface for Run-3

Authors: Sabrina Perrella[1]; Andrei Kazarov[2]

[1] *CERN*

[2] *NRC Kurchatov Institute PNPI (RU)*

Corresponding Authors: andrei.kazarov@cern.ch, sabrina.perrella@cern.ch

The Muon-to-Central Trigger Processor Interface (MUCTPI) was completely redesigned as part of the ATLAS Level-1 trigger upgrade for Run 3 of the LHC. The new system is implemented as a single ATCA module, using three large state-of-the-art FPGAs and high-density fibre-optic modules. 208 high-speed links receive trigger information from the muon trigger detectors, while 60 links are used to send processed trigger information to the Topological Trigger and the Central-Trigger-Processor. Extensive integration tests with all input and output systems have shown that the data transfer is stable and reliable. We will also report on the commissioning of the MUCTPI.

Summary (500 words):

The Muon-to-Central Trigger Processor Interface (MUCTPI) is part of the Level-1 trigger system of the ATLAS experiment at the LHC. It interfaces the output of the muon trigger detectors to the Central Trigger Processor (CTP), the Topological Trigger Processor (L1Topo), and the Data Acquisition (DAQ)

system. The MUCTPI receives information on the muon candidates from the muon trigger sectors and calculates the total number of muon candidates for various transverse momentum thresholds taking into account double counting of muon candidates in different sectors due to overlap regions. It further extracts topological information and sends it to the L1Topo.
The MUCTPI has been completely redesigned for Run-3. The new MUCTPI is a highly-integrated system implemented on a single ATCA module, which completely replaces the 18 VMEbus modules of the Run-1/2 system. It uses three large state-of-the-art Xilinx FPGAs (Ultrascale/Ultrascale+) to implement the trigger and readout data processing, and a Xilinx System-on-Chip to control, configure and monitor the board. The MUCTPI receives the muon candidates from 208 muon sector logic modules through high-speed speed serial optical links operating at 6.4 Gbps. Topological information is extracted, sorted by transverse momentum and the data from up to 16 muon candidates is sent to two L1Topo modules over 8 serial optical links operating at 11.2 Gbps. The calculated muon threshold multiplicity triggers are sent to the CTP through a fixed latency serial optical links at 6.4 Gbps. The optical input/output connections are implemented using high-density 12-channel fibre optic transmitter and receiver modules.
Three fully working MUCTPI prototypes have been designed and extensively tested. The performance of the 276 on-board serial optical links has been validated. Eye diagram measurements were used in order to determine the best transceiver settings and to check the eye-opening. In addition, long bit error rate (BER) test runs have been carried out demonstrating that all the links can operate with a BER of less than 10-15. The functional firmware for using the MUCTPI in the experiment has also been developed and extensively tested. Interface tests with the connected subsystems, i.e. the sector logic modules, L1Topo and the CTP, have also been performed successfully. The correctness of data transmission has been verified, using memories to capture the incoming data and CRC checks. Latency measurements for the trigger data links have been performed and shown that the values are within the specifications. One MUCTPI module is currently being installed in the ATLAS experiment.
We will present the results of the integrations tests with all the subsystems, as well as the status of the installation and commissioning of the MUCTPI in the ATLAS experiment.

Systems, Planning, Installation, Commissioning and Running Experience / 11

FELIX: the new ATLAS readout system from Run 3 to High Luminosity LHC

Authors: Frans Schreuder[None]; Frans Schreuder[1]

Co-authors: Michael Begel [2]; Mmathieu Benoit [2]; Filiberto Bonini [2]; Hucheng Chen [2]; Hongbin Liu [2]; George Redlinger [2]; Shaochun Tang [2]; Weigang Yin [2]; Elena Zhivun [2]; Dimitrios matakias [2]

[1] *Nikhef National institute for subatomic physics (NL)*

[2] *Brookhaven National Laboratory*

Corresponding Authors: frans.philip.schreuder@cern.ch, f.schreuder@nikhef.nl

The Front-End Link eXchange (FELIX) system is a new ATLAS DAQ component designed to for detector readout in the High-Luminosity LHC era. FELIX acts as the interface between the data acquisition, detector and trigger timing systems. FELIX routes data between custom serial links from front-end electronics to data collection and processing components via a commodity switched network. This presentation covers the current design of FELIX and its evolution for High-Luminosity LHC, including the development of a new hardware platform based on a Xilinx Versal Prime FPGA, incorporating PCIe Gen4 and a new 25Gbps optical link standard.

Summary (500 words):

In the decade leading up to the High-Luminosity LHC programme, the collider will deliver significantly increasing instantaneous luminosities to experiments such at ATLAS. Alongside the luminosity increase, the number of collisions per beam crossing will also rise, resulting in larger and more complex events for the Trigger and Data Acquisition (DAQ) systems to process. The Front-End Link eXchange (FELIX) system has been developed to meet ATLAS' DAQ needs in this evolving environment. A key goal of this upgrade is to improve the capacity, flexibility and scalability of the detector readout system while also providing a single common platform for all detector components.

FELIX acts as the interface between the data acquisition; detector control and TTC (Timing, Trigger and Control) systems; and new or updated trigger and detector front-end electronics. The system functions as a router between custom serial links from front end ASICs and FPGAs to data collection and processing components via a commodity switched network. The serial links may aggregate many slower links or be a single high bandwidth link. FELIX also forwards the LHC bunch-crossing clock, fixed latency trigger accepts and resets received from the TTC system to front-end electronics. FELIX is being installed and commissioned for a subset of ATLAS detector components ahead of LHC Run 3, before being rolled out for the rest of ATLAS in time for Run 4, the start of the High-Luminosity LHC era.
FELIX uses commodity server technology in combination with FPGA-based PCIe I/O cards to receive data from detector and trigger components. Data are passed between the I/O cards and host server by means of multiple DMA channels. The servers hosting the cards then run a software routing platform which both serves and receives data to and from network peers. Commodity servers connected to FELIX systems via the same network run the new multi- threaded Software Readout Driver (SW ROD) infrastructure for event fragment building, buffering and detector-specific processing to facilitate online selection.
Ahead of High-Luminosity LHC the FELIX system will be upgraded to support higher trigger rates and data volumes, as well as the processing and detector control requirements of the new ATLAS components planned for this time. The SW ROD will also be updated to integrate with the new wider DAQ architecture, featuring a large distributed file store and more dynamic routing requirements.
This presentation will cover the design of FELIX and the SW ROD, as well as their planned evolution for High Luminosity LHC. The results of the installation and commissioning activities from spring 2021 will be presented, alongside those from ongoing High-Luminosity LHC demonstrator programmes.

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FPGA implementation of RDMA for ATLAS Readout with FELIX in High Luminosity LHC

Authors: Andrei Kazarov[1]; Matei Vasile[2]

[1] *NRC Kurchatov Institute PNPI (RU)*

[2] *IFIN-HH (RO)*

Corresponding Authors: matei.vasile@cern.ch, andrei.kazarov@cern.ch

The FELIX system is used as an interface between front-end electronics and commodity hardware in the server farm. FELIX is using RDMA through RoCE to transmit data from its host servers to the Software Readout Driver using off-the-shelf networking equipment. RDMA communication is implemented using software on both end of the links. Exploring opportunities to improve data throughput as part of the High Luminosity LHC upgrade, an implementation for RDMA support in the front-end FELIX FPGA is being developed. We present a proof-of-concept RDMA FPGA implementation, which will help inform the design of the FELIX platform for High Luminosity LHC.

Summary (500 words):

The FELIX (Front-End Link eXchange) system is used for interfacing the front-end detector electronics to the readout system and the high-level trigger farm. The system is based on a custom FPGA board which receives data from the front-end detector electronics via optical links and outputs data via a PCIe interface to a host computer which manages processing and relaying the data further to the readout system. The host computer uses the RDMA (Remote Direct Memory Access) support offered by network interface cards with RoCE (RDMA over Converged Ethernet) support to transmit data further towards the readout systems over an Ethernet network.
In the context of the High Luminosity LHC upgrade, the FELIX board needs to be able to handle a data throughput of 200Gbps, while the FELIX host, integrating two FELIX boards, will have to handle 400Gbps. At these data rates, the transfer operations over PCIe and the required local host processing may become a serious bottleneck. The current FELX board can handle a maximum theoretical throughput of 128Gbps, which is the maximum bandwidth possible with PCIe 3 x16. A possible solution is the implementation of RDMA support in the FELIX FPGA itself. This would mean not using the PCIe interface and the host computer anymore, thus simplifying the data path from front-end detector electronics to the readout system. Not using the host computer anymore, apart from avoiding the limitations of the

PCIe 3 bus, would mean improved throughput and latency because data would not be moved anymore from the FELIX board to the host computer but processed directly on the FPGA before being sent out downstream. Moreover, this drastically reduces the performance requirements of the host system, potentially reducing cost.
The challenge is in exploring the available options and finding the most suitable way of implementing a complex protocol such as RDMA inside the FELIX FPGA. An open source RDMA HLS core has been used as a starting point, which has been modified and expanded in order to make it compatible with existing off-the-shelf networking equipment and integreate our application- specific functionality.
Additionally, software had to be developed to make it possible to set-up connections and exhange data between the RDMA FPGA implementation and a RDMA receiver/server, as well as perform performance tests.
Development of this RDMA FPGA implementation is done on a Xilinx VCU128-Evaluation kit (Virtex Ultrascale+) which integrates on-board DRAM memory and integrated HBM memory. Separately, an Xilinx Alveo system is used as an alternative development platform, particularly taking advantage of the HLS acceleration tools provided by Xilinx. Two PC hosts, with Mellanox
ConnectX-4 and ConnectX-5 cards that support Infinband and RoCEv2 are used toghether with a RDMA-enabled 100Gb Ethernet switch. The main goal is to achieve a 100 Gbps data rate per port, which is the maximum bandwith supported by the available Mellanox cards. In parallel, a Xilinx VCU129 development board with integrated 56Gbps PAM-4 serializers is used to explore the possibility of implementing 400Gbps Ethernet links out of the FPGA.

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Verification of ATLAS detector readout with FPGA-based front-end emulator

Authors: Ricardo Luz[1]; Andrei Kazarov[2]

[1] *Argonne National Laboratory (US)*

[2] *NRC Kurchatov Institute PNPI (RU)*

Corresponding Authors: ricardo.luz@cern.ch, andrei.kazarov@cern.ch

The FrontEnd LInk eXchange (FELIX) is an FPGA-based data router designed to interface custom detector readout systems, and commodity switched networks as part of the ongoing upgrade of the ATLAS experiment at CERN. FELIX relies on synchronous data aggregation with GBT and lpGBT protocols to control and readout multiple detector front-ends. To facilitate validation and benchmarking, we designed and used an FPGA-based emulator of the front-end systems, FELIG. FELIG uses the same hardware as FELIX, FLX-712 board and inherits selected firmware blocks from FELIX. However, FELIG features clock and data recovery and a configurable data generator specifically designed for it.

Summary (500 words):

The FELIG system emulates detector front-ends to verify and benchmark the FELIX system. FELIG can use GBT or lpGBT protocols and generate output data. The output data can be 8b/10b encoded, and the content is configurable. FELIG uses the FLX712 hardware platform, just like FELIX. FELIX and FELIG are interconnected with fiber-optical data links, and FELIG recovers the 40.08 MHz clock from the incoming bitstream.
FELIG was first designed for the commercially available HTG-710 board, and more recently, ported to the latest version of the FELIX custom hardware platforms, the FLX-712. The FLX-712 hosts a Xilinx Kintex UltraScale FPGA and supports 48 high-speed optical links via minipods. Communication with the host computer is performed using a 16 lane PCIe Gen 3 interface connected to two PCIe hardcore EndPoints in the FPGA.
FELIG inherits from FELIX firmware design. A block diagram of the FELIG firmware is attached. Its main components are the link (GBT or lpGBT) wrapper, the emulator, the Wupper PCIe engines, and the clock management module. Both the link wrapper and the Wupper, including the register map, are mostly kept the same as in FELIX. The FELIX central router firmware block, responsible for the interface between the link wrapper and the PCIe wupper, was removed and replaced with the emulator. The clock management also differs from FELIX.

The emulator is configurable, allowing to enable and disable channels as well as choose the e-group widths: 2-bit, 4-bit, 8-bit, 16-bit and soon 32-bit; the data format: 8b10b encoding and direct mode; if LSB or MSB is first; the data chunk length; and the generation trigger: internal (using a counter) or external (sent via TTC by the FELIX board connected to FELIG). The data itself is a countdown from the chunk length to zero with an eight bytes header. Some detector specific data generation modules are now being developed to be part of FELIG.
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Most of the software tools used for FELIX are also available for FELIX since they share the same Wupper and register map blocks. Namely, the initialization procedure for FELIX and FELIG cards uses the same software tool. A toolset called felig-tools was put together to simplify the FELIG configuration procedure. Thus, it is to configure all FELIG relevant registers with simple commands. felig-tools is distributed with the standard FELIX software tools.
For example, a FELIG testing server can host two FLX-712 cards inter-connected via optical links. One of the cards should be running the FELIX firmware version to be tested and connected to a TTC system, while the other is running FELIG.
The GBT version of FELIG, used for the phase-1 FELIX validation, is thoroughly tested and working. Phase-2 FELIG is now being developed. Besides adding the new lpGBT wrapper, it also includes the new FELIX phase-2 wupper and new data formats.
FELIG was already crucial in uncovering some bugs of phase-1 FELIX and is expected to keep being used as a testing and validation tool for the developments coming for phase-2 FELIX.

ASIC / **14**

Performance simulations and characterization of RD53 pixel chips for ATLAS and CMS HL-LHC upgrades

Authors: Attiq Ur Rehman[1]; Jorgen Christiansen[2]; Maurice Garcia-Sciveres[3]; Bjarne Stugu[1]

[1] *University of Bergen (NO)*

[2] *CERN*

[3] *Lawrence Berkeley National Lab. (US)*

Corresponding Author: attiq.ur.rehman@cern.ch

The RD53B pixel readout chip has been submitted for fabrication, meeting specifications of the ATLAS and the CMS experiments for HL-LHC upgrades. Performance characterization of a readout chip in terms of link data rate, average readout latency and efficiency of hit data is essential to evaluate operation of pixel sensors at an extreme interaction rate. At the same time it is complex due to its dependence on various environmental conditions and operational settings. In this work, readout performance parameters and their simulation results for various detector positions of the ATLAS and the CMS experiments are presented.

Summary (500 words):

The Large Hadron Collider (LHC) at CERN is being upgraded to deliver increased luminosity of 7.5 \times 10^{24} cm^{-2}s^{-1}, a factor seven higher than its operation during 2018. Sub detectors of the ATLAS and the CMS experiments are being upgraded to cope with new operational conditions and physics requirement at an unprecedented interaction rate. Silicon based tracker systems of the ATLAS experiment and the CMS experiment will be equipped with new pixel sensors having pitches of 50 µm x 50 µm and 100 µm x 25 µm for phase II upgrade. The RD53 collaboration has designed and submitted readout chips testing and evaluating performance of sensors and their redout electronics. The collaboration has submitted two specific versions of RD53B chips following specifications of each experiment. Both versions of the RD53B chip for the ATLAS (ITK-V1) and the CMS (CROC-V1) differ in terms of required chip size and analogue front ends based on specifications driven by respective experiment. These chips are identical in terms of control, configuration, processing, and readout link interface of the hit data. In this work performance of readout architecture of the RD53B chip is characterized for data rate on readout link under range of operational conditions of the ATLAS and the CMS experiment. Characterization and performance evaluation is performed utilizing Universal Verification Methodology (UVM) based simulation and verification framework developed by the RD53 collaboration. Submitted version

of the RD53B chip is extensively simulated processing detector Monte Carlo (MC) hit data of different positions. Effect of operational environment in terms of hit rate and role of operational parameters related to trigger and readout link settings are evaluated to estimate bandwidth utilization of front-end links and average readout latency. Option to minimize number of front-end links is investigated by simulating and reading out data from four chips via a shared single front-end link. In this work, average readout latency and bandwidth utilization of the shared single front-end link is characterized for various trigger settings. The RD53B chip is equipped with memory buffering hit data while waiting for a trigger which validates buffered data to be readout, named as latency buffer. Saturation of the latency buffer may lead to loss of hit data. This work further includes occupancy studies of latency buffer verifying that implemented size of memory is sufficient handling extreme hit rates without being over saturated. Hit efficiency in terms of lost hits vs total generated hits during a simulation is recorded and compared against specifications. These results are expected to guide in establishing performance benchmarks (data rate, readout latency, hit efficiency) for evaluations of sensors and pixel modules under various environmental conditions (hit rate) and range of operational settings (trigger rate, latency, link speed).

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CIC2: a radiation tolerant 65nm data aggregation ASIC for the future CMS tracking detector at LHC

Authors: Sebastien Viret[1]; Simone Scarfi'[2]; Luigi Caponetto[1]; Geoffrey Christian Galbit[3]; Benedetta Nodari[1]; Sandhya Jain[4]

[1] *Centre National de la Recherche Scientifique (FR)*

[2] *CERN*

[3] *Inst. Nat. Phys. Nucl et Particules (FR)*

[4] *Universite Catholique de Louvain (UCL) (BE)*

Corresponding Author: sebastien.viret@cern.ch

The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-II CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). This data aggregator, designed in 65nm CMOS technology, will be a key element of the tracker front-end chain. A first prototype, CIC1, was tested successfully in early 2019 and was followed by the development of a final radiation tolerant version of the chip: the CIC2. CIC2 design, implementation, and complete test results, are presented.

Summary (500 words):

The Concentrator Integrated Circuit (CIC) ASIC is a front-end (FE) chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker (OT) upgrade at the High-Luminosity LHC (HL-LHC). This 65nm CMOS radiation tolerant data aggregator is a fundamental element on the future detector FE chain.

The main OT feature will be its inclusion at the first level of the CMS trigger system. 40MHz readout of the detector is therefore necessary. To this end, a very innovative detection element, the pT-module, has been developed. The main principle, two silicon layers separated by a few mm, is relatively standard in current tracking systems. Readout electronics, on the other hand, is entirely original. Indeed, for the first time, the signal of the 2 layers will be put in coincidence directly at the module level, thus allowing a significant reduction of the detector output data rate. This coincidence will be performed by a set of 3 very front-end ASICs types: CBC and SSA/MPA for 2S and PS modules respectively. Each pT-module will contain 16 such ASICs, each of them handling the readout of around 120 detection channels.

The CIC handles the data produced by those chips and performs another data compression stage. It receives different input streams from 8 FE chips, either MPAs or CBCs (there are 2 CICs per module), processes them, and finally sends out a standardized data stream to one lpGBT ASIC which transmits the data of both CICs. In average the CIC reduces the data throughput by an order of magnitude. It has to be compatible with both module flavors (different hybrids, voltages, input streams) and his therefore highly configurable.

In order to validate the CIC model, a first physical version, the CIC1, was developed and implemented, along with a complete standalone testbench. This chip, which incorporates all the functionalities of the final system along with the same footprint, was successfully tested in 2019. These results paved the way for a fast second iteration in 2020: the CIC2.

CIC2 could be considered as a pre-production version. It is radiation tolerant and satisfies all the technical requirements of the final CIC chip in terms of data transfer rates and power budget. CIC2 chips were extensively tested in 2020. In particular, SEU and TID test campaigns were conducted in order to qualify the chip behaviour under radiations. All these tests did not revealed any major issue, thus qualifying the CIC2 as a potential candidate for the final version of the chip. However, few minor modifications will be implemented in order to further improve the chip performance. The final chip, CIC2.1, will be produced along with the CIC2 in 2021.

Posters Trigger / **16**

Ultra-low jitter clock distribution for the trigger electronics of the ATLAS New Small Wheel experiment.

Authors: Panagiotis Gkountoumis[1]; Theodoros Alexopoulos[2]; Ioannis Mesolongitis[3]

[1] *CERN*

[2] *National Technical Univ. of Athens (GR)*

[3] *University of West Attica (GR)*

Corresponding Author: panagiotis.gkountoumis@cern.ch

The low radiation levels on the outer rim of the New Small Wheels of the the ATLAS experiment gave the opportunity of utilizing commercial FPGAs for the trigger electronics of the sTGC detectors. The demanding requirements of the Xilinx FPGA transceivers in terms of jitter imposed the development of an ultra-low jitter clock distribution scheme. This scheme includes a custom board placed in the USA15 which distributes 32 clocks over 100 m fiber cables with a jitter of about 700fs. The design techniques for noise reduction and the results are presented.

Summary (500 words):

The LHC at CERN plans to have a series of upgrades to increase its instantaneous luminosity to 7.5×1034 cm−2s−1. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The inner-most station of the ATLAS muon spectrometer, the so-called Small Wheels, will be replaced with a New Small Wheel (NSW) system, consisting of Micromegas (MM) and sTGC detectors, which is expected to be installed in the ATLAS underground cavern during the summer of 2021.
The low radiation levels on the rim of the ATLAS New Small Wheels gave the opportunity of utilizing commercial electronic chips (like Field Programmable Gate Arrays - FPGAs) for the trigger chain of the small-strip Thin Gap Chambers (sTGC) detectors. Those FPGAs require an ultra-low jitter clock for the proper operation of the Gigabit transceivers (4.8 Gb/s serial links). The initial design was based on a radiation tolerant ASIC fabricated at CERN but due to its intrinsic jitter and the high error rate on the transition lines, a different approach had to be chosen. The ASIC was replaced by a custom board named clock distributor based on commercial electronics like jitter cleaners and fanout chips. The new scheme can provide 32 low jitter clocks and achieves a total jitter of about 700 fs over 110 m of fiber cables. The clock distributor board and the whole path were evaluated and extensively tested. In this paper the design techniques for noise reduction and the results are presented.

ASIC / **17**

A radiation tolerant 12 bits, 160 MS/s data conversion and transmission ASIC for the CMS electromagnetic calorimeter

Authors: Gianni Mazza[1]; Stefano Argiro[2]; Dario Soldi[1]; Marco Mignone[3]; Richard James Wheadon[4]; Giulio Dellacasa[5]

[1] *Universita e INFN Torino (IT)*

[2] *Universita di Torino and INFN (IT)*

[3] *INFN sez. di Torino*

[4] *INFN - National Institute for Nuclear Physics*

[5] *INFN Torino (IT)*

Corresponding Author: mazza@to.infn.it

The readout electronics for the CMS Electromagnetic Calorimeter is undergoing a re-design in order to cope with the LHC ugrade. In particular, a fourfold increase in the sampling frequency (from 40 to 160 MS/s) is required. Therefore a new readout ASIC has been developed.
The ASIC, named LiTE-DTU, is designed in a CMOS 65 nm technology. The LiTE-DTU embeds two 12 bits, 160 MS/s ADCs, a time window based sample selection, lossless data compression and 1.28 Gb/s serialization. An on-chip PLL provides the 1.28 GHz clock required by the ADCs and the serializers from the 160 MHz clock.

Summary (500 words):

The High Luminosity LHC (HL-LHC) will require a significant upgrade of the readout electronics for the CMS Electromagnetic Calorimeter (ECAL).
While the detectors will be unchanged (PbWO4 crystals and APD photosensors), new Very Front-End (VFE) and Front-End (FE) cards with their associated ASICs are in advanced state of development.
The new VFE card will be equipped with a fast transimpedance amplifier (named CATIA), capable to follow the input signal shape and therefore more efficient in disentangle pile-up events with respect to the legacy charge sensitive amplifier. It will also have better capability in recognize signals from directs hits in the APD detectors from scintillation signals.
To take full advantage from the new preamplifier, its output signal needs to be sampled at 160 MS/s (i.e. four times the current sampling rate) with a 13 bits resolution. Therefore, a high-speed, high-resolution ADC is required. With these specifications, each readout channel will produce 2.08 Gb/s, in turn requiring a fast data transmission circuitry.
A new ASIC, named LiTE-DTU, was developed to this purpose. The ASIC has been designed in a commercial CMOS 65 nm technology and tested. The LiTE-DTU is designed to work connected on one side to the CATIA amplifier and on the other side to the LpGBT optical transceiver. It embeds two 12 bits, 160 MS/s A/D converters, a time window based sample selection, a lossless data compression and 1.28 Gb/s serializer. An on-chip PLL provides the 1.28 GHz clock required by the ADCs and the serializers from the 160 MHz master clock. The ADC IP block was designed by an external company while the PLL is adapted from the LpGBT low jitter PLL/CDR IP block.
Extensive tests have shown that the ADC is capable to reach the required ENOB of 10.2 bits with an external clock, while with the internal PLL clock the ENOB is limited to 9.7 bits with an input frequency of 30 MHz. The issue has been identified as deterministic jitter due to the coupling between the power supply and the frequency divider in the PLL and will be corrected in the final version. Data selection and compression logic has been successfully tested, as well as the PLL (apart from the extra jitter contribution).
The ASIC was designed to be radiation tolerant to a dose up to 20 kGy and resistant to single event upset. Functional test of the LiTE-DTU and its main building blocks (ADC and PLL) have been performed both before and after irradiation. SEU tests with protons and ions have also been performed. Overall results are very good, albeit a few issues have to be addressed in order to fully comply with the specifications. Test results of the LiTE-DTU coupled with CATIA shows no increase in noise and excellent performance in terms of time and amplitude resolution.

Programmable Logic, Design Tools and Methods / 18

Hough-transform-based FPGA track processor for the ATLAS experiment at CERN

Authors: Tong Xu[1]; Andrei Kazarov[2]

[1] *Argonne National Laboratory (US)*

[2] *NRC Kurchatov Institute PNPI (RU)*

Corresponding Author: tong.xu@cern.ch

The Hough-transform-based FPGA track processing is considered for the trigger system of the ATLAS detector at the Large Hadron Collider at CERN as a part of the upgrade for the High-Luminosity program. The prototype firmware has been developed to evaluate system size. The track processing is organized as a pipeline to increase data processing and clock rates. This Hough transform accumulator can use input pixel and strip hits, stubs, and space-points. It outputs track candidates for bins that meet the track reconstruction requirements. The accumulator is configurable with number of bins in φ and q/pT, and number of input hits.

Summary (500 words):

The ATLAS experiment at CERN will require identification of charged particle tracks for its trigger system. The trigger algorithms are executed using CPUs however, we are considering to offload track identification to FPGAs. To perform pattern match for track reconstruction we have prototyped firmware that uses two-dimensional Hough transform identification with q/pT and ϕ coordinates. The pattern reconstruction is targeting track candidates with pT>1 GeV and |d0|<2mm. Bin sizes of the Hough transform accumulator are driven by the random scattering and the impact parameter range. The prototype firmware has been configured to fit Xilinx Alveo U250 board to evaluate the system size.

The hough transform accumulator firmware operates as a pipeline. Event data are divided into regions and regions are processed separately. Each region corresponds to a slice in η-z0 phase-space to reduce occupancy of the accumulator. Resolution of the ITk hits and space-points is reduced to match the accumulator bins and the full resolution hits and space-points are stored in a buffer. The accumulator cells are loaded with pointers to the buffer and ITk layer information. Once loading is complete, selected cells with appropriate layer patterns are readout for further processing and the pointers are used to lookup the original hits and space-points. The accumulator firmware is configurable with numbers of bin, number input hits, and layer patterns. An accumulator with 256 bins in ϕ, 200 bins in q/pT, 16 hits per cell, and 1023 hit buffer takes about 50% of U250 LUTs. It uses fewer FFs and DPSs. We are exploring ways to reduce the FPGA resource utilization and proximity-based removal of duplicate track candidates.

Posters ASIC / 19

2 ps rms Jitter Analog PLL Running at 2.56 GHz in 130nm CMOS Technology

Authors: Baptiste Joly[1]; Edouard Bechetoille[2]; Herve Mathez[2]; Imad Laktineh[3]; Olivier Lemaire[2]; Patrice Russo[2]; Philippe Vallerand[4]; Richard Vandaele[1]; Samuel Pierre Manen[1]

[1] *Université Clermont Auvergne (FR)*

[2] *Centre National de la Recherche Scientifique (FR)*

[3] *Universite Claude Bernard-Lyon I (FR)*

[4] *Linear Accelerator Laboratory*

Corresponding Author: mathez@ipnl.in2p3.fr

The aim of this work is to develop an internal PLL for ASIC developments which integrates time measurement or which requires an internal clock in the range of GigaHertz. For future upgrades in High Energy Physic detectors experiments, time measurement becomes a decisive element, which will make it possible to reduce the data flow and improve the spatial accuracy of the interaction point. This design is based on a top down design methodology including a behavioural and a linearized PLL. Two PLLs were designed with two different VCOs based on ring and LC tank oscillator.

Summary (500 words):

Introduction:
Two PLLs were designed to evaluate the jitter performance and the silicon area required. The first PLL implements a ring oscillator architecture. Integrated PLLs use ring oscillator as VCO for lower silicon area. However, the low damping factor (at most equal to $\pi/2$) of these oscillators permits to achieve few ps rms PLL jitter. The second one uses a LC oscillator for its higher Q factor. VCO based on LC tank oscillator have damping factors greater than 10, which results in ultra-low jitter PLLs. A Verilog-A model PLL and a linearized one was designed to scale intrinsic jitter of each block and stability.

Architecture:
The block diagram of a PLL operating as a clock generator is shown in figure 1. It consists of a frequency reference input (Fref), a phase/frequency detector (PFD), a charge pump (CP) with its output current (Icp), a low pass loop filter (LF) with its equivalent impedance (Zlp), a voltage controlled oscillator (VCO) with its conversion gain (Kvco) and a frequency divider (FD) with its divider ratio (N). The feedback loop acts to equal in phase Fref (40 MHz) and Ffb. When the PLL is locked, the frequency at the output is 2.56 GHz.

Test results:
The bandwidth of the output driver is limited to 1.5 GHz and the maximum output divider frequency recordable is 1.28 GHz. For the two PLLs, one can plot the output phase noise in dBc/Hz from 40 MHz to 1.28 GHz (figure 2 and 3). As predicted, all the curves are separately by 6 dB. For both PLLs, some peaks at frequencies multiple of 40 MHz are observed. For the specific case of the ring oscillator PLL, additional peaks at frequencies not multiple of 40 MHz are present. A peak in phase noise plot at 12 MHz is observed in figure 2. This frequency is an alias of the frequency of the standalone VCO divided output (628 MHz, cf figure 2). The final absolute jitter at 1.28 GHz in ps rms is evaluated from the phase noise plots and extrapolated for 2.56 GHz output. The absolute jitter are respectively 2.05 ps rms for the ring oscillator PLL and 1.6 ps rms for the LC tank oscillator PLL. Offline analysis at 1.28 GHz for the two PLLs allows to plot the absolute output jitter (figure 4 and 5) as a function of the offset frequency carrier. This two set of curves are well in accordance.

Conclusion:
We have designed two low jitter PLLs using a top down methodology. A Verilog-A behavioural PLL has been qualified in terms of jitter for all blocks of the PLLs. The absolute output jitter calculated from the phase noise plots are 2.05 ps rms for the ring oscillator architecture and 1.6 ps rms for the LC tank oscillator.
Possible improvements are reducing internal couplings, optimizing VCOs jitter and therefore minimizing output PLL jitter. Ring oscillator with Injection locked architecture is a promising way of improvement.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 20

Design and testing of a long Flexible Printed Circuit for the ATLAS High Granularity Timing Detector

Author: Maria Robles Manzano[1]

[1] *Johannes Gutenberg Universitaet Mainz (DE)*

Corresponding Author: maria.robles.manzano@cern.ch

The High Granularity Timing Detector for the ATLAS upgrade is under construction to meet the challenges of the HL-LHC. The silicon detectors along with the electronics are installed in two double-sided disks per end-cap and consist of basic units (called modules) connected to the peripheral electronics by Flexible Printed Circuit cables. The reduced space between disks and the positioning constraints as well as the large number of modules pose additional challenges for the power supply distribution and the readout system. We present the design and test results for a 2-layer flexible PCB with a maximum distance of 75cm between connections.

Summary (500 words):

The High Granularity Timing Detector (HGTD) for the ATLAS Phase II upgrade is being built to meet the demands of the High Luminosity LHC and provide a time measurement per end-cap track with a resolution of about 30 ps. This detector consists on two double-sided disks equipped with 8034 modules, two ASICs bump-bonded to two Low Gain Avalanche Detectors (LGAD) in turn glued to a flexible PCB, and is contained in a 75 mm thick vessel. The Peripheral Electronic Boards (PEB), PCBs dedicated for power and readout, surround the ring-shape active area where the modules are distributed. The interconnection between each module and the PEB is realized by a Flexible Printed Circuit (FPC), called FLEX tail. The compact design of the HGTD requires a custom design of the FLEX tail, constrained geometrically by the space available between two disks and the number of modules (220 mum thickness maximum) as well as the positioning of the modules and their connection on the PEB, defining the length. As a result, the FLEX tail length ranges from 3 cm to 69 cm. The electrical constraints are similarly challeging, including
dedicated differential pairs for signal transmission for a 1.28 Gbps maximum rate, together with dedicated lines for clock distribution and control. Moreover, planes for powering and grounding are required for the ASIC in addition to a High Voltage (HV) line to bias the LGAD sensors (800V at 3 mA). The impedance of the lines is required to be in a between 90 and 120 ohm for the differential pairs and 50 to 65 ohm for single lines for a proper impedance matching. Those constraints require a careful design, manufacturing and exhaustive testing. As part of the R&D program of the FLEX tail, a 2-layer FPC prototype has been designed and tested. The length of the prototype is 75 cm, longer than the designed length for testing purposes. It includes the lines for one module, i.e. differential pairs for communication, clock and data, single lines for control and dedicated planes for power (1.2V at 1A) and ground and a line for HV. An adapter board was designed for the FPC prototype testing. The impedance
of the differential pairs and single lines were verifed via a Time Domain Reflectometer (TDR). The voltage drop of the power and ground planes was also evaluated and compared with post-layout simulations. With regard to the signal transmission performance, a setup based on a Kintex Ultrascale+ evaluation board emulates the realistic conditions of the FLEX tail in normal operation.The Integrated Bit Error Rate Test (IBERT) provided valuable information, having no errors detected over several days of measurement. The in infuence of the HV bias on the high-speed digital logic was also estimated. Those tests were performed at room temperature and at -30℃, the HGTD operational temperature in addition to optical tests to estimate the thermal contraction at those temperatures.

Posters ASIC / 21

Radiation hardness of the ITkPixV1 and RD53A chips

Author: Maria Mironova[1]

[1] *University of Oxford (GB)*

Corresponding Author: maria.mironova@cern.ch

The ITkPixV1 chip is the pre-production pixel readout chip for the Phase-2 Upgrade of the ATLAS experiment at the HL-LHC. The harsh environment of HL-LHC, including a peak luminosity of 5x10^34cm-2s-1 and an estimated total ionising dose (TID) of more than 500 Mrad throughout its lifetime is placing strong requirements on the radiation tolerance of the chip. This contribution outlines investigations into the radiation tolerance of ITkPixV1. The impact of TID damage to the digital and analog front-end up to total doses of 1 Grad (at dose rate 4 Mrad/h) is reported.

Summary (500 words):

The ATLAS experiment at the LHC will upgrade its entire tracking system around 2026 in preparation for the High Luminosity LHC (HL-LHC). This includes a new system of five layers of silicon pixel detectors, which will face the challenges of an increase in pile-up and luminosity by an order of magnitude. The new inner tracker (ITk) will consist of hybrid pixel detectors with smaller pixel pitch to provide higher granularity and better resolution. It will also include a novel readout chip with increased bandwidth and improved radiation hardness. The chip is designed by the RD53 collaboration, with the latest prototype of the ATLAS readout chip being ITkPixV1, which has 50 x 50 μm pixel pitch and a total of 384 x 400 pixels.

The radiation tolerance of ITkPixV1 can be studied in irradiation campaigns. The chip is equipped with ring oscillators to characterise the radiation damage on digital circuits. In this contribution, the TID damage to the ring oscillators up to total doses of 1 Grad at a dose rate of 4 Mrad/h is discussed, as measured in irradiations using X-rays with energies between 10 and 30 keV. The irradiations are performed at a temperature of -10 C, and no annealing is considered, as the chip is kept cold. Results from low dose rate irradiations using X-rays and electrons from Kr-85 are also presented. The impact of metallisation layers on the chip on the delivered dose is discussed. The effect of radiation damage on the analog front-end is also reported, by studying the threshold dispersion with irradiation and the performance of the analog front-end at 400 Mrad and 1 Grad.

ASIC / **23**

Towards the next generation of CERN radiation monitoring front end ASICs

Author: Sarath Kundumattathil Mohanan[1]

Co-authors: Hamza Boukabache [2]; Daniel Perrin [2]; Ullrich Pfeiffer [3]

[1] *Bergische Universitaet Wuppertal (DE)*

[2] *CERN*

[3] *University of Wuppertal*

Corresponding Author: sarath.mohanan@cern.ch

The front-end electronics of Ionization chamber for radiation protection demands challenging sensitivity requirements in the femtoampere range and a wide dynamic range. This work details the development trajectory that culminated in a single chip solution with current measurement capability spanning nine decades. The various Application Specific Integrated Circuits designed in the Radiation Protection team at CERN are explained. The challenges faced and the methodology adopted in designing ASICs for ultra-low current measurement is detailed. The latest version of the ASIC designed in 130nm technology can measure currents from -6 fA to -20 μA with an accuracy of 7%.

Summary (500 words):

ARCON and RAMSES are the two pillars that cemented the radiation protection and monitoring sphere of CERN. With the in-house developed next-generation radiation monitors- CROME, the legacy systems are getting replaced. This SoC-based SIL2 compliant modernized front end of the Ionization chamber is state-of-the-art technology. However, to mitigate the risks of obsolescence that might hinder the development in the future and to reduce the industrialization complexity process, an in-house development of ASICs for radiation monitoring was taken up. In this program, five series of ASICs were developed.
The first two families of ASICs named UTOPIA were designed in 350 nm technology. UTOPIA 1 identified the main sources of leakage in a typical current to frequency (CFC) based current measurement architecture in the 350 nm technology. UTOPIA 2 increased the measurement span to 9 decades and can measure current from -1 fA to -5 μA.
As the fab which provided the 350 nm technology started limiting the support for new designs, and with the need to have improved performance in pulsed radiation fields, newer technology nodes were evaluated for designing a future version of the ASIC. As the technologies scale down, the leakage currents

increase which was hindering the use of advanced nodes for ultra-low current measurements. A technology demonstrator chip in GLOBAL FOUNDRIES 22nm technology established techniques of using thick gate transistors in the critical path to minimize leakage thus enabling the use of such technology nodes for low current measurements.
By following a similar approach, another ASIC in TSMC 130 nm was designed which compared different current measurement topologies and successfully demonstrated a measurement range from -1 fA to -1 μA. Among the three architectures compared – it was found that the direct slope measurement method was a good choice for fast low current measurement in the femtoampere range and charge balancing method for current from picoampere to microampere range.
The newest version of the ASIC designed also in 130 nm technology incorporated the two current measurement topologies and could attain an ultra-wide dynamic range from -6 fA to -20 μA. An increased feedback capacitor of the CFC along with a dedicated channel for generating high charges for measurement in the microampere range helped in increasing the dynamic range. The increase in the time of measurement resulted from higher feedback capacitor was compensated by the fast results from the direct slope method channel. Thus, a high-speed wide-band ultra-low current measurement system was realized. The ASIC meets the stringent requirements acting as a versatile front end for the Ionization chambers for future radiation monitors at CERN.

Posters Radiation Tolerant Components and Systems / 24

Test of Low-Dropout voltage regulators with neutron and protons

Authors: Sergey Abovyan[1]; Varuzhan Danielyan[1]; Markus Fras[1]; Robert Richter[1]; Oliver Kortner[1]; Hubert Kroha[1]; Iacopo Longarini[2]; Massimo Corradi[2]; Riccardo Vari[2]; Riccardo Lunadei[3]; Panagiotis Gkountoumis[4]; B. Bianchi[5]; M Cesaroni[6]; Luca Falconi[6]; A Ratto[6]; P Ricci[6]; Alfonso Santagata[6]; Patrick Berger[7]; Miriam Modjesch[8]

[1] *Max-Planck-Institut fur Physik (DE)*

[2] *Sapienza Universita e INFN, Roma I (IT)*

[3] *Istituto Nazionale di Fisica Nucleare Sezione di Roma 1*

[4] *CERN*

[5] *Enea, centro ricerche Casaccia*

[6] *Enea, Centro Ricerche Casaccia*

[7] *Unknown*

[8] *Max Plank Institute, Munich*

Corresponding Author: iacopo.longarini@cern.ch

The ATLAS Muon System will be upgraded for the High-Luminosity phase of LHC. Its new on-detector electronics should withstand a non-ionizing dose equivalent to 10^13 n/cm2 (1 MeV eq on Si) and have a negligible rate of single-event effects. Commercial low-dropout (LDO) voltage regulators have been considered as a practical solution for powering on-detector electronics. We present results from the irradiation of 7 types of CMOS LDOs at the fast neutron reactor RSV TAPIRO at ENEA Casaccia (Roma) and at the 200 MeV proton beam at PSI (Zurich).

Summary (500 words):

The Muon System of the ATLAS experiment at CERN LHC will be upgraded for the high-luminosity phase of LHC to cope with higher rates and higher radiation levels.
Most of the Muon-System on-detector electronics will be replaced. Commercial low-dropout (LDO) voltage regulators have been considered as a robust, low-noise and economic solution to power distribution. The appropriate COTS components should be selected based on their capability to comply to radiation requirements.
The requirement for non-ionizing energy loss (NIEL) for the new electronics is 1013 n/cm2 (1 MeV equivalent on Si). The fluence of high energy (E>20 MeV) hadrons will be up to 1011 hadrons/cm2 during 10 years of operation. For reliable operation, the LDOs should provide stable output voltage, have a very small rate of recoverable failures (SEE) and a negligible number of destructive failures. We tested 7 different types of CMOS LDOs, monitoring online the output voltage of 10 samples of each

type. Irradiations were performed in the Radial Channel 1 of the RSV TAPIRO fast neutron reactor at ENEA Casaccia (Roma), to test resistance to NIEL, and at the PIF 200 MeV proton beam at PSI (Zurich), to test SEE. The experimental setup and the results are presented and discussed in this communication.

Production, Testing and Reliability / 25

Frontend and backend electronics for the ATLAS New Small Wheel Upgrade

Authors: ATLAS Muon Collaboration[None]; Siyuan Sun[1]

[1] *University of Michigan (US)*

Corresponding Authors: siyuan.sun@cern.ch, shikma.bressler@cern.ch

The present ATLAS innermost endcap muon station will be replaced by a New Small Wheel (NSW) detector to handle large trigger and readout data rates expected at high luminosity LHC runs. Two new detector technologies, Resistive Micromegas (MM) and small-strip Thin Gap Chambers (sTGC), will be used for triggering and tracking. A common readout path and two separate trigger paths are developed. It is challenging to integrate and commission this complicated detector-electronics system with 128 MM and 192 sTGC detector modules and 2.4M readout channels. I will discuss the design of the NSW electronics and the status of detector-electronics intergration.

Summary (500 words):

To maximize the physics reach, the Large Hadron Collider (LHC) plans to increase its instantaneous luminosity to 7.5×1034 cm-2s-1 and deliver 3,000-4,000 fb-1 of data at a center-of-mass energy of 14 TeV. The luminosity increase will drastically impact the ATLAS detector, trigger and readout system. To retain the good precision tracking and trigger capabilities in the high background environment of the high-luminosity LHC, the present ATLAS innermost endcap muon detector will be replaced with a New Small Wheel (NSW) detector. The NSW will feature two new detector technologies, Resistive Micromegas (MM) and small strip Thin Gap Chambers (sTGC). Both detectors will be used for muon triggering and precision tracking.
A common readout path and two separate trigger paths are developed for these two detector technologies. The frontend electronics are implemented in about 8000 printed circuit boards including the design of four ATLAS customly-designed ASICs capable of driving trigger and tracking primitives to the backend trigger processor and readout system. The readout data flow is performed through a high-throughput network approach. Tasks such as time, trigger and control signal distribution and readout are performed by several ASICs developed by CERN.
The large number of readout channels, short time available to prepare and transmit trigger data, large volume of output data, harsh radiation environment, and the need of low power consumption all impose great challenges on the design, integration and commissioning. Extensive work is ongoing with the NSW detector and electronics at CERN. It is extremely challenging to perform integration and commissioning for this large and complicated detector-electronics system with 128 MM and 192 sTGC detector modules (each module contains four layers of MM or sTGC detector) and ~2.4 million readout channels. Various issues have been found and corrective actions have been implemented. The overall design of the NSW frontend and backend electronics and the status of the detector-electronics intergration and commissioning will be discussed, along with results from noise runs and cosmic rays.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 27

A complete readout system for the CGEM detector

Author: Michela Greco[1]

Co-author: BESIII Italian Collaboration

[1] *INFN- Torino; University of Torino*

Corresponding Author: greco@to.infn.it

An innovative Cylindrical Gas Electron Multiplier (CGEM) detector is under construction for the upgrade of the inner tracker of the BESIII experiment. A novel system has been worked out for the readout, including a new ASIC, dubbed TIGER, designed for the amplification and digitization of the CGEM output signals. The data output by TIGER are collected and processed by a first FPGA-based module, GEM Read Out Card, in charge of ASIC configuration and control. A second FPGA-based module, GEM Data Concentrator, builds the trigger selected event packets containing the data and stores them via the main BESIII data acquisition system.

Summary (500 words):

A ten years extension of the data taking of the Beijing Electron Spectrometer (BESIII) experiment, recently approved, motivated an upgrade program both for the collider BEPCII (Beijing Electron Positron Collider), that hosts the experiment and for some of the sub-detectors, that compose the spectrometer. The current inner drift chamber is suffering of aging and the proposal is to replace it with a detector based on Cylindrical GEM technology.
The CGEM Inner Tracker (CGEM-IT) is made of three coaxial layers of triple GEM. The tracker is expected to restore the efficiency, and to improve the z determination and the secondary vertex position reconstruction, with a resolution of 130 μm in xy plane and 300 μm along the beam direction. For the reconstruction in magnetic field with Charge Centroid and uTPC methods, it is required an analog readout and an electronics contribution to the time resolution better than 5 ns. The full system consists of about 10,000 electronics channels. The overall readout chain needs to sustain a peak rate of 14 kHz/strip of signal hits for the strips of the CGEM-IT innermost layer. In order to ensure enough bandwidth and rate capability headroom to accommodate the signal and the noise, the rate has been multiplied by a factor of safety equal to four, requesting a capability of 60 kHz/channel.
The scheme of the full readout chain is shown in the attached file.
The TIGER (Torino Integrated GEM Electronics for Readout) chips are assembled in pairs on front-end boards and installed on the detector. Each mixed-signal chip can handle the complete readout of the data incoming from 64 channels.
Data and ASIC Low Voltage are fed through Data Low Voltage Patch Cards by the GEM Read Out Cards (GEMROC). The core of each GEMROC is a development kit based on an FPGA of the Intel/Altera ARRIA V GX family, connected to an interface card designed for the BESIII experiment.
The GEMROC boards receive signals from the BESIII timing and trigger interface, communicate with the BESIII slow control via Ethernet interface and via optical fibers with the GEM-Data Concentrator cards, which build the events and communicate with the VME-based BESIII DAQ. The GEMROC boards manage the front-end boards power supply and configuration as well as the TIGER output data collection.
To improve the quality of the fast control signals (FCS) and overcome the signal integrity issues, an upgrade of the FCS distribution system has been designed. It consists of a System FCS Fanout module interfaced directly to the BESIII FCS, driving by bidirectional optical links four Local FCS Fanout modules. These modules use transceiver daughter cards to drive the received electrical signals onto a multi-drop backplane with single-ended signaling.
The requirements met for the CGEM-IT project make the electronics also suitable for the readout of other innovative micro-pattern gaseous detectors. It is reported how the readout system has been designed keeping in mind strong adaptability and modularity and tested using a dedicated software interface developed in Python with control, monitoring, and logging functionalities.

ASIC / 29

FAST2: a new family of front-end ASICs to read out thin Ultra-Fast Silicon detectors achieving picosecond time resolution.

Authors: Alejandro David Martinez Rojas[1]; Marco Ferrero[2]; Nicolo Cartiglia[3]; Roberta Arcidiacono[2]; Elias Jonhatan Olave[2]; Federico Fausti[4]; Federico Siviero[1]; Marta Tornago[None]; Marco Mandurrino[5]; Luca Menzio[2]; Valentina Sola[2]

[1] *INFN - National Institute for Nuclear Physics*

[2] *Universita e INFN Torino (IT)*

[3] *INFN Torino (IT)*

[4] *Polytechnic University of Turin*

[5] *INFN*

Corresponding Authors: marco.ferrero@cern.ch, alejandrodavid.martinezrojas@to.infn.it

We present the first results obtained with the FAST2 family of ASICs. The FAST2 ASIC family, designed in the 110 nm CMOS technology, has been optimized for the read-out of Ultra-Fast Silicon Detectors, aiming to achieve a combined total time resolution of less than 40 ps. In the FAST2 family, the ASIC (FAST2_A) presents 16 channels and has only the amplification stage with a timing jitter lower than 16 ps experimentally, and power dissipation of 1 mW/ch.

Summary (500 words):

FAST2: a new family of front-end ASICs to read out thin Ultra-Fast Silicon detectors achieving picosecond time resolution.
In this contribution, we present the first results obtained with the FAST2 family of ASICs. The FAST2 ASIC family, designed in the 110 nm CMOS technology, has been optimized for the read-out of Ultra-Fast Silicon Detectors, aiming to achieve a combined total time resolution of less than 40 ps. The FAST2 family comprises 3 different ASICs: two of them (FAST2_EVO1, FAST2_EVO2) have 20 channels, and use the amplifier-comparator architecture, while the third ASIC (FAST2_A) has 16 channels and has only the amplification stage. In this contribution, we present the first results of the FAST2_A ASIC.
The FAST2 prototypes have been designed in 110 nm CMOS technology with a power consumption of about 1 mW/channel.
The experimental results presented here have been obtained by coupling the FAST2_A ASIC with a UFSD and using several techniques to evaluate the combined performances.
The setup includes a Large Scanning-TCT with a 1060 nm wavelength laser diode and a tunable laser width between 350 − 4000 ps. The laser intensity is tuned in such a way to generates the light needed to produce a MIP. Experimentally, several output signals are acquired to analyze the timing jitter and rising time over the input charge. The UFSD under test has a capacitance of 3.4 pF, and a generated charge range from 5 to 30 fC depending on the bias voltage operation range (120 to 240 V). At these operation conditions, the front-end architecture produces a time jitter lower than 30 ps for input charges higher than 8 fC, as shown in the experimental results. The ASIC prototype achieves a jitter lower than 15 ps with an input charge of a MIP equal to 17 fC. The Near-end and Far-end crosstalk caused due to the mutual capacitance and inductance among 16 electronics channels come out as a time derivative of the transmitter channels. The crosstalk components are attenuated more than 23 dB at 50 ☒ of load.
The experimental results discussed in the conference presentation will include results obtained with a beta telescope, where 2 MeV electrons from the Sr90 beta source are used to evaluate the performances. These results include the corrections due to time walk and the uncertainties introduced by the MIP non-uniform energy deposition, called Landau noise σlandau.

Radiation Tolerant Components and Systems / 30

The radiation-hard low-Voltage LDO for HGCAL in the CMS Phase-2 upgrade

Author: Aamir Irshad[1]

Co-author: Ludivine Ceard [2]

[1] *Universite Libre de Bruxelles (BE)*

[2] *National Taiwan University (TW)*

Corresponding Author: aamir.irshad@cern.ch

The CMS detector will see the replacement of its existing endcap calorimeter with a new high granularity calorimeter (HGCAL), which will need to withstand much higher radiation levels than the present endcaps. This poses tight constraints on the front-end electronics, including the powering

chain. As part of this chain, a low-dropout linear regulator (LDO) has been designed and prototyped for post-regulation for HGCAL, providing extremely low noise stable power to the analog front-end. We present results from tests of the LDO, including from a detailed irradiation campaign (TID, SEE, neutrons).

Summary (500 words):

The HGCAL calorimeter, which will replace the endcap calorimeters in the CMS detector, will undergo unprecedented luminosity and radiations levels due to collisions from the HL-LHC. A radiation-hard adjustable high current custom low-dropout regulator (LDO) has been designed for the post-regulation and powering of sensitive analog front-end devices for the HGCAL electronics system. The LDO offers an excellent transient response at a current of 3000 mA, maintaining a low dropout of under 200 mV. The functional characterization of the LDO showed full compliance with the strict design specifications. The LDO will be placed in all regions of HGCAL facing a dose of up to 200 Mrad and a fluence of up to 8 x 10^15 MeV neq cm^-2. A comprehensive irradiation study of the LDO took place to validate its design for mass production and radiation hardness for the duration of the HL-LHC operation. Three different radiation characterization tests were devised, including total ionizing dose (TID), a heavy-ion Single Event Effect (SEE), and a neutron beam exposure. The TID test, performed at CERN with X-Rays, is necessary to estimate the ageing effects on the performance of LDO after an accumulation of dose from 10 years of HL-LHC operation. The LDO was irradiated up to 1 Grad. The output adjustment functionality and internal monitoring indicators of the LDO also showed flawless function even after such a high TID exposure. A voltage drift smaller than 20 µV/Mrad was observed within 2% deviation over the entire TID range. An SEE test was conducted at the Cyclotron in Louvain-La-Neuve (Belgium) with various heavy-ion beams. To enhance the radiation robustness, no digital block is used in the LDO design except one latch in the test block. The SEE test allows the observation of transients at the output of the LDO caused by a single, energetic particle hit and temporary malfunction of status pins. This test also excludes the occurrence of possible latch-up and gate rupture in the device. A fast trigger-based test system is designed to detect and record eventual Single Event Transients (SET) due to the presence of sensitive nodes in the design. Lastly, to test the foreseen large neutron flux in the experiment, LDO samples were sent to the Jozef Stefan Institute (Slovenia), and exposed to 1.0 x 10^16 and 2.0 x 10^16 MeV neq cm-2 of neutron fluence. The post-irradiation analysis would reveal any displacement damage caused by neutrons in the internal atomic structure of the LDO.

Power, Grounding and Shielding / 31

Serial powering and signal integrity characterisation for the TEPX detector for the Phase-2 CMS Inner Tracker

Authors: Arne Christoph Reimers[1]; Anna Macchiolo[1]; Ben Kilminster[1]; Kyle James Read Cormier[1]; Stefanos Leontsinis[1]; Yuta Takahashi[1]

[1] *Universitaet Zuerich (CH)*

Corresponding Author: arne.reimers@cern.ch

The entire CMS silicon pixel detector will be replaced to operate at High Luminosity LHC. The novel scheme of serial powering will be deployed to power the pixel modules and new technologies will be used for a high bandwidth readout system. In this contribution the new TEPX detector will be presented, with particular focus on a novel concept to provide both power and data connectivity to the modules through a disk-shaped PCB. As TEPX also features the longest serial powering chains in IT, an emphasis on serial powering results will be shown, together with signal integrity and data transmission performance.

Summary (500 words):

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is expected to collide protons at a centre-of-mass energy of 14 TeV and to reach the unprecedented peak instantaneous luminosity of 5 x 10^34 cm^-2 s^-1 with an average number of pileup events of 140. This will allow the ATLAS and CMS experiments to collect integrated luminosities up to 4000 fb^-1 during the project lifetime. To cope with

this extreme scenario the CMS detector will be substantially upgraded before starting the HL-LHC, a plan known as CMS Phase-2 upgrade. The entire CMS silicon pixel detector (IT) will be replaced and the new detector will feature increased radiation hardness, higher granularity and capability to handle higher data rate and longer trigger latency.

The upgraded IT will be composed of a barrel part, TBPX, and small and large forward disks, TFPX and TEPX. The novel scheme of serial powering will be deployed to power the pixel modules and new technologies will be used for a high bandwidth readout system. The TEPX detector has four large disks on each side, extending the coverage up to |eta|<4.0. Furthermore, the services will be redesigned for the new system. In this contribution the new TEPX detector will be presented, with particular focus on a novel concept to provide both power and data connectivity to the modules through a disk PCB. As TEPX also features the longest serial powering chains in IT, an emphasis on serial powering results will be shown, together with signal integrity and data transmission performance. In TEPX the modules are arranged in five concentric rings. The chains corresponding to the first and third rings have been tested with 5 and 9 quad digital RD53A modules, respectively. Their performance in the disk, while being powered in series, has been compared with the one achievable in stand-alone mode, in terms of noise, threshold uniformity, signal integrity. No degradation of these parameters was observed for these serial power chains and it was possible to establish a simultaneous communication to all the modules. The study will continue with the implementation in the chains of quad modules with sensors, to study the HV distribution, and with the serial power operation of the longest chain in Ring 5, where 12 modules are located.

Programmable Logic, Design Tools and Methods / 32

Automated firmware generation and continuous testing for the CMS HGCAL trigger primitive generator

Authors: Jean-Baptiste Sauvan[1]; Thierry Romanteau[1]; Florence Danielle Beaujean[1]

[1] *Centre National de la Recherche Scientifique (FR)*

Corresponding Author: jean-baptiste.sauvan@cern.ch

A first version of the firmware blocks of the trigger primitive generator for the CMS endcap calorimeter upgrade (HGCAL) are being implemented, in order to assess the FPGA resource requirements and dimension the system. For the development of some of these blocks, a data-driven design flow is used to automate the production of multiple firmware variants based on VHDL and HLS C/C++ templates. In addition, the design steps are integrated into Continuous Integration tools to automatically test and validate every change, and as much as possible avoid repetitive human tasks and the associated errors.

Summary (500 words):

The Level 1 (L1) trigger primitive generator (TPG) of the future Phase-2 upgrade High Granularity Calorimeter (HGCAL) of CMS is composed of two off-detector processing stages. The first stage (Stage 1) mainly performs a synchronization, reorganization and truncation of the incoming data and time multiplexes its output data to the second stage. The latter then builds the actual trigger primitives and sends them to the central L1 trigger. One essential task of the Stage 1 firmware is to group trigger cell (TC) data coming from multiple detector modules into bins corresponding to projective regions of the detector. A sorting and potential truncation of these TC data are then applied in each individual bin. Stage 1 processing will run in six identical copies of 24 FPGAs each, with one copy for each 120 degree endcap sector. Each of these 24 FPGAs sees a different portion of the detector and the TC data routing and sorting is different in each of them. As an example, each FPGA contains 84 different sorting networks with numbers of inputs varying from 2 to more than 200 in different combinations for each FPGA. Having a single firmware design for all 24 FPGAs is not possible as it would require too many resources and excessive latency to handle all the different cases. It is therefore necessary to design the firmware individually for each of the 24 FPGAs. Doing this manually would be extremely difficult to develop and maintain. In addition, since the geometry of the HGCAL is still evolving and the connection map between frontend detector modules and backend FPGAs is not yet fixed, the content of each FPGA will need to be updated several times in the future. Therefore an automated design workflow is developed,

featuring automated firmware generation and continuous testing and integration. The key inputs to this workflow are code templates (VHDL and HLS C/C++) and configuration data, containing among other things information on the detector geometry and the frontend-backend connection map. A template engine, Jinja2, produces firmware source files from these inputs which can be automatically assembled into Vivado HLS and Vivado projects. The full workflow pipeline, composed of source code generation, high level synthesis, RTL synthesis, simulation, and place-and-route, is described as a Directed Acyclic Graph (DAG) and handled by a workflow manager. In addition the full process is integrated with Gitlab Continuous Integration tools such that every step can be tested and validated automatically for each update of the code templates and configuration data. The firmware blocks performing the TC data processing in the HGCAL TPG Stage 1, developed in C/C++ for some of them and in VHDL for others, will be presented as well as the methods and tools used to automatize the design process and to update firmware in a continuous fashion, as changes occur (for instance in the detector design).

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Fully-integrated set-up for gate current characterization in 28nm CMOS technology

Authors: Federico Fary[1]; Matteo Pezzoli[None]; Lodovico Ratti[2]; Andrea Baschirotto[3]

[1] *University of Milano-Bicocca*

[2] *University of Pavia*

[3] *Univ. Milan Bicocca*

Corresponding Author: f.fary@campus.unimib.it

This work introduces design and simulation validation, of a monolithic setup, based on a current amplifier, for accurate gate current measurement in NMOS devices integrated in 28nm technology. The Devices-Under-Test (DUTs) include transistors with gate width between 60µm and 300µm and length between 400nm and 1µm. Current in the DUT is amplified by a 100x factor, with an accuracy above 90%. The current amplifier achieves low noise operation for an accurate gate-current parallel noise estimation. The device will also be exploited to study radiation (up to 500Mrad-TID) damage effects on the noise current and on its associated parallel noise.

Summary (500 words):

The requirement for increased IC components density in read-out systems for High Energy Physics (HEP) experiments led, in the last decade, and will lead, in the future upgrades, to an extensive exploitation of deep-submicron technologies (65nm and below). These highly downscaled nodes suffer from a reduction in the gate oxide layer thickness (nowadays less than 2nm), which can be strictly correlated with an increased gate-channel direct tunneling phenomena. This situation translates in an increase in the MOSFET Gate Current (IGate), resulting in digital power consumption increase and analog device noise performance worsening. To Study the relationship between the gate current and the most important transistor design parameters, the impact of this current on analog performances, and the effect of radiation on the current value itself, has become of crucial importance.
Within the INFN project FinFet16v2, this work proposes a gate current amplifier in 28nm CMOS technology achieving a 40dB current amplification. This large amplification is a mandatory requirement for measuring such small currents, in the nA range, and distinguish it from the noise floor. To achieve the desired task, the circuit represented by the schematic of fig.1 has been developed. The DUT gate current is sensed by M21 and mirrored in M22 with a mirror factor of 9. M7 provides both transistors with their bias current, which will be mirrored in a 10-times wider M23 transistor, yielding an output current a factor of 100 larger than the original gate current.
More than 90% accuracy in the ratio between the output current and the gate current in the Device-Under-Test (DUT) is achieved thanks to proper design and layout precautions. Transistor M30 is designed to match M22 and M21 and provides M7 and M23 with the same bias conditions. The most important transistor couples (M23-M7 and M22/M21-M30) are laid out in an interdigitated fashion to maximize device matching and improve accuracy, in corner and Montecarlo simulations. A capacitive feedback path (C1) was implemented for stability purpose.

The same gate current amplifier can be operated with DUT featuring different gate size, with width between 60µm and 300µm and length between 400nm and 1µm, making it possible to characterize the gate current as a function of the transistor size. In this prototype setup overall 20 different DUTs are available. Moreover, since gate current also depends on the transistor bias point, the drain-source current in the DUT can be tuned, by properly trimming the Ibias_tuning between 100µA and 5mA. In simulation, the measurable gate current with these setup conditions ranges between 0.3nA and 157nA.
Last, thanks to the proper feedback loop and an accurate transistor sizing, the DUT gate current noise can be assumed as the dominant contribution in the overall current noise at the amplifier output. For this reason, the gate current amplifier can be exploited for accurate gate current noise measurement.

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The MDT Trigger Processor development for the ATLAS Level-0 Muon Trigger at HL-LHC

Authors: Kunihiro Nagano[1]; Guillermo Loustau De Linares[2]

Co-author: Davide Cieri [3]

[1] *High Energy Accelerator Research Organization (JP)*

[2] *University of Massachusetts (US)*

[3] *Max-Planck-Institut fur Physik (DE)*

Corresponding Authors: guillermo.jose.loustau.de.linares@cern.ch, kunihiro.nagano@cern.ch, davide.cieri@cern.ch

The novel MDT Trigger Processor (MDTTP) is a fundamental component of the ATLAS Level-0 Muon trigger upgrade, designed to meet High-Luminosity LHC requirements. The MDTTP will use MDT hits to improve the momentum resolution of muon candidates provided by RPC and TGC detectors and to reduce the fake rate.
A hardware demonstrator has been developed based on the Apollo ATCA platform.
The demonstrator includes two large FPGAs, high-speed FireFly optical transceivers, and other peripheral hardware. We present here demonstrator test results, plans for the prototype design, firmware implementation, including the core algorithm and control and monitoring.

Summary (500 words):

The first-level muon trigger (L0Muon) of the ATLAS experiment will be upgraded to operate in the substantially increased luminosity environment of the HL-LHC. The selectivity of the current system is limited by the moderate spatial resolution of RPC and TGC trigger chambers. The Monitored Drift Tube (MDT) chambers currently used for offline precision tracking will be included in the trigger to improve the transverse momentum resolution and the reduce the fake muon trigger rate.

The processing of MDT hits will be performed by the MDT trigger processor (MDTTP) ATCA blades, which will define regions of interest based on the candidates provided by the Sector Logic boards, formed using RPC or TGC data, and identify the MDT hits that are compatible in space and time. Those hits are then used to form track segments and combine them for the determination of the transverse momentum. The MDTTP will also be used to reject low quality sector logic candidates for which no MDT track segments could be found.
Simulation studies confirm that the MDTTP will reduce the L0Muon output trigger rate up to 70%, while keeping a high efficiency plateau of 95%, for a single muon trigger with a threshold of 20 GeV.

The MDTTP blade will be implemented using the generic open-source platform Apollo. An Apollo ATCA blade is comprised of two PCB modules. The generic “Service Module”, common to all Apollo applications, provides the required ATCA Intelligent Platform Management Controller (IPMC), power entry and conditioning, a powerful system-on-module (SoM) computer, and flexible clock and communications infrastructure. The application-specific “Command Module” provides the processing FPGAs and the FireFly Transceivers for communication with the other systems inside ATLAS.

In addition to the trigger processing tasks, the MDTTP will be also responsible for the configuration and monitoring of the MDT front-end boards, and to transmit MDT hit information to the FELIX system on receipt of a L0 acceptance signal.

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The ATLAS Electron Feature Extractor Module: Design, Manufacture and Test

Author: Kunihiro Nagano[1]

Co-author: Ian Brawn [2]

[1] *High Energy Accelerator Research Organization (JP)*

[2] *Science and Technology Facilities Council STFC (GB)*

Corresponding Authors: saeed.taghavirad@cern.ch, kunihiro.nagano@cern.ch

In Run 3, the ATLAS Level-1 Calorimeter Trigger (L1Calo) will be augmented by an Electron Feature Extractor (eFEX), which will identify isolated electron/photon and tau particles. Each eFEX module accommodates 424 signals at 11.2 Gb/s. Three generations of eFEX have been manufactured, and the design, manufacturing, and testing processes have been optimised. The firmware for the eFEX is managed using a custom system that has since been adopted by ATLAS TDAQ as the standard for the Phase-II upgrade. Presented here are the eFEX design, test results, and lessons learned from prototype and pre-production manufacturing.

Summary (500 words):

In Run 3, the ATLAS level-1 Calorimeter Trigger (L1Calo) will be augmented by new processing modules. Of these, the Electron Feature Extractor (eFEX), will identify isolated energy deposits in the calorimeter characteristic of electron/photon and tau particles, and achieve a higher discriminatory power than the previous trigger by running more complex algorithms on data of a higher granularity (ten E_T values for each tower of 0.1 × 0.1 in eta × phi).
The principle design challenges of the eFEX arise from the nature of the algorithms employed: overlapping windows of data are processed in parallel, requiring data to be shared between modules. An efficient implementation requires a small number of modules of high bandwidth. Furthermore, sharing data across the module complicates the PCB design: data can be brought to a single FPGA using optical receivers placed close to that device, but longer tracks are necessary to transmit data to multiple FPGAs. The resultant eFEX design is a 22-layer board with six micro-via layers. It houses 3942 tracks, including 424 pairs carrying signals of 11.2-Gb/s. The PCB material is Isola Itera. Four Processor FPGAs (Xilinx XC7VX550) implement the core of functionality. On the real-time trigger path, they synchronise the data across all inputs, run feature-extraction algorithms, sort the results across the four FPGAs and transmit them downstream, all within a latency of 13.4 ns. A fifth FPGA (XC7VX330T) implements the control and readout interfaces.
The firmware for the four Processor FPGAs is built in a single project using generic parameters and programmable registers to implement the different pinouts, mappings, and functions required. All of the firmware is managed using a custom, script-based, automated workflow, HDL On Git (HOG), which has since been adopted by ATLAS TDAQ as the standard firmware-management system for the Phase-II upgrade. It provides version management and Continuous Integration.
Prototype eFEX modules were built and tested successfully in 2016, but subsequently, the connectivity of the high-speed outputs was changed to take advantage of changes to the trigger system proposed for the Phase-II ATLAS Upgrade. The PCB stack-up was also changed to reduce the voltage drop across the module. A first pre-production run suffered PCB manufacturing problems (eventually resolved), and a second was conducted with a different manufacturer, which was then chosen for the full production run.
These experiences provided an opportunity to optimise the eFEX design flow further, to minimise the likelihood and impact of errors. The flow includes signal-integrity and power simulations, and time-domain reflectometry/transitometry tests. To facilitate the latter, specific tracks are included in the PCB design. These provide a better measure of layer impedances than coupons, due to variations in plating thickness over the panel.

Hardware tests of the eFEX show that the inputs have a bit error rate of less than 10^-15 , and the noise, power, and cooling measurements are within specification. The firmware functionality has been tested as part of a full slice of the ATLAS L1Calo trigger, and the system will be installed in the summer of 2021.

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QEMU-based hardware/software co-development for DAQ systems

Author: Wojciech Zabolotny[1]

[1] *Institute of Electronic Systems, Warsaw University of Technology*

Corresponding Author: wzab@ise.pw.edu.pl

Modern DAQ systems typically use the FPGA-based PCIe cards to concentrate and deliver the data to a computer used as an entry node of the data processing network.
This paper presents a QEMU-based methodology for the co-development of the FPGA-based hardware part, the Linux kernel driver, and the data receiving application. That approach enables quick verification of the FPGA firmware architecture, organization of control registers, the functionality of the driver, and the user-space application.
The developed design may be tested in different emulated architectures with a changeable type of CPU, IOMMU, size of memory, and the number of DAQ cards.

Summary (500 words):

The data acquisition chain for the BM@N experiment is planned to use the standard commercial PCIe board equipped with Virtex 7 FPGA.
Such a flexible solution allows developing a highly optimized FPGA-based data concentrator and DMA engine delivering the data to the computer working as an entry note of the data acquisition and processing network. However, the joint development of the FPGA firmware, the associated Linux kernel driver, and the user-space application responsible for data reception and processing is usually an iterative process with a long modification and testing cycle.
Modification and resynthesizing of the FPGA firmware requires significant effort and time. Bugs in the bus-mastering DMA engine or the kernel driver may result in system crashes or even in filesystem corruption.
Additionally, testing the driver and the whole system with multiple boards may be limited by hardware availability.
The QEMU emulator offers efficient emulation of the PCIe-capable computers and may be easily extended with the models of user-defined hardware written in C.
The developed methodology offers a possibility to simulate the data concentrator working either with the data generator included in the model or with the data delivered from external applications (e.g., the database of archived signals or the detector simulator) to the QEMU using the ZeroMQ protocol.
With that approach, multiple developers may work simultaneously developing the device model, driver, and application, testing them on their computers. The development may be started before the hardware is available and may even help in selecting the FPGA platform.
The organization of the delivered data in the host memory may be quickly tested and modified.
The proposed methodology was successfully used to develop a complete system consisting of the simple bus-mastering DMA engine, kernel driver, and data receiving application.
The system uses hugepages-backed buffers allocated by the target data-processing application, allowing zero-copy implementation of data delivery.
Due to the use of hugepages, no boot-time reservation of the memory or CMA-enabled kernel is required.
The emulated machine uses a standard Debian/testing Linux system. The boot time of the emulated system was below 20 seconds (on a host with Intel i7-4790 CPU), enabling very quick crash recovery.
Recompilation of each component - the QEMU model of the device, the driver, and the application consumed less than 1 minute, which enabled a quick development cycle.
The created DAQ system was successfully tested on a virtual machine with 16 GB of RAM (the host had 32 GB of RAM) with eight simulated DAQ boards. Each board used a 1 GB data buffer consisting of 512 hugepages with a size 2 MB each.

The data were delivered with ZeroMQ via a local TCP/IP socket from the local data-generating applications.
The results suggest that the proposed methodology may be a valuable tool in developing the new FPGA-based DAQ firmware.
The C-implemented model must be translated into the HDL implementation suitable for synthesis. Further research is needed to investigate if that process may be automatized using the HLS technology.

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Irradiation of VFAT3: A 128-channel charge-sensitive front-end chip for the CMS GEM phase-2 upgrade

Author: Aamir Irshad[1]

Co-authors: Paul Aspell [2]; Gilles De Lentdecker [1]

[1] *Universite Libre de Bruxelles (BE)*

[2] *CERN*

Corresponding Author: aamir.irshad@cern.ch

VFAT3 is the 128-channel charge-sensitive front-end chip explicitly designed for the CMS GEM phase-2 upgrades. LHC is undergoing major upgrades for HL-LHC where the particle rate is expected to increase up to 5 times. It is therefore necessary to monitor the evolution of the VFAT3 response due to aging in the radiation environment by total ionizing dose (TID) tests. The device operation could also be interrupted by a single high-energy particle. Thus, the estimation of the single event upset (SEU) cross-section is essential as well. We summarize irradiation test results that validate the suitability of VFAT3 for CMS GEM upgrades.

Summary (500 words):

The VFAT3 is a 128-channel charge readout ASIC specifically designed for CMS GEM detector charge readout. Two different radiation characterization campaigns were launched to qualify the chip for CMS operation: TID and SEU tests. TID tests have been conducted at the CERN micro-electronics X-ray facility, and VFAT3 was irradiated with a monochromatic beam of X-rays at 1.8 Mrad/hr for several hours of beam time. The chip response was measured for possible variation in its internal parameters. VFAT3 was exposed up to 70 Mrad of TID with a mono-energetic X-ray beam and showed excellent robustness to the radiation. No significant deterioration is observed in the core device functionality during the test. However, the I/O block of the chip showed sensitivity towards the TID. A frequent communication break was observed after 35 Mrad of TID. In CMS, the GEM detectors would receive a maximum of 1 Mrad of TID in the HL-LHC. The TID results show that neither aging nor communication performance degradation is expected to disturb VFAT3 operation in CMS GEMs. The SEU tests were performed at Louvain-La-Neuve heavy-ion facility (HIF). The ions of varying stopping powers were used to irradiate the VFAT3, and corresponding upsets in the device registers were recorded. The SEU cross-sections and extrapolations to the HL-LHC conditions are also established. The VFAT3 registers are triplicated and showed low statistics of bit-flips (saturation cross-section: 6.1 X10^-10 cm2/bit), a good indication of the robustness of the device against SEU effects. A communication breakdown issue is also experienced during the SEU test, like the TID test. A related cross-section is calculated for this process, and the observed frequency of synchronization break is found more significant than register SEU rates. The worst-case scenario was found for the most forward GEM station, ME0, which would receive the maximum particle flux (up to 378 kHz/cm^2). There, a synchronization loss is expected in the system, after every 2.3 hrs at HL-LHC. This frequency is well below CMS global reset request frequency for the muon stations. The results show that VFAT3 would perform well in all the three GEM stations for the whole ten years of GEM operation without any significant radiation damage.

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The Prototype Hardware Design and Test of Global Common Module for Global Trigger System of the ATLAS Phase II Upgrade

Authors: Kunihiro Nagano[1]; Shaochun Tang[2]

[1] *High Energy Accelerator Research Organization (JP)*

[2] *Brookhaven National Laboratory (US)*

Corresponding Authors: filiberto.bonini@cern.ch, kunihiro.nagano@cern.ch

The HL-LHC will start operations in 2027, to deliver more than ten times the integrated luminosity of the LHC Runs 1-3 combined. Meeting these requirements poses significant challenges to the hardware design of the Trigger and Data Acquisition system. Global Trigger is a new subsystem, which will perform offline-like algorithms on full-granularity calorimeter data. The hardware implementation of the Global Trigger consists of three primary components: Multiplexer Processor layer, Global Event Processing layer, and demultiplexing Global-to-CTP Interface, all of which have identical hardware. The single Global Common Module hardware is implemented across the Global Trigger system.

Summary (500 words):

The Global Trigger is a new subsystem, which will perform offline-like algorithms on full-granularity calorimeter data. The calorimeter detector subsystems, L0Calo Feature Extractor (FEXs), and Muon Central Trigger Processor Interface (MUCTPI) provide serial data for each bunch crossing to the Multiplexer Processor (MUX) layer. These data are then time-multiplexed and all the data for a given event are transported to a single Global Event Processor (GEP) node that executes the algorithms. The results are then sent to the Central Trigger Processor (CTP) through the CTP Interface. There are two main advantages of the time-multiplexed architecture. First, ordering the data transmission to scan across the detector allows two-dimensional algorithms to be implemented in one dimension, reducing resource usage by an order of magnitude. Second, the event processor is decoupled from the LHC bunch-crossing rate, allowing the use of asynchronous and high-level algorithms that are impossible in the Phase-I hardware trigger.

As shown in Fig. 1, the hardware implementation of the Global Trigger consists of three primary components: a MUX layer, a GEP layer, and a demultiplexing Global-to-CTP Interface (CTP Interface), all of which use the same hardware implementation - Global Common Module (GCM) to minimize the complexity of the firmware and simplify the system design and long-term maintenance.

The GCM design is an ATCA Front Board with two large FPGAs and one SoC FPGA. The number of processor nodes of each layer is based on the total front-end output channels, maximum input channels of each node, and the maximum resource available for processing of each node FPGA. Driven mainly by the outputs from the Calorimeter, 72 MUXes and 48 GEPs with up to 72 25 Gb/s inputs/outputs are required.

To meet both the resource requirements and number of 25 Gb/s transceivers, the Xilinx Vertex UltraScale+ FPGA VU13P is selected for the node processors, and a MPSoC FPGA ZU19EG is selected for control and monitoring function. The hardware design block diagram is shown in Fig. 2. Each node has 8 pairs of FireFly, which is 25Gb/s 12-channel optical module produced by Samtec.

The hardware was designed in 2020 and is being tested since December 2020. All the major hardware functionalities and critical technologies have been verified such as Zynq UltraScale+ FPGA OS interfaces, monitoring, processor FPGA 25.78125 Gb/s electrical links, 12.8 Gb/s optical links with 14Gb/s FireFly modules, power consumptions, and thermal performance. Fig. 3 and Fig. 4 show the performance test of optical links and electrical links of the processor FPGAs at 12.8 Gb/s and 25.78125 Gb/s respectively. More details will be reported in the meeting.

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Firmware Architecture of the back-end DAQ system for the CMS High Granularity Endcap Calorimeter detector.

Author: Stavros Mallios[1]

Co-authors: Paschalis Vichoudis [1]; Paul Dominic Dauncey [2]; André David [1]

[1] *CERN*

[2] *Imperial College Sci., Tech. & Med. (GB)*

Corresponding Author: stavros.mallios@cern.ch

During the High-Luminosity phase of the LHC, the CMS endcap calorimeter will be replaced by the High-Granularity Calorimeter (HGCAL). A first firmware for the back-end DAQ system of the CMS Phase-2 upgrade HGCAL was implemented in the Serenity ATCA hardware. The system is responsible not only for the readout of the detector but also for its slow control and timing. To facilitate system maintenance, the firmware is optimized to handle all the different Front-End electronics configurations and data rates using a single — highly configurable — design. The architecture and implementation of the back-end DAQ system will be presented here.

Summary (500 words):

The next phase of the Large Hadron Collider (LHC), known as High Luminosity LHC (HL-LHC), will commence its operation in 2027. During this phase the HL-LHC is foreseen to provide about ten times the LHC dataset, operating at an instantaneous luminosity around five times higher than presently available. In order to cope with the new challenging conditions, the CMS collaboration will replace the existing electromagnetic and hadronic endcap calorimeters with the new High Granularity Calorimeter (HGCAL). The new detector will feature unprecedented transverse and longitudinal segmentation for both electromagnetic (CE-E) and hadronic (CE-H) compartments and will have the ability to withstand the high radiation levels. The CE-E and a large fraction of CE-H will use silicon hexagonal shaped detector modules as active detector material, while the lower-radiation part of the CE-H will be instrumented with scintillator tiles. A new read-out ASIC (HGCROC) was designed to meet the high dynamic range, low noise and high-precision timing information requirements of the detector. A concentrator ASIC (ECOND) will collect data from multiple HGCROCs and transmit them to the backend, using the lpGBT ASIC, through high speed (10Gbps), low power, radiation-hard links. The back-end DAQ functionality will be implemented in the Serenity ATCA hardware hosting two FPGAs. Each FPGA will receive ECOND data through 60 lpGBT links, align and store them to buffers. The buffers provide a means to smooth out the data flow sufficiently, to ensure that all downstream parts of the event data chain are able to handle the worst-case data rates. In addition, a L1T throttle signal can be asserted to reduce the probability of buffers overflowing. Since each ECOND can occupy the bandwidth of up to 2 lpGBT links, while multiple ECONDs can fit in one lpGBT, the DAQ firmware was designed in 30 highly configurable parallel processing units. Each unit processes data from two lpGBTs, capable of handling all possible ECOND/lpGBT combinations. Furthermore, data from the 30 Event Buffers are collected and sent to the central DAQ through 12 Links (SLinks) running at 16 Gbps. For each SLink, an engine block gathers the data from the selected Event Buffers and builds the SLink event. Depending on the number of event buffers per SLink (multiplexing ratio), each event buffer can be accessed by more than one SLink through an interconnecting logic. The selection can be different for each board, taking into account different input rates. The configuration data for the on-detector electronics is stored in control buffers in the DAQ FPGA. A control block associated with each buffer propagates the configuration data to the front-end electronics through the lpGBT control link offering both point-to-point and broadcasting transmission. A number of controller instantiations will be selected to optimise the tradeoff between resource utilization and configuration time. Finally the backend DAQ system receives the clock from the DTH and forwards it through the lpGBT control links to the on-detector electronics where it is recovered for use in the front-end. It also passes on the relevant fast control commands.

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Hog: handling HDL repositories on git

Authors: Nico Giangiacomi[1]; Francesco Gonnella[2]; Davide Cieri[None]; Nicolo Vladi Biesuz[3]; Davide Cieri[4]

Co-authors: Andrew Peck [5]; Alessandra Camplani [6]

[1] *University of Toronto (CA)*

[2] *University of Birmingham (GB)*

[3] *Universita e INFN, Ferrara (IT)*

[4] *Max Planck Society (DE)*

[5] *Boston University (US)*

[6] *University of Copenhagen (DK)*

Corresponding Authors: davide.cieri@cern.ch, nico.giangiacomi@cern.ch

Handling HDL project development within large collaborations presents many challenges in terms of maintenance and versioning, due to the lack of standardized procedures. Hog (HDL on git) is a tcl-based open-source management tool, created to simplify HDL project development and management by exploiting git and Gitlab Continuous Integration (CI).

Hog is compatible with the major HDL IDEs from Xilinx and Intel-FPGA, and guarantees synthesis and placing reproducibility and binary file traceability, by linking each binary file to a specific git commit. Hog-CI validates any changes to the code, handles automatic versioning and can automatically simulate, synthesise and build the design.

Summary (500 words):

Hog: handling HDL repositories on git
Coordinating firmware development among many international collaborators is becoming a very widespread problem. Guaranteeing firmware synthesis with Place and Route reproducibility and assuring traceability of binary files is paramount.

Hog tackles these issues by exploiting advanced git features and integrating itself with
HDL IDEs: Xilinx Vivado, Xilinx ISE (planAhead) or Intel Quartus. The integration with these tools intends to reduce as much as possible useless overhead work for the developers.

Hog is a set of Tcl/Shell scripts plus a suitable methodology to handle HDL designs in a
Gitlab repository. Hog is included as a submodule in the HDL repository (a Hog directory is always present in Hog-handled repository) and allows developers to create the
Vivado/PlanAhead/Quartus project(s) locally and synthesise and implement it or start working on it.

The main features of Hog are:
• a simple and effective way to maintain HDL code on git;
• automatic tag creation for versioning;
• automatic Gitlab release creation (including timing reports, changelog, and binary
• files);
• yml files to run continuous integration in your Gitlab repository;
• multi-platform compatibility, working both with Windows and Linux;
• any change to the source code is detected, and binary biles are certified.

Other optional features are:
• the possibility of creating multiple projects sharing the same top level file
• the possibility to store the output binary files on CERN EOS
• compatibility and support for IPBus (https://ipbus.web.cern.ch/)
• automatic creation of Sigasi project (https://www.sigasi.com/)

Hog is designed to use just a small fraction of developers' time to set up a local machine and get them to work on the HDL design as soon as possible.

For synthesis and Place and Route (P&R) reproducibility, it's necessary to be in control
of:
• HDL source files
• Constraint files
• IDE settings (such as synthesis and implementation strategies)

For traceability, every time a binary firmware file is produced, it is required to:
• know exactly how the binary files were produced
• be always able to go back to that point in the repository

To do this, Hog automatically embeds the git commit SHA into the binary file together with a more understandable numeric version in the form of M(ajor).m(inor).p(atch). Moreover, it automatically renames the file, including the version and inserts the hexadecimal value of the SHA so that it can be retrieved (using a text editor) in case the file gets renamed.

Avoiding errors is impossible, but the goal of Hog is to leave as little room as possible.
Another important principle in Hog is to reduce to the minimum the time needed for an external developer to set it up and configure it. For this reason, Hog does not rely on any external tool or library apart from on those needed to synthesise, implement (Vivado/PlanAhead/Quartus) and simulate (Modelsim/Questasim) the design.

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Developments on Radiation-Hard Silicon Photonic Devices towards Integrated Transmitters for High Energy Physics

Author: Simone Cammarata[1]

Co-authors: Gabriele Ciarpi [1]; Guido Magazzu [2]; Fabrizio Di Pasquale [3]; Sergio Saponara [4]; Philippe Velha [5]; Fabrizio Palla [2]; Stefano Faralli [5]

[1] *Università di Pisa & INFN Pisa (IT)*

[2] *INFN Pisa (IT)*

[3] *Scuola Superiore Sant'Anna*

[4] *Università di Pisa*

[5] *Scuola Superiore Sant'Anna & INFN Pisa (IT)*

Corresponding Author: simone.cammarata@phd.unipi.it

Custom silicon photonics intensity modulators for data readout in particle detectors will be presented together with preliminary experimental results. A variety of devices has been designed to explore the technological requirements to achieve data rate up to 25 Gb/s while sustaining extremely high dose levels (1 Grad total ionizing dose). Packaging constraints have been carefully considered to allow hybrid integration between photonic components, radio-frequency boards and integrated electronics.

Summary (500 words):

Silicon photonics (SiPh) is progressively being evaluated as a potential technology to upgrade the optical transceivers deployed inside particle detectors. Compared to state-of-the-art readout systems based on directly modulated laser diodes, e.g., VTRx+ [1], SiPh solutions could enable higher data rates, possibilities of data aggregation (e.g., wavelength division multiplexing), lower power consumption and reduced material budget. Results from work recently carried out at CERN show a promising radiation hardness for SiPh devices which paves the way for unprecedented levels of integration with electronics and front-end modules [2].
According to those studies, we designed a silicon photonic integrated circuit (PIC) in Imec's iSiPP50G 220-nm silicon on insulator (SOI) platform. The PIC integrates a variety of optical modulators to further investigate their radiation tolerance and their interconnection with driving electronics. Those modulators would be the building blocks to create a full integrated system.
Targeting a challenging 1 Grad total ionizing dose (TID) tolerance, some custom shallow-etched Mach Zehnder modulators (MZMs) have been designed with different doping configurations to understand the trade-off between radiation hardness, optical losses, and modulation efficiency. Each MZM is equipped with traveling-wave (TW) electrodes to study the influence of the pn junction loading and the radiation effects on the microwave response of the device.
All the components are laid out to guarantee both chip probing as well as hybrid packaging with radiofrequency printed circuit boards (RF-PCB) and integrated driving electronics. The flexibility allowed by this design enables high speed characterizations both in laboratory as well as inside irradiation chambers.
Ultra-compact meandered MZMs have also been designed to provide power-efficient alternatives to conventional TW devices. A footprint reduction generally extends the electro-optic modulation bandwidth and exempts from the usage of a terminating impedance, reducing power consumption and limiting on-chip thermal dissipations.

In addition, some building blocks for SiGe electro-absorption modulators (EAMs) have also been included to test their suitability under irradiation. To the authors' knowledge this would be the first time that such modulators are tested for HEP purposes. Given the radiation tolerance demonstrated by CERN for germanium (Ge) integrated photodetectors [3], it is likely that also those SiGe devices would present similar performances and thus add more design choices for future SiPh-based transceivers to be operated in harsh radiation environments.
The PIC was submitted for production in June 2020 and it is expected to be delivered in July 2021. According to this schedule, we expect to have some preliminary measurement results by the start of TWEPP conference in 2021.

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ASIC / **45**

Implementation and testing of Design For Testability methodologies in 65 nm ASICs for HL-LHC.

Author: Gianmario Bergamin[1]

Co-authors: Alessandro Caratelli [2]; Davide Ceresa [1]; Kostas Kloukinas [1]; Simone Scarfi' [1]

[1] *CERN*

[2] *CERN, EPFL*

Corresponding Author: gianmario.bergamin@cern.ch

The development of the MPA and SSA ASICs is approaching the production phase with a volume of more than 1000 wafers. The importance of yield management in the construction of the Outer Tracker modules requires rigorous testing methods capable to identify all defective parts. This contribution presents customized Design for Testability methods to replace the currently used functional tests that show limited coverage and long testing time. Scan-chain design, memory and Logic Built-In-Self-Test have been adapted for radiation-hard ASICs and introduced on-chip for a novel testing approach. Design flow and implementation choices will be presented together with silicon results.

Summary (500 words):

CMS Outer Tracker Front-End ASICs, namely MPA and SSA, are required to work in a harsh environment for an extended time period (10 years, ~53 Mrad) without any maintenance. The impact of faulty chips is aggravated by their combined assembly into expensive modules and for this reason production testing represents a fundamental step. On the other hand, the increasing complexity and integration in VLSI technology have a significant impact on the cost and difficulty of this phase.
To face the challenge, over the past decades, the industry has developed new approaches and methods to ensure quality and feasibility, replacing functional tests which simply exercise the circuit behaviour according to functional stimuli. Manufacturing defects are grouped into models representing the digital behaviour of physical defects and automatic algorithms have been elaborated to detect faults. Due to the complexity of these procedures, additional circuitry is needed to guarantee controllability and observability of internal nodes: these additional developments, referred as Design For Testability solutions, must be integrated during development.
Different methods have been studied to test different parts of the FE ASICs hardware: Built-In Self-Tests for SRAMs and Latch-based memory blocks, Scan-Chain Design approach and BIST circuitry for the remaining combinational and sequential logic.
SRAM blocks features an integrated BIST which performs a MARCH C- algorithm on a 512x128 cells matrix and detects SRAM faults with 10n operations, n being the memory lines. Stimulating its dual

port behaviour at working speed (40 MHz), it allows to identify the SRAM failures in less than 7ms. A checkerboard test was implemented in hardware for Latch memories, allowing to discover in around 50 us stuck-at faults in the sequential elements with a 4n complexity. Control signals and results for both BISTs are fully manageable internally via I2C protocol and radiation tolerance is preserved with Triple Module Redundancy (TMR) strategy, making the additional hardware transparent during the normal operation of the chip.
Core digital logic can be instead successfully tested within the Scan-Chain Design approach, which allows to exploit the powerful ATPG algorithms. The structural modifications foreseen in the commercial flow for scan chain insertion present radiation tolerance issues for sensitive test signals and therefore are not directly applicable in our design. A flow compatible with TMR design and Single Event Effects resistant was developed and scan chains were inserted to test the peripheral processing logic of the chips. Additional Logic BISTs and compressed scan chains were integrated in the MPA to provide the ASIC with the capability of automatically testing its pixel matrix.
Studies have been carried out to reduce power overhead, eventually limited to few percent's and maintained within specification, and to assess the best trade-off between fault coverage, timing closure and routability constraints. Testing phase demonstrated the correct functionality of the structures and extensive SEU tests proved the radiation hardness of the ASICs.
This contribution will present a novel testing approach from design consideration to silicon testing results for a reliable and cost effectiveness testing procedure.

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Development of the probe station for the hybrid assemblies of the European XFEL camera AGIPD

Authors: Ulrich Trunk[1]; Alexander Klujev[2]; Torsten Laurus[3]; Heinz Graafsma[1]; Sergey Smoljanin[1]; Sergei Fridman[1]; Stephan Stern[1]; Julian Becker[1]

[1] *DESY*

[2] *Deutsches Elektronen-Synchrotron*

[3] *Deutsches Elektronen-Synchrotron DESY*

Corresponding Author: alexander.klyuev@desy.de

The European XFEL facility delivers bunches of high brilliance pulses with a unique time structure, which requires a specially designed photon detectors for taking and recording the high quality scientific data. The Adaptive Gain Integrating Pixel Detector (AGIPD) is a hybrid pixel X-ray detector developed to cope with crucial requirements like 4.5 MHz frame rate and a dynamic range of 10⁴ 12.5 keV-photons. An important part for the data quality is the hybrid front-end module and its yield. In order to improve it a special probe station was designed and commissioned, the challenges and results are to be reported.

Summary (500 words):

The experimental stations of the European XFEL offer a possibilities for conducting the cutting edge physical experiments using original properties of the source, which include a burst operation with the bunch trains containing 2700 pulses of >1012 photons of 12 keV each, separated by 220 ns. This cycle is repeated at the rate of 10 Hz. Those properties put a challenging requirements on the detectors for the experimental stations of the facility. The AGIPD detector was developed to fulfill the requirements of the SPB and MID instruments including the following key features: a high dynamic range - from single photon sensitivity up to 104 12 keV photons, a fast frame rate of 4.5 MHz and a memory for 352 usable images in burst operation. Also the radiation tolerance of several 10 kGy was taken into account.
The AGIPD is based on a hybrid technology, including a sensitive surface consisting of a semiconductor pixel sensor and 16 ASICs attached to it using bump bonding technique. This assembly (further hybrid) is glued and wire bonded to the Low Temperature Co-Fired Ceramic (LTCC) board and mechanically connected to the copper interposer. This multilayer unit called a front-end module (FEM) is an essential part of the detector for the quality of the data.
As any component this unit has its own yield based on different factors and it had a rate of ~52%, which is not enough for the successful production of FEMs, taking into account that a newer systems should

be designed as double modules reducing the yield even further.
In order to improve the FEM yield an extensive study on yield killers was done and it showed that there are 4 main sources of imperfections for the FEM production exist:
• the ASIC quality after the bump bonding
• sensor quality after the bump bonding
• bump bonding process itself
• unacceptable sensor dark current, which originates from the poor thermal contact between the hybrid and the cooled copper interposer.
In order to reduce the first three mentioned above factors a special probe station for the hybrids was developed. The station includes a custom designed cantilever probe card for probing of 480 ASIC read-out pads and also providing the high voltage to the sensor with 4 pins. The probe card is attached to the specifically manufactured probe holder and to the read-out board. For the probing the DUT is pushed up to the probe card, powered and then being read out.
The special testing methodology of probing was developed and implemented resulting in eliminating the factors regarding the quality of both ASICs and bump bonding process. The sensors are tested by the hybrid manufacturers and then are being tested once more during the probing. All mentioned error sources are thus screened and any bad hybrid is to be rejected or reworked. The poor thermal conductivity is to be improved by use of the flattest LTCCs and better thermal filling with an expectation of yield improvement up to ~80%.

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CMS Phase-2 data acquisition, clock distribution, and timing: prototyping result and perspectives

Author: Jeroen Hegeman[1]

Co-author: CMS central DAQ group

[1] *CERN*

Corresponding Author: jeroen.hegeman@cern.ch

The CMS detector will undergo a major upgrade for Phase-2 of the LHC program: the HiLumi LHC. The Phase-2 CMS back-end electronics will be based on the ATCA standard, with node boards receiving the detector data from the front-ends via custom,
radiation-tolerant, optical links. An ATCA hub board, the DAQ and Timing Hub, will provide the interface between the back-end nodes and the central Trigger, Timing, and DAQ systems. This paper presents the progress on the development towards the DTH design. Measurements are presented showing the performance achieved for all main DTH tasks: clock distribution, DAQ throughput, and hub-to-node networking.

Summary (500 words):

The upgraded CMS detector will be read out at an unprecedented data rate of up to 60 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size reaching 10 MB. The back-end electronics will be based on the ATCA standard, with
node boards receiving the detector data via optical links from the front-end electronics and processing them.

Back-end electronics will be connected to the central Trigger, Timing, and DAQ systems, as well as the CMS control network, by a duo of custom boards: the DAQ and Timing Hub (DTH), and an additional DAQ800 node board. The DTH will connect to all back-end boards and be responsible for the distribution of clock, trigger, and fast-control commands from the central trigger control system to all back-end electronics, and the handling of throttling signals in the opposite
direction. The DAQ interface for the event data uses point-to-point optical links connecting back-end boards to the DTH using a custom lossless 'SLinkRocket' protocol. The event data are aggregated in the DTH and transmitted via standard 4x100 Gb/s Ethernet links to event
building computer nodes at the surface. Where detector needs exceed 400 Gb/s in a single ATCA crate, additional DAQ800 boards can be used to augment the DAQ throughput.

The introduction of timing detectors for Phase-2 CMS, aiming for a 30 ps precision on individual detector hits, strongly tightens the requirements on the clock and timing information distributed throughout the experiment, with different sub-detectors introducing different requirements.

The R\&D process towards the DTH design spans three prototyping branches: one for the clock distribution, one for the event building and DAQ throughput, and one for the managed Ethernet switch connecting the back-end boards to the control network. At past TWEPP events we have presented the design of the first DTH prototype, and discussed some of the design challenges encountered. The current paper summarises the progress made in the three prototype branches, and how these branches now converge into the final prototype: the DTH-P2. Performance measurements are presented of all three main DTH tasks, showing that most of the CMS Phase-2 can be met already with these prototypes. The quality and stability of the distributed clock will be quantified, the DAQ throughput and buffering performance will be presented, and the back-end Ethernet connectivity demonstrated.

We will conclude with a brief look forward to the qualification of the final DTH and DAQ800 designs.

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SMX and front-end board tester for CBM readout chain

Authors: Wojciech Zabolotny[1]; David Emschermann[2]; Marek Gumiński[1]; Michał Kruszewski[1]; Jörg Lehnert[2]; Piotr Miedzik[1]; Krzysztof Poźniak[1]; Ryszard Romaniuk[1]; Christian Joachim Schmidt[2]

[1] *Institute of Electronic Systems, Warsaw University of Technology*

[2] *GSI-Helmholtzzentrum für Schwerionenforschung GmbH*

Corresponding Author: wzab@ise.pw.edu.pl

The SMX chip is a front-end ASIC dedicated for the readout of STS and MUCH detectors in the CBM experiment.
The production of the ASIC and the front-end boards based on it is just being started and requires thorough testing to assure the quality.
The paper describes the SMX tester based on a standard commercial Artix-7 FPGA module with an additional simple baseboard.
In the standalone configuration the tester is controlled via IPbus and enables full functional testing of connected SMX, FEB, or a full detector module.
The software written in Python may easily be integrated with higher-level testing software.

Summary (500 words):

The production of components for the readout chain of the CBM experiment is ongoing.
The readout of the STS and MUCH detectors in CBM uses the dedicated STS-MUCH-XYTER 2.2 (in short, SMX) developed by AGH Krakow.
The SMX ASICs are mounted on front-end boards (FEBs) in various configurations depending on detector system and expected hit rates.
Readout is done with GBTx-based CROB boards further connected to CRI data concentration backend.
Testing of produced ASICs, assembled FEBs and full modules is the essential quality verification step in the production process.
The GBTxEMU board has been proposed as a common platform for all testing setups with two benefits: It provides broad availability of tester hardware for production in various sites and additionally allows full system tests in collaborating institutions worldwide independently of the GBTx-based readout.
It can be used either as an emulator of the GBTx data readout board alone or as full standalone backend system for FEB control. The GBTxEMU board is based on a standard commercial Artix-7 board (TE-0712, Trenz Electronics GmbH).
The board is supplemented with a dedicated motherboard providing necessary connectors and communication interfaces and a jitter cleaning device (SiLabs Si5344). It allows for clock recovery and system-wide synchronization if used in GBTx emulating mode.
The tester IP cores have been developed for this Artix-7 platform, based on the GBTxEMU board, and the developments done for the new CRI-based readout in CBM.

The tester supports communication with the SMX ASICs on various FEBs, employing various numbers of connected ASICs and readout E-Links, interfaced with different VITA 57.1 FMC adapters.
It emulates E-Links with phase adjustable clocks otherwise provided by the GBTx ASICs with a clock frequency set to 40, 80, or 160 MHz. The clock phase may be adjusted with a resolution offered by the MMCM blocks (1/1600 MHz/8 = 78 ps, slightly worse than 48.8 ps offered by GBTx). The input data delay may be adjusted with the IDELAYE2 blocks offering the resolution of 78 ps with a 200 MHz reference clock.
The tester is controlled via the IPbus interface over 1 Gb/s Ethernet. With the accompanying software written in Python the tester supports full testing of the E-Link communication. It also provides access to all internal registers of the SMX chips, enabling complete functional tests.
The received ASIC hit data may be stored in an internal FIFO accessible via IPbus, enabling the direct collection of a limited amount of hit data at a high hit rate. For longer tests at a limited hit rate, a possibility to transmit the hit data from selected channels in UDP packets has been implemented.
The tester is hardware-compatible with the GBTxEMU firmware. That allows the sites equipped with the prototype versions of the CBM readout chain to connect the tester via an emulated GBT optical link and perform long-time tests at a high rate. The Python-based software may be easily modified and adapted to the user's particular needs, including interfacing with the higher-level operation and quality verification software.

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Upgrade of the RPC detectors' data collection and transmission electronics for the ATLAS experiment at High Luminosity LHC

Author: ATLAS Muon Collaaboration[None]

Corresponding Authors: shikma.bressler@cern.ch, ioannis.mesolongitis@cern.ch

RPC detectors are used to trigger muons in the ATLAS Muon Spectrometer barrel region. The foreseen HL-LHC operation imposes replacing their trigger and readout electronics with a data collector and transmitter (DCT) system, which implements the LPGBT optical link to handle data bandwidth up to 10.24Gb/s. A testing system will be implemented to assess all DCT prototypes and mass production. Since the first DCT prototype is under irradiation tests, a methodology has been developed that renders feasible indispensable implementations towards the complete validation of the functionalities of the DCT and of any board that implements the LPGBT.

Summary (500 words):

The HL-LHC accelerator will have an instantaneous luminosity 5-7 times above its reference value resulting in higher data rates and radiation levels that will pose significant challenges to both the experiment's detectors and the readout and trigger electronic systems.
To preserve the acceptance of critical signatures for physics, the trigger system of the ATLAS experiment has to maintain both low-momentum trigger thresholds and manageable trigger rates. Hence, it will undergo a decisive upgrade (Phase II upgrade) by increasing the trigger rate and latency to 1MHz and 10μs, respectively, so that more complex trigger algorithms than in the present system can be feasible[1]. That trigger scheme renders the current readout and trigger electronics, which accommodate a maximum rate of 100 kHz with a maximum latency of up to 3 μs, incompatible.
This paper refers to the Phase II upgrade of the trigger system (based on RPC technology) in the central region (barrel) of the ATLAS Muon Spectrometer, a detector that will play a vital role in the full exploitation of the HL-LHC physics potential. It will focus on the high-radiation resistant Data Collector and Transmitter (DCT) boards that will replace the on-detector readout and trigger electronics of the RPC detectors.
The design architecture of a DCT prototype currently being under irradiation tests is presented (Figure 1). It is based on a Xilinx Artix FPGA able to digitize 288 input signals and the radiation-tolerant LPGBT)ASIC [3]; a multipurpose high-speed transceiver developed for high energy physics experiments. LPGBT handles the transmission of timing, trigger data, monitoring, control, and data readout between the RPCs' Front Ends (FE) and the off-detectors barrel Sector Logic boards (SL) that implement the trigger and readout logic (Figure 2). With the implementation of the LpGBT, the data bandwidth that the DCTs can handle is up to 10.24 Gb/s.

Due to the importance of the DCT system, the complexity of the signals it handles, and the large number of boards required (1570 DCTs), an automated test station will be developed to evaluate the performance of all its functionalities.
Presented are the architecture and measurement results of a test bench developed to evaluate the DCT's optical link LpGBT by implementing its backend counterpart (lpGBT-FPGA core) [4] on a VC709 development board. Since the DCT prototype is under fabrication, and loopback tests of the lpGBT-FPGA are not possible (due to asymmetry of its downlink and uplink connections), the tests were performed by modifying the alternative of the LPGBT ASIC (lpGBT-Emulator), and by implementing it in a second VC709 board (Figure 3). Data integrity has been verified by transmitting fixed patterns from the modified lpGBT-Emulator to the lpGBT-FPGA core and vice versa at 10.24 Gb/s and 2.56 Gb/s, respectively (Figures 4,5).
Even though the DCT prototype is not yet delivered, the successful operation of the above testing setup renders feasible indispensable implementations towards the complete validation of the functionalities of the DCT (or of any board that implements the LPGBT).

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ATLAS LAr Calorimeter Commissioning for LHC Run-3

Authors: Narei Lorenzo Martinez[1]; Florent Bernon[2]

[1] *Centre National de la Recherche Scientifique (FR)*

[2] *Aix Marseille Universite (FR)*

Corresponding Authors: florent.bernon@cern.ch, narei.lorenzo.martinez@cern.ch

Liquid argon (LAr) sampling calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region |η| < 3.2, and for hadronic and forward calorimetry in the region from |η| = 1.5 to |η| = 4.9. Phase-I detector upgrades began after the end of ATLAS Run-2. New trigger readout electronics of the LAr Calorimeter have been developed. Installation began at the start of the LHC shut down in 2019 and is expected to be completed in 2021.This contribution will give an overview of the new trigger readout commissioning, as well as the preparations for Run-3 detector

Summary (500 words):

The Liquid Argon Calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region |η| < 3.2, and for hadronic and forward calorimetry in the region from |η| = 1.5 to |η| = 4.9. It also provides inputs to the first level of the ATLAS trigger. After successful period of data taking during the LHC Run-2 between 2015 and 2018 the ATLAS detector entered into the a long period of shutdown. In 2022 the LHC should restart and the Run-3 period should see an increase of luminosity and pile-up up to 80 interaction per bunch crossing.

To cope with this harsher conditions, a new trigger readout path have been installed on the during the long shutdown. This new path should improve significantly the triggering performances on electromagnetic objects. This will be achieved by increasing by a factor of ten, the number of available units of readout at the trigger level.

The installation of this new trigger readout chain required the update of the legacy system to cope with the new components. It is more than 1500 boards of the precision readout that have been extracted from the ATLAS pit, refurbished and re-installed. The legacy analogic trigger readout that will remain during the LHC Run-3 as a backup of the new digital trigger system has also been updated.

For the new system it is 124 new on-detector boards that have been added. Those boards are able to digitize the calorimeter signal for every collisions i.e. at 40MHz and in radiative environment. The digital signal is then processed online to provide the measured energy value for each unit of readout an for each bunch crossing. In total this is up to 31Tbps that are analyzed by the processing system and more than 62Tbps that are generated for downstream reconstruction. To minimize the triggering latency the processing system had to be installed underground. There the limited space available imposed the

needs of a very compact hardware structure. To achieve a good enough compacity larges FPGAs with high throughput have been mounted on ATCA mezzanines cards. In total no more than 3 ATCA shelves are used to process the signal of approximately 40k channels.

Given that modern technologies have been used compared to the previous system, all the monitoring and control infrastructure had to be adapted and commissioned as well.

This contribution should present the challenges of such installation, what have been achieved so far and what are the milestones still to be done toward the full operation of both the legacy and the new readout paths for the LHC Run-3.

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Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Authors: Narei Lorenzo Martinez[1]; Fabrice Gensolen[2]

[1] *Centre National de la Recherche Scientifique (FR)*

[2] *Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France*

Corresponding Authors: gensolen@cppm.in2p3.fr, narei.lorenzo.martinez@cern.ch

To meet new TDAQ buffering requirements and withstand the high expected radiation doses at the high-luminosity LHC, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded. Developments of low-power preamplifiers and shapers and of a low-power 40 MHz 14-bit ADCs are ongoing. The signals will be sent at 40 MHz to the off-detector electronics, where FPGAs connected through high-speed links will perform energy and time reconstruction. The data-processing, control and timing functions will be realized by dedicated boards. Results of tests of front-end component prototypes will be presented, along with design studies on the off-detector readout system.

Summary (500 words):

A new era of hadron collisions will start around 2027 with the High-Luminosity LHC, that will allow to collect ten times more data that what has been collected since 10 years at LHC. This is at the price of higher instantaneous luminosity and higher number of collisions per bunch crossing.
In order to withstand the high expected radiation doses, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded.
The electronic readout chain is made of 4 main parts.
New front-end board will allow to amplify, shape and digitise on two gains the ionisation calorimeter signal over a dynamic range of 16 bits and 11 bit precision. Low noise below Minimum Ionising Particle (MIP), i.e below 120 nA for 45 ns peaking time, and maximum non-linearity of two per mil are required. Custom low noise preamplifier and shaper are being developed to meet these requirements using 65 nm and 130 nm CMOS technologies. They should be stable under irradiation until 1.4kGy (TID) and 4.1x10^13 new/cm^2 (NIEL). Two concurrents preamp-shaper ASICs have been developed and the best one in term of noise has been chosen. The test results of the new version of this ASIC will be presented. A new ADC chip prototype has been also submitted in June. Integration tests of the different components (including lpGBT links developed by CERN) on a 32-channels front-end board are ongoing, and results of this integration will be also shown.
The new calibration board will allow the precise calibration of all 128000 channels of the calorimeter over a 16 bits dynamic range. A non-linearity of one per mil and non-uniformity between channels of 0.25% with a pulse rise time smaller than 1ns should be achieved. In addition, the custom calibration ASICs should be stable under irradiation with same levels as preamp-shaper and ADC chips. HV SOI CMOS XFAB 180nm technology is used for the pulser ASIC, while TSMC 130 nm technology is now used for the DAC part. During second prototype testing, it was found that the DAC part of the calibration system, inserted previously with the pulser in XFAB 180nm technology, was not rad-hard, already after 0.5 kGy. This is why a third version has been designed overcoming this issue, and all results will be presented.
The data are sent off-detector at 40 MHz where FPGAs connected through high-speed links will perform energy and time reconstruction through the application of corrections and digital filtering. The

off-detector electronics receive 345 Tbps from front-end readout, which require 33000 links at 10 Gbps. For the first time, online machine learning technics are used in the FPGAs in order to better filter the data. The first test results of the signal processing board will be shown.
Reduced data are then sent with low latency to the first level trigger, while the full data are buffered until the reception of trigger accept signals. The data-processing, control and timing functions are realized by dedicated boards connected through ATCA crates. Design status of this timing boards will be shown too.

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Machine Learning for Real-Time Processing of ATLAS Liquid Argon Calorimeter Signals with FPGAs

Author: Nemer Chiedde[1]

[1] *Centre National de la Recherche Scientifique (FR)*

Corresponding Author: nemer.chiedde@cern.ch

Within the Phase-II upgrade of the LHC, the readout electronics of the ATLAS LAr Calorimeters is prepared for high luminosity operation expecting a pile-up of up to 200 simultaneous pp interactions. Real-time processing of digitized pulses sampled at 40 MHz is thus performed using FPGAs.
To cope with the signal pile-up, new machine learning approaches are explored that outperform the optimal signal filter currently used, both in assignment of the reconstructed energy to the correct bunch crossing and in energy resolution.
Latest performance results and experience with prototype implementations will be reported.

Summary (500 words):

The Phase-II upgrade of the LHC will increase its instantaneous luminosity by a factor of 7 leading to the High Luminosity LHC (HL-LHC). At the HL-LHC, the number of proton-proton collisions in one bunch crossing (called pileup) increases significantly, putting more stringent requirements on the LHC detectors electronics and real-time data processing capabilities.

The ATLAS Liquid Argon (LAr) calorimeter measures the energy of particles produced in LHC collisions. This calorimeter has also trigger capabilities to identify interesting events. In order to enhance the ATLAS detector physics discovery potential, in the blurred environment created by the pileup, an excellent resolution of the deposited energy and an accurate detection of the deposited time is crucial.

The computation of the deposited energy is performed in real-time using dedicated data acquisition electronic boards based on FPGAs. FPGAs are chosen for their capacity to treat large amount of data with very low latency. The computation of the deposited energy is currently done using optimal filtering algorithms that assume a nominal pulse shape of the electronic signal. These filter algorithms are adapted to the ideal situation with very limited pileup and no timing overlap of the electronic pulses in the detector. However, with the increased luminosity and pileup, the performance of the filter algorithms decreases significantly and no further extension nor tuning of these algorithms could recover the lost performance.

The back-end electronic boards for the Phase-II upgrade of the LAr calorimeter will use the next high-end generation of INTEL FPGAs with increased processing power and memory. This is a unique opportunity to develop the necessary tools, enabling the use of more complex algorithms on these boards. We developed several neural networks (NNs) with significant performance improvements with respect to the optimal filtering algorithms. The main challenge is to efficiently implement these NNs into the dedicated data acquisition electronics. Special effort was dedicated to minimising the needed computational power while optimising the NNs architectures.

Five NN algorithms based on CNN, RNN, and LSTM architectures will be presented. The improvement of the energy resolution and the accuracy on the deposited time compared to the legacy filter algorithms, especially for overlapping pulses, will be discussed. The implementation of these networks in firmware

will be shown. Two implementation categories in VHDL and Quartus HLS code are considered. The implementation results on Stratix 10 INTEL FPGAs, including the resource usage, the latency, and operation frequency will be reported. Approximations for the firmware implementations, including the use of fixed-point precision arithmetic and lookup tables for activation functions, will be discussed. Implementations including time multiplexing to reduce resource usage will be presented. We will show that two of these NNs implementations are viable solutions that fit the stringent data processing requirements on the latency (O(100ns)) and bandwidth (O(1Tb/s) per FPGA) needed for the ATLAS detector operation.

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Successive Approximation Register ADC Single Event Effects Protection and Evaluation

Authors: Bruno Sanches[1]; Marco Bregant[2]; Wilhelmus van Noije[1]

[1] *EPUSP*

[2] *IFUSP*

Corresponding Author: bruno.csanches@usp.br

This work analyses seven different alternatives to implement an ADC based on the successive approximation register (SAR) architecture. The influence of the encoding is taken into account while evaluating the importance of its reset approach. Different protection strategies against single event upsets are addressed, including the comparison of per module and per cell triplication. All versions of the SAR were designed and prototyped in the TSMC 130 nm technology. The ASIC was packaged in an open window QFN64 and irradiated in the IFUSP Pelletron particle accelerator, which revealed the impact of the encoding and reset choices in the block cross-section.

Summary (500 words):

ADCs are critical parts of numerous acquisition systems in HEP experiments. There are several possible architectures to implement an ADC and a popular one is the successive approximation register (SAR).

The SAR ADC is a mixed-signal block and may be implemented using a comparator, a DAC and a control module. The last is a digital block named SAR register which is responsible to run the successive approximation algorithm, triggering the sampling, controlling the DAC switches and reading the comparator responses. Moreover, it is responsible to register the calculated conversion and send it to further digital processing steps.

This digital block can suffer from single-event effects (SEE) generated by interactions with radiation, causing inappropriate control of the other blocks and creating incorrect conversions. Another possibility is the occurrence of single-event upsets (SEU) in a completed conversion value. These events can corrupt experiment data and should be investigated and mitigated.

To accomplish that, seven implementations of a 10 bit SAR were designed using different approaches in its digital control, but still focusing on not changing its analog side, triplicating it, or doing extra conversions.

Table 1 shows the implemented alternatives where two encoding options were done, binary and one-hot, also two reset options were tested synchronous and asynchronous. In relation to resistance to SEE three versions were done, one unprotected, one with per register TMR (Triple Modular Redundancy) and one with three complete blocks with voting between them (identified as Modular TMR). Three reference versions were also inserted and identified as ADC0, ADC1 and ADC0 with parity at the output.

The blocks were fabricated in TSMC 130nm process and packaged in an open-window QFN64 which was soldered to a minimal board just with supply components and tested using a Sockit FPGA which was placed outside of the beam chamber. Figure 1 illustrates the board together with the chip microphotography and Figure 2 shows the test scenario.

The ASIC was irradiated using the Pelletron particle accelerator at the São Paulo University. Three different beam types were used, starting with 5 MeV alpha particles and going to 44 MeV ^{16}O and finally 57 MeV ^{28}Si. Due to the low event count, the alpha particle test was discarded.

Table 2 provides the compiled cross-section results. Comparing the reference with sar_reg_03, a 70 times bigger cross-section is found, where the major difference is the asynchronous reset, showing that it increases the sensitivity and may be avoided.

In relation to the coding, a worse performance (greater than 140%) happened when using the one-hot in the state machines.

No considerable difference was found when changing the redundancy to the bigger modular strategy and both TMR alternatives have been successful.

Finally, is possible to state that there are positive results in relation to the evaluation of the inserted protections since, for all cases with some level of redundancy, no errors were registered. And this scenario was repeated for all the bundles and all the flows illustrating a great improvement in relation to the reference in this aspect.

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A flexible and low-cost open-source IPMC mezzanine for ATCA boards based on OpenIPMC

Authors: Luigi Calligaris[1]; Luis Ardila[2]; Andre Muller Cascadan[1]; Mark Pesaresi[3]; Mark Pesaresi[4]; Giacomo Fedi[3]; Andrew Peck[5]; Daniel Edward Gastler[5]

[1] *UNESP - Universidade Estadual Paulista (BR)*

[2] *KIT-IPE*

[3] *Imperial College (GB)*

[4] *Imperial College*

[5] *Boston University (US)*

Corresponding Authors: giacomo.fedi@cern.ch, dan.gastler@cern.ch, andrew.peck@cern.ch, luigi.calligaris@cern.ch

We present the development of an Intelligent Platform Management Controller mezzanine in a Mini DIMM form factor for use in electronic boards compliant to the Advanced Telecommunication Computing Architecture standard. The module is based on an STMicroelectronics STM32H745 microcontroller running the OpenIPMC open-source software, and its design has been published under open-source hardware license. The mezzanine has been successfully tested on a variety of ATCA boards being proposed for the upgrade of the experiments at the HL-LHC.

Summary (500 words):

Many experiments at the CERN LHC are adopting the PICMG Advanced Telecommunication Computing Architecture (ATCA) as a standard for the design of the electronic boards used in their detector backends. The standard requires that each board hosts a controller device, known as Intelligent Platform Management Controller (IPMC), tasked with a number of responsibilities such as managing the power state of the components of the board, measuring the health parameters of the latter and coordinating these operations together with the Shelf Management Controller. Since there are countless possibilities for the design of an ATCA electronic board, the IPMC needs to be configured specifically for the board it is meant to be used in. Therefore, an universal IPMC solution needs to be highly flexible and configurable in order to support these many different hardware configurations.

Following the success in developing OpenIPMC - an open-source microcontroller software based on FreeRTOS and implementing the IPMC features required by the PICMG standard - we developed a flexible hardware platform to serve as a host for OpenIPMC. This platform has been given the name OpenIPMC-HW.

This platform takes the form of a mini-DIMM mezzanine, pin-to-pin compatible with existing IPMC mezzanine solutions used in HEP. Similarly to the OpenIPMC software, the mezzanine design is released under an open-source license, making it very attractive for academic use in long-running experiments. At the core of the mezzanine operation lies a powerful STM32H745 microcontroller running OpenIPMC inside a FreeRTOS instance. The mezzanine has been tested and validated on a variety of ATCA electronic boards proposed for use in HEP experiments at the LHC.

ASIC / 59

Test results of RD53B chips for ATLAS and CMS phase-2 pixel upgrades

Author: Dominik Koukola[1]

[1] *CERN*

Corresponding Author: dominik.koukola@cern.ch

Following the RD53A demonstrator, the ItkPix (ATLAS) and CROC (CMS) pixel readout chips are being developed within the RD53 collaboration for the HL-LHC pixel detector upgrades of the two experiments. The two chips are based on a common design, called RD53B, in 65nm CMOS technology and are optimized for very high rate (3GHz/cm2) and radiation levels (>500Mrad). The ATLAS pre-production chip ItkPixV1 was submitted in March 2020 and the CMS pre-production chip CROCv1 is being submitted in May 2021.
This contribution gives a general overview of the chip architecture and discusses the characterization and testing of the pre-production chips.

Summary (500 words):

The RD53 collaboration is a joint effort between ATLAS and CMS to develop pixel readout chips for the HL-LHC pixel detectors of the two experiments. The harsh environment in the innermost layers of the detectors is setting stringent requirements on the pixel chip design. The readout has to be capable to cope with very high hit rates of 3 GHz/cm2 and trigger rates of 1 MHz in combination with a trigger latency of 12.5 us. A very high radiation tolerance of over 500 Mrad and 2x10^16 neq/cm2 is required as well as the support for a serial powering scheme.

A half-size demonstrator chip, called RD53A, was submitted in 2017 and has been tested exhaustively to qualify the different IP blocks and the general architecture for the development of the final pixel chips. It has also been used extensively for sensor characterization as well as for system studies giving viable input to the module designs and system architecture of both experiments.

The next generation RD53 chips, called RD53B, are designed as full sized pre-production chips and incorporate all production requirements defined by the experiments. There are two experiment specific versions of RD53B: the ATLAS version, called ItkPixV1 and the CMS version, called CROCv1. The two chips are two separate instances of the common RD53B design framework. The main difference between them is the pixel matrix size (400x384 for ATLAS and 432x336 for CMS) and the pixel analog front end.

The RD53B generation is as the RD53A designed in 65nm CMOS technology and features 50um x 50um sized pixels. Among the many added features are data-merging between neighbouring chips, data compression to reduce the data rate by a factor of 2 and a self-trigger capability. The PLL/CDR and the Shunt-LDO power regulator circuits have improved greatly allowing for a reliable operation. Protection features against overvoltage and overload have been added together with an optional low power mode. To mitigate Single Event Effects (SEE) a Triple Modular Redundancy (TMR) strategy was adopted including self-correction and a triplicated clock tree with skew for critical parts.

The ATLAS pre-production chip ItkPixV1 was submitted in March 2020 and has since been extensively tested and characterized. The CMS pre-production chip CROCv1 is being submitted in May 2021 and incorporates bug fixes and few additional monitoring and diagnostic features.

A general overview of the chip architecture will be given and the characterization and testing of the pre-production chips will be discussed based on results of the ItkPixV1. Depending on the availability of the chip, also preliminary test results of the CROCv1 will be shown.

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Hardware Design of the Generic Rear Transition Module for Global Trigger System of the ATLAS Phase II Upgrade

Authors: Kunihiro Nagano[1]; Weigang Yin[2]

[1] *High Energy Accelerator Research Organization (JP)*

[2] *Brookhaven National Laboratory (US)*

Corresponding Authors: wyin1@bnl.gov, kunihiro.nagano@cern.ch

In the ATLAS Phase-II upgrade, Global Trigger is a new subsystem that will bring event filter-like capability to the Level-0 trigger system. A common hardware platform in ATCA form factor named Global Common Module (GCM) is proposed to be configured as nodes in the Global Trigger. To mitigate the risk and simplify the GCM hardware design, a Generic Rear Transition Module (GRM) is developed. GRM, which is implemented with a Xilinx Versal Prime FPGA and sufficient multi-gigabit transceivers, aims at system control and communication with FELIX, it could also provide additional processing or readout capacity.

Summary (500 words):

The HL-LHC is expected to start operations in the middle of 2027, and to deliver more than ten times the integrated luminosity of the LHC Runs 1-3 combined (up to 4000fb-1). Meeting this requirement poses significant challenges to the ATLAS TDAQ system. In the Trigger and Data Acquisition System upgrade, Global Trigger is a new subsystem, which will perform offline-like algorithms on full-granularity calorimeter data and bring Event Filter-like capability to the Level-0 trigger system.
The Global Trigger consists of three primary components: a MUX layer, a GEP layer, and a demultiplexing Global-to-CTP Interface, all of which use the same hardware implementation to minimize the complexity of the firmware, simplify the system design and improve maintainability. The identical hardware implementation is composed of a Global Common Module (GCM) and an optional Generic Rear Transition Module (GRM). Each pair of GCM and GRM could be configured as two nodes of MUX, GEP, or CTP. The GCM is an ATCA front board, which contains two big processor FPGAs and many multi-gigabit transceivers, used for the major data processing and transmission functions. GRM is an ATCA rear transition module, which contains a Xilinx Versal Prime FPGA and sufficient multi-gigabit transceivers, used for system control and communication with FELIX. Besides, the power consumption of GCM is limited to 350W by the cooling system. It is imposing significant constraints on power consumption, especially when GCM/GRM are used as GEP nodes, which need maximum resources of FPGA logic and transceivers. In this case, GRM is required to provide additional resources for event processing algorithms and data transmission.
To provide more programmable logic resources and transceivers, and achieve a better energy efficiency ratio, the Xilinx Versal Prime FPGA VM1802 is selected for the GRM design. Fig.2 shows the block diagram of GRM. GRM is connected to GCM through Zone3 connectors. Two Si5395 are used for clock cleaners and distributors, the clock source could be configured as the local clocks or remotely clocks from GCM or FELIX with flexibilities. Totally 18 transceivers between GCM and GRM's FPGA are implemented for monitoring, control, and data transmission. Two 12-channel transceivers via FireFly modules are used for communication with FELIX and other possible applications. In addition, there are 40 TX links from Zone3 connectors to expand the readout capability of nodes in the Global Trigger system. All transceivers and FireFly modules support data rate up to 25Gbps. A CERN MMC is used to monitor the health of the board in the ATCA chassis.
The hardware was designed in 2020 and is being tested since February 2021. Now the power rails and the TX links from GCM to GRM have been verified. GTY links from GCM to TX FireFly modules in GRM through Zone3 connectors could work well at 20Gbps. Fig.3 and Fig.4 show the performance of these links at 14Gbps. More progress and details will be reported in the meeting.

ASIC / 61

A Sub-Picosecond Digitally-Controlled Phase Delay

Authors: Roger Rusack[1]; Erich Frahm[2]; Rohith Saradhy[1]; Yahya Tousi[3]; Diba Dehmeshki[3]

[1] *University of Minnesota (US)*

[2] *University of Minnesota*

[3] *The University of Minnesota*

Corresponding Author: roger.rusack@cern.ch

The use of precision timing measurements will be a major tool at the HL-LHC, where it will be used to suppress pile-up and to search for long-lived particles. To control a reference clock with sub-picosecond accuracy, we have fabricated in the TSMC 65nm process a digitally controlled phase shifter. It is composed of a chain of 66 cells, each with a digitally controlled planar wave guide with either a short or long delay. With this a reference clock's phase can be controlled to a precision of 200 fs with dynamic range of 13 ps.

Summary (500 words):

The digitally-controlled phase shifter (DCPS) is an integrated direct digital-to-phase converter with the purpose of enabling accurate and predictable phase adjustment in real time with high efficiency, while occupying a minimal physical footprint.

The operating principle of the DCPS is shown in the attached figure and is best explained by considering the physical characteristics of a TEM wave propagating in a transmission line. In an ideal loss-less transmission line, the TEM mode features a linear dispersion relationship which is equivalent to a constant, frequency-independent time delay.

In order to adjust the propagation speed in the transmission line we break the line into small delay cells. Each cell has a coplanar waveguide structure, with two pairs of parallel ground lines. By switching the return current between the two lines, each unit delay of the line can adjust the equivalent inductance and hence the propagation speed and each delay cell operates in two distinct modes: In the "low-delay" mode the L switches are on and the inner lines carry the return path minimizing the unit inductance of the cell. In the "high-delay" mode the L switches are deactivated. As a result the return path flows through the outer lines, maximizing the inductance.

In order to maintain a true-delay line with minimal dispersion, we simultaneously adjust the unit capacitance in each cell to maintain a stable $\sqrt{\mathrm{L}/\mathrm{C}}$ ratio. For this purpose, we introduce a shunt capacitor in parallel with the signal line. In the low-delay mode, where the inductor is small, the capacitor switch is off, resulting in the inherent capacitance of the structure. In the high-delay mode, the capacitor is added to balance the higher inductance.

The DCPS had been tested with 0.5 to 10 GHz RF signals and with a 160 MHz digital clock. It has shown excellent linearity in the delay, seen in the attached figure, and 4 dB signal attenuation up to 7 GHz, in good agreement with the device simulation.

In our presentation we will describe the design of the delay cell, the results we have obtained with the first version, our plans to extend the dynamic range of the device and the steps we are following to make it radiation tolerant

Posters Production, Testing and Reliability / 62

Performance and Plans for Production of the Powerboard for ATLAS ITk Strip Barrel Modules

Authors: Timon Heim[1]; Karol Krizka[1]; Zhicai Zhang[1]; John Joseph[None]; Evan Paul Mladina[2]; Noah Grayson Zisser[1]

[1] *Lawrence Berkeley National Lab. (US)*

[2] *University of Washington (US)*

Corresponding Author: karol.krizka@cern.ch

The Inner Tracker silicon strip detector (ITk Strips) is a part of the ATLAS upgrade for the HL-LHC. It employs a parallel powering scheme for the high voltage sensor bias and the low voltage to power readout ASIC's. This design requires on-module DCDC conversion and high voltage switching. These are implemented on the Powerboard using a buck converter (bPOL12V) to drop the low voltage, a GaNFET for the HV switch, and a custom ASIC (AMAC) for control and monitoring. This contribution will present the Powerboard performance and the test system that will be used for the production of 15,0000 Powerboards.

Summary (500 words):

The ATLAS upgrade for the HL-LHC contains a new silicon tracker called the Inner Tracker (ITk). The ITk Strip detector is a subset of the ITk with striped silicon sensors. It will employ a powering scheme where a single power supply provides power to several modules in parallel. This includes both the high voltage to bias the sensor and the low voltage to power the on-module electronics. The low voltage is supplied to the supporting stave structure using an external 10-11V. The power of a single module will be managed using a custom electronics board called the Powerboard. The Powerboard has four main functionalities; employ a rad-hard switching DCDC regulator (bPOL12V) to step the low voltage from 11V down to 1.5V for local power, monitor the low and high voltage currents directly on a module, disable power in case of module failure and monitor the local temperature. The last three tasks are accomplished using a custom ASIC called the Autonomous Monitor And Control (AMAC) chip. The AMAC is powered using a rad-hard linear regulator (linPOL12V).

The prototyping phase of the project has been completed. The Powerboard has been successfully used at all levels of the prototype ITk Strips system, ranging from standalone tests to operations on a stave consisting of 14 modules per side. Dedicated tests to ensure radiation hardness and reliability after continuous thermal cycling were performed.

The pre-production of the Powerboard has now started. This phase focuses on scaling the manufacturing procedures to handle the final production of 15,000 Powerboards required for the barrel of the ITk Strip upgrade. A commercial partner that can handle SMD loading and wire bonding has been identified and assembled the first batch of 250 Powerboards. This first batch has gone through a stringent quality assurance (QA) and control (QC) process to ensure high reliability. The QA involves a comprehensive stress testing of a random sampling from each batch. The QC tests are done on every board to identify problems during the assembly. The QC involves standard manufacturing controls followed by a full electrical tests and burn-in.

An all-in-one custom test system was developed to aid with the electrical tests. It consists of a passive carrier board containing multiple Powerboards connected to an active board for testing. The active board contains all necessary circuits to test AMAC communication, monitor low and high voltage power outputs, measure the bPOL12V efficiency at varying loads and detect any EMI outside of the shield box. It is controlled by a commercial mezzanine card containing a Xilinx Zynq-7000 SoC FPGA. The operator connects to the system via a web server running on the SoC. The test setup can be operated in a custom crate for mass burn-in or on table-top for initial electrical testing and reception tests at module assembly sites.

Radiation Tolerant Components and Systems / 63

Radiation hardness and timing performance in MALTA monolithic Pixel sensors in TowerJazz 180 nm

Author: Milou Van Rijnbach[1]

Co-author: Carlos Solans Sanchez [2]

[1] *University of Oslo (NO)*

[2] *CERN*

Corresponding Author: milou.van.rijnbach@cern.ch

The MALTA family of depleted monolithic Pixel sensors produced in TowerJazz 180 nm CMOS technology target radiation hard applications for the HL-LHC and beyond. Several process modifications and front-end improvements have resulted in radiation hardness up to 2e15 n/cm2 and time resolution below 2 ns, with uniform charge collection efficiency across the Pixel of size 36.4 x 36.4 um2 with a 3 um2 electrode size. This contribution will present the results from new cascoded front-end flavour that further reduces the RTS noise and improves the threshold reach, and the comparison of samples produced on high-resistivity epitaxial silicon with Czochralski substrates.

Summary (500 words):

The MALTA family of depleted monolithic Pixel sensors have been produced in TowerJazz 180 nm CMOS technology with small collection electrode and a novel asynchronous read-out that reduces the front-end power needs that allows to capture 100 MHit/s [1-3]. The challenge is to make this designs radiation hard to the levels of the inner trackers of the experiments at HL-LHC and beyond [4]. Prototypes have been produced with several process modifications to improve the charge collection. Starting from an n-blanket extends the junction to the full pixel size (standard), another one with a gap in the n- blanket (NGAP), and a third one with an extra deep p-well structure at the pixel edges (EDPW) [5].
The latest front-end modification flavour introduces a new transistor in series, so called cascoded, along with an increase size for selected transistors, that address the RTS noise and improves the threshold reach. This is important for the uniformity of the matrix because it doesn't have in-pixel tuning of the threshold [6]. Samples have been produced on high-resistivity epitazial silicon, and on Czochralski substrates exhibit larger cluster sizes to those produced on epitaxial silicon before irradiation with an average 1.8 pixels for Cz standard, 1.4 pixels for Cz NGAP, and 1.2 pixels for epitaxial silicon. After irradiation the standard process suffers more from radiation damage, resulting in the NGAP having larger cluster size (1.4 vs 1.2 pixels) than standard modified process. Time resolution evaluated through means of the Pico-TDC ASIC as the time difference of the leading edge of the signal from one of the planes used as a reference and the other planes in a beam telescope setup, yields 2.60 ± 0.05 ns at 6 V for epitaxial high-resistivity, and 1.7 ± 0.1 ns between 10 V and 30 V for the Czochralski samples. This is compatible with the assumption of a larger electrical field in the Czochralski samples.
The work being presented here is of interest for the HEP community and in special for that working on applications for the HL-LHC and beyond. Technical details on the integration with of ASICs like the Pico-TDC might be of interest for the community. This technology is being developed at CERN in the context of the EP R&D and the AIDA innova programmes.

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Posters Systems, Planning, Installation, Commissioning and Running Experience / 65

Description and status of the EMCI-EMP interface

Author: Daniel Blasco Serrano[1]

Co-authors: Andreas Bay Madsen [1]; Morten Haahr Kristensen [1]; Henk Boterenbrood [2]; Paris Moschovakos [1]; Piotr Nikiel [1]; Vladimir Ryjov [1]; Stefan Schlenker [1]

[1] *CERN*

[2] *Nikhef*

Corresponding Author: daniel.blasco.serrano@cern.ch

A novel DCS front-end interface for slow control, composed of two devices, the Embedded Monitoring and Control Interface (EMCI) and the Embedded Monitoring Processor (EMP), is presented. The EMCI, based on the lpGBT and the VTRx+, is placed in a radiation hard environment and is connected to multiple front-ends via eLinks. Up to 12 different EMCIs can transmit data via optical fibre to a single EMP, placed in the back-end in a radiation soft area. The EMP, based on commercial MPSoC module, is configured for data processing and monitoring and is accessible from the network via Ethernet.

Summary (500 words):

The importance of an efficient and reliable DCS increases with the complexity of the high-energy physics experiments. The High Luminosity upgrade of the LHC increases the requirements on the level of radiation tolerance of the detectors and relevant control systems. To fulfil these requirements, a new system based on two devices, the EMCI and the EMP, is being proposed.

The aim of the EMCI, which is usually placed in a radiation environment, is to work as an interface for the control and monitoring data signals going in between multiple front-ends (FE) and the DCS system, while keeping a small factor form (9 cm x 7.5 cm). It is based on the lpGBT, which combines all the signals of the FEs, called eLinks, in one bidirectional channel and interfaces with the VTRx+, the optical transceiver, which transmits the data through a high-speed optical link. The transmission rate towards the back-end (uplink) is 10.24 Gbps and towards the front-end (downlink) is 2.56 Gbps. A single FMC connector integrates all the eLink differential signals to the FEs, as well as additional digital and analog interfaces and power input to the board. After having established a link with the back-end, the EMCI can be remotely re-configured to serve multiple configurations of the front-end.

The EMP is primarily meant to serve as an interface between the EMCI and the distributed back-end of the experiment control system within a commodity Local Area Network. The EMP serves as an optical link transceiver module for non-radiation areas such as counting rooms, supporting the connection of multiple Versatile Link+ (VL+) compatible optical fibres towards the detector front-end and an Ethernet interface towards the back-end. As the EMP is based on a highly flexible System-On-Chip module (Zynq Ultrascale+) with digital and analog interfaces, it may also serve as a general-purpose I/O concentrator with integrated processing platform. The EMP allows running Linux-based software applications, facilitating integration within the control system back-end.

Technical specifications of EMCI are available and several prototypes have already been assembled. A specifically designed test bench is under construction to fully validate the design. The EMP hardware is under design, although two commercial MPSoC modules are currently being evaluated and used to implement a firmware and software solution to serve as an example for specific user designs.

Posters Optoelectronics and Links / 66

Hermes - A robust, low latency, optical link protocol for synchronous data transfer at commercial asynchronous line rates

Authors: Kosmas Adamidis[1]; Gregory Michiel Iles[2]; Costas Fountas[1]; Alexander Howard[2]; Ioannis Bestintzanos[1]; Nikos Manthos[1]; Ioannis Papadopoulos[1]; Konstantinos Vellidis[3]; Stavros Mallios[4]; Tom Williams[5]

[1] *University of Ioannina (GR)*

[2] *Imperial College (GB)*

[3] *National and Kapodistrian University of Athens (GR)*

[4] *CERN*

[5] *Science and Technology Facilities Council STFC (GB)*

Corresponding Author: kosmas.adamidis.kosmas@cern.ch

The Phase-2 CMS Level-1 Trigger and associated upstream systems consist of more than 20,000 25Gb/s optical links, transferring almost a Pb/s synchronously between different back-end processing nodes. The stable operation of these links is essential to avoid the injection of an erroneous signals into the trigger path, potentially leading to a flood of false triggers.

The Hermes protocol, implemented on Xilinx UltraScale+ FPGAs, provides this stability while operating at asynchronous, industry standard, line rates. The protocol design as well as the performance from extensive tests are presented here

Summary (500 words):

The Phase-2 CMS Level-1 Trigger and associated upstream systems must synchronously transfer data between many different processing nodes with 25Gb/s optical links. The data transmitted on these links must remain aligned to the LHC beam to avoid accidentally swamping CMS with a large number of false triggers due to misinterpretation of link data.

Synchronization between different processing nodes is achieved by splitting the link bandwidth into a synchronous part with a fixed number of data words per LHC orbit and an asynchronous part that is used to pad the link with filler words so that the line rate is within the optical transceiver Clock & Data Recovery (CDR) operating range. This approach requires that filler words can be reliably distinguished from data words even in the presence of a bit flip. The Forward Error Correction (FEC) methods used in industry to protect against bit errors (e.g. RS-FEC(528,514) for 25G Ethernet) are not suitable due to their latency. Instead a new approach is needed, which has led to the development of the Hermes link protocol. It combines a toughened protocol layer with rapid re-alignment to minimize downtime due to a failing link. Hermes has shown to be immune to single bit flips at BERs exceeding 1 in 10^9.

Link metadata, CRC checksums and even the alignment markers, used to synchronize to the LHC orbit, are transmitted through the Filler bandwidth so that the entire synchronous bandwidth can be dedicated solely to carrying the data necessary for detecting interesting physics signatures. Separation of Data from Control words is done utilizing the 64b67b encoding scheme, which defines a 3-bit Header alongside every 64-bit word. Apart from word characterization, the Header allows for a simple FEC to ensure that Data and Control words can be safely distinguished. In addition, Hamming (7.4) codes are used to ensure that the type of Control words, particularly those used as Fillers, can be reliably identified in cases of single bit errors.

So far, the Hermes Protocol Firmware have undergone detailed testing by transmitting data between several Phase-2 ATCA processors, all of which have been successful. No bit errors have even been observed. The adoption of the 64b67b encoding has raised concerns about the lack of DC balance, albeit small, introduced by the 3-bit Header, since, apart from the scrambled 64-bit words, the Header will always have disparity of +1 or -1. To counter this the Header toggles between two polarity modes.

The protocol has been implemented on the GTH and GTY transceivers used by the Xilinx UltraScale+ FPGA family and has been tested extensively. The protocol design as well as results on its performance are presented here.

Power, Grounding and Shielding / **67**

rPOL2V5: a compact radiation-hard resonant switched-capacitor DC-DC converter for the CMS HGCAL

Authors: Stefano Caregari[1]; Giacomo Ripamonti[2]; Pablo Daniel Antoszczuk[2]; Stefano Michelis[2]; Stefano Saggini[3]

[1] *National Central University (TW)*

[2] *CERN*

[3] *University of Udine*

Corresponding Author: stefano.caregari@cern.ch

A high power density resonant switched capacitor DC-DC converter (rPOL2V5) has been developed as a possible alternative to the bPOL2V5, of particular interest to the CMS High-Granularity Calorimeter (HGCAL) due to the relatively compact 12nH air-core inductor that it requires. The converter is based on an ASIC developed in a 130nm CMOS technology. It is powered by a 2.5V input, it can supply a maximum current of 3A to the output voltage range 1-1.5V. This work presents the strategies adopted at ASIC and PCB level to bring the converter to maturity, and the electrical and radiation characterization results.

Summary (500 words):

rPOL2V5 is a radiation-hard resonant switched-capacitor DC-DC converter, which can be adopted in a two-stages power distribution scheme proposed for the High-Luminosity Large Hadron Collider experiments. It is a second-stage converter that steps down the voltage from 2.5V to an adjustable output voltage in the range 1-1.5V, providing up to 3A of output current. The converter's module hosts an ASIC designed in 130 nm CMOS (which includes the power switches and the control circuitry) and discrete components such as capacitors and inductors. The resonant switched capacitor topology allows this converter to feature a smaller inductor (12nH) compared its buck converter counterpart bPOL2V5, whose inductor is approximately 8 times bigger (100nH). Thanks to its compactness, rPOL2V5 can be of interest for environments with challenging space constraints, such as the CMS High-Granularity Calorimeter (HGCAL). The harsh environment of HGCAL is characterized by large magnetic field (up to 4 T) and challenging radiation levels: a total ionizing dose (TID) exceeding 200Mrad and a neutron fluence up to 8 x 10^15 1 MeV neq cm-2. Therefore, the converter is equipped with an air-core inductor to be compliant with the magnetic field, while hardening by design techniques have been adopted for the ASIC design. In particular, enclosed layout transistors have been used to avoid TID-induced leakage currents, while triplication of the most important control circuitry has been adopted to protect the ASIC from potentially destructive events, generated by SEEs up to a Linear Energy Transfer of 40 MeV·cm2 /mg.
The first prototype of rPOL2V5 proved the effectiveness of its novel multi-mode control strategy and the tolerance of the converter to a TID of 220 Mrad. Nevertheless, its characterization highlighted a not always reliable operation of the converter and a sub-optimal efficiency in certain operating conditions. This works focuses on the second prototype of rPOL2V5, which has been designed to improve these aspects and bring the converter to maturity. The ASIC control circuitry has been simplified with respect to the previous prototype: two of the four operation modes have been discarded to avoid issues in the mode-to-mode transitions, while the control circuitry has been improved to guarantee safer and enhanced efficiency operation for Vout larger than 1.2V.
The parasitic inductances of the input and output path are responsible for overvoltages on the power devices that could affect the reliability of the converter. These inductances have been therefore studied and reduced by almost 50% compared to the original module by choosing appropriate ESL capacitors and a proper PCB stackup. The first prototype of rPOL2V5 adopted a flip chip assembly and copper filled microvias in pad. In order to ease the manufacturing constraints and costs of the production, a new module that features exclusively through vias outside of the flip-chip area has been also designed. Together with the design strategies at ASIC and PCB level mentioned above, this work presents the electrical and radiation characterization results of this new prototype of rPOL2V5.

ASIC / 68

HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter

Authors: Frederic Dulucq[1]; Damien Thienpont[1]; Abdelmowafak El Berni[2]; Christophe De La Taille[2]; Sebastien Extier[3]; Marek Idzik[4]; Jakub Moron[4]; Aleksandra Molenda[4]; Florent Bouyjou[5]; Alessandro Marchioro[6]; Giulia Bombardi[2]; Tommaso Vergine[6]; Fabrice Guilloux[7]; Krzysztof Piotr Swientek[4]; Miroslaw Firlej[4]; Tomasz Andrzej Fiutowski[4]

[1] *OMEGA - Ecole Polytechnique - CNRS/IN2P3*

[2] *OMEGA (FR)*

[3] *Centre National de la Recherche Scientifique (FR)*

[4] *AGH University of Science and Technology (PL)*

[5] *CEA IRFU - Université Paris-Saclay (FR)*

[6] *CERN*

[7] *Université Paris-Saclay (FR)*

Corresponding Author: fdulucq@in2p3.fr

For the CMS HGCAL, the final version of the 72-channel front-end ASIC (HGCROC3) was submitted in December 2020. HGCROC3 includes low-noise/high-gain preamplifier/shapers, and a 10-bit 40 MHz SAR-ADC, which provides the charge measurement over the linear range of the preamplifier. In the saturation range a discriminator and TDC provide the charge information from TOT (200ns dynamic range, 50ps binning). A fast discriminator and TDC provide timing information to 25ps accuracy. The chip embeds all necessary ancillary services: bandgap circuit, PLL, threshold DACs. We present the experimental results on the latest and final version HGCROC3 received in April 2021.

Summary (500 words):

The HGCROC3 is the final ASIC designed to readout the future High Granularity Calorimeter (HGCAL) of CMS, which will consist of hexagonal silicon sensors for a large part. The HGCAL is designed by the CMS collaboration to replace the existing endcap calorimeters for the High Luminosity phase of the LHC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. The HGCROC chip measures and digitizes the charge deposited in the silicon sensors pads, provides a high precision measurement of the time of arrival (ToA), and transmits the digitized data to the back-end electronics. It also computes, every bunch crossing, digital sums of neighbouring channels which are compressed and then transmitted to the concentrator ASICs through 1.28 Gbps serial links in order to build trigger primitives. The requirements for the front-end electronics are extremely challenging, including dynamic range over 16 bit equivalent (0-10 pC), noise bellow 2500 electrons, high-precision timing information (25 ps) in order to mitigate the pileup effect under high luminosity conditions and low power consumption (below 15 mW/channel). The front-end electronics will face a harsh radiation environment which will reach 200 Mrad at the end of life and 1x10^16 neq/cm². Beyond the analog performance, the chip embeds a large part of digital processing to manage the Trigger and the Data paths: a 2-stage memory buffering is implemented with DRAMs to accommodate the 12.5 ms L1 trigger latency and the readout buffering (respectively 512 and 32 deep memories). The radiation hardening against SEE is done by triplicating all the control logic and the ASIC parameters: each clock cycle, state machines and counters are refreshed with a majority voter. For the data path, a SECDED Hamming algorithm is applied before the L1 buffering. The ASIC outputs its data through six 1.28 Gbps serial links: four dedicated for the trigger path and the rest for the DAQ path. It has 72 channels and the analog chain is composed of: low noise and high gain preamplifier, shaper and a 10-bit 40 MHz SAR-ADC provide the charge measurement over the linear range of the preamplifier. In the saturation range of the preamplifier, a discriminator and a TDC provide the charge information from a Time-Over-Threshold over 200 ns dynamic range using 50 ps binning. A fast discriminator and another TDC provide timing information to 25 ps accuracy. The final HGCROC3 ASIC was submitted (130 nm node) in December 2020 and the first lab tests will start in May 2021. The talk will focus on the description of the main changes compared to the previous ASIC iteration, the problem seen and how they have been mitigated in the design. In addition to that, the talk will report on the first performance results in terms of noise, charge and timing, as well as the digital processing with the triplicated logic inside the ASIC.

Optoelectronics and Links / 69

CMS HCAL VTRx-induced communication loss and mitigation

Author: Grace Cummings[1]

[1] *University of Virginia*

Corresponding Author: gec8mf@virginia.edu

The Compact Muon Solenoid (CMS) Phase 1 Hadron Calorimeter Upgrade (HCAL) saw the first large-scale use of VTRx modules, optical transceivers designed to be radiation and magnetic field

tolerant. During Run II of the Large Hadron Collider, the CMS HCAL experienced a short period of communication loss that revealed a manufacturing weakness in the VTRx affecting nearly half of the communication links. The CMS HCAL Team provided the first observation of this phenomenon, revealed its temperature dependence, and pioneered the mitigation tactic adopted by other LHC experiments. We will present these aspects of the larger VTRx investigation.

Summary (500 words):

During the 2018 data-taking period of Run 2 of the Large Hadron Collider (LHC), the Compact Muon Solenoid Experiment (CMS) experienced communication loss with the newly upgraded Hadron Calorimeter (HCAL) front end electronics. Installed in 2017, the new CMS HCAL Endcap front end incorporated the first large-scale use of the VTRx optical transceivers. These new radiation and magnetic field tolerant transceivers proved to be the origin of the communication loss, with symptomatic devices present in 45% of all HCAL Endcap control links. Anomalous features occur within the monitored Received Signal Strength Indicator (RSSI) current. Under normal operating circumstances, the RSSI should maintain a steady value, proportional to the level of received light. Before communication loss, slow losses in RSSI, termed "drift", were observed. Upon inspection, nearly half of all HCAL Endcap VTRxs exhibited some amount of drift at system power-on. The RSSI circuit itself is not involved in the communication pathway, and the transmitted backend power and optical fiber quality did not appear affected. Therefore, investigation was needed to understand the relationship between communication loss and RSSI. To decouple the VTRx from the rest of the CMS HCAL communication and control module, a custom Raspberry Pi-controlled multi-ADC system was developed. This autonomous setup, coupled with a custom VTRx mounting board, allowed for user friendly monitoring, and quickly tailorable test features. With the development of this simple to use system, multiple VTRx quantities could be read and studied, with minimal physical intervention to the VTRx. This system offered finely tuned temperature control and monitoring. With this, temperature was isolated as the cause of the VTRx communication loss. With the conversion of the test system, normally meant for in situ detector replication, to single-use application, we were able link the drift phenomenon to temperature gradients experienced between the VTRx module and the optical fiber plugged into the VTRx. The modular test setup allowed for the photographic capture of condensation on the fiber face, due to outgassing within the VTRx. While long term solutions are in development, for detector upgrades necessary for Run 3 operation, mitigation techniques are required. The CMS HCAL solution applies advancements used in the HCAL Barrel upgrade to the HCAL Endcap. The HCAL Barrel control electronics uses the VTRx as well, but drift is absent in the barrel. A rework of the HCAL Endcap Next Generation Clock and Control modules completed in winter 2020-2021 remedied the HCAL Endcap drift with the addition of copper heat sinks to the VTRx. The use of heat sinks to disperse heat generated by the VTRx serve as the first example of successful outgassing mitigation in situ.

Systems, Planning, Installation, Commissioning and Running Experience / **70**

Recent results from the first lpGBT-based prototype of the End-of-Substructure card for the ATLAS Strip Tracker Upgrade

Authors: Artur Lorenz Boebel[1]; Harald Ceslik[1]; Mogens Dam[2]; Sergio Diez Cornell[3]; Ingrid-Maria Gregor[4]; Peter Goettlicher[1]; James Michael Keaveney[5]; Joash Nicholas Naidoo[5]; Max Nikoi Van Der Merwe[5]; Jan Oechsle[2]; Stefan Schmitt[1]; Marcel Stanitzki[1]; Lars Rickard Strom[1]; Janet Ruth Wyngaard[6]

[1] *Deutsches Elektronen-Synchrotron (DE)*

[2] *University of Copenhagen (DK)*

[3] *Deutsches Elektronen-Synchrotron (DESY)*

[4] *DESY & Bonn University*

[5] *University of Cape Town (ZA)*

[6] *University of Notre Dame (US)*

Corresponding Author: lars.rickard.stroem@cern.ch

The building blocks of the upgraded ATLAS Strip Tracker for HL-LHC are modules that host silicon sensors and front-end ASICs. The modules are mounted on carbon-fibre substructures hosting up

to 14 modules per side. An End-of-Substructure (EoS) card on each substructure connects up to 28 differential data lines at 640 Mbit/s to lpGBT and VL+ ASICs that provide data serialisation and 10 GBit/s optical data transmission to the off-detector systems respectively. Prototype EoS cards have been designed and extensively tested using lpGBT and VL+ prototypes. The status of the electronics design and recent test results are presented.

Summary (500 words):

The silicon tracker of the ATLAS experiment will be upgraded for the upcoming High-Luminosity Upgrade of the LHC (HL-LHC). The main building blocks of the new strip tracker are modules that consist of silicon sensors and hybrid PCBs hosting the read-out ASICs. The modules are mounted on rigid carbon-fibre substructures, known as staves in the central barrel region and petals in the end-cap regions, that provide common services to all the modules. At the end of each stave or petal, a so-called End-of-Substructure (EoS) card facilitates the transfer of data, power, and control signal between the modules and the off-detector systems. The module front-end ASICs transfer data to the EoS card on 640 Mbit/s differential lines. The EoS connects up to 28 data lines to one or two lpGBT chips that provide data serialisation and uses a 10 GBit/s versatile optical link (VL+) to transmit signals to the off-detector systems. The lpGBT also recovers the LHC clock on the downlink and generates clock and control signals for the modules. To meet the tight integration requirements in the detector, several different EoS card designs are needed. We have produced prototypes of the different designs using the currently available versions of the lpGBT and VL+ ASICs. The EoS is powered by a two-stage DC-DC converter, generating both 2.5 V and 1.2 V out of the incoming 11 V, mounted on a custom-designed daughter board which will be connected to the EoS during assembly. We will here present the current status of the EoS card's electronics design, results from extreme temperature and magnetic field tests, preliminary results from error rate tests in the presence of neutron radiation to test for susceptibility to single-event-upsets and detailed studies of the optical signal quality. We will also discuss the first results from full integration tests with the final design of the DC-DC converter, as we move towards production of the first 5% for final staves/petals. Since each EoS sits at a single-point-of-failure for an entire stave or petal side, a dedicated quality control (QC) and assurance (QA) procedure for the production has been developed. An overview of the QA and QC will also be presented.

Posters Production, Testing and Reliability / 71

PANDORE: an environmental box for ITk integration tests.

Authors: Francesco Costanza[1]; Nicolas Gilbert Allemandou[1]; Eric Chabanne[1]; elodie CORNUDET[1]; Pierre Delebecque[1]; Renaud Gaglione[1]; Andrea Jeremie[2]; Jessica Leveque[3]; Nicolas Massol[1]; Isabelle Mievre[1]; Olivier Prevost[1]; Sebastien Vilalte[1]

[1] *Centre National de la Recherche Scientifique (FR)*

[2] *Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP)*

[3] *LAPP (Annecy-Le-Vieux)*

Corresponding Author: francesco.costanza@cern.ch

PANDORE is the environmental box that is going to be used for the quality control (QC) of loaded local supports of the ATLAS ITk Pixel Outer Barrel (OB) at LAPP. First PANDORE, its interlock system, diphasic CO2 cooling station, and data acquisition system are described. Subsequently, the results of the qualification tests are shown. Given the complexity of the OB system, several other loading sites are going to be needed. By documenting the state-of-the-art of PANDORE, this note aims to help the wide OB community in the discussion for standardizing the QC procedure and equipments of the loaded local supports.

Summary (500 words):

The Inner Tracker (ITk) is one of the key detectors of the High Luminosity (HL) upgrade of the ATLAS experiment at the Large Hadron Collider (LHC). The ITk Pixel at its core is made of three subsystems: the inner system, the outer barrel and the outer endcaps.
Such a complex apparatus requires a collaborative effort in all phases of its design, building, testing and operation. This document focuses on the integration steps in which the sensors are loaded on the

mechanical support structures of the Outer Barrel (OB). Several assembly sites will be qualified to load and test 5000 modules, and to integrate them on about 300 OB local supports. As a part of the quality assurance, the loading and testing procedures must be standardized among the assembly sites. This document describes the current status of PANDORE, the environmental box shown in Figure 1 in the auxiliary material and that is going to be used for the quality control (QC) of the loaded local supports at LAPP (Annecy, France). Most importantly, the qualification tests performed to-date are also presented.
PANDORE, with its internal dimensions of 191/95/100 cm3, can comfortably be used to test the 77,8cm long longerons of the ITk outer barrel, through a 130cm long handling frame. A dew point below -60℃ is ensured with a flux of dry air (0ppm) that can be remotely controlled. PANDORE is light-tight and thermally isolated from the outside environment. To guarantee a safe operation, an interlock and a slow control system has been implemented with a Wago programmable logic controller (PLC) and Node-Red software . Air temperature, dew point, CO2 temperature and pressure, door switches, and emergency buttons are permanently monitored and displayed with a custom graphical interface.
PANDORE is complemented with an evaporative CO2 cooling system called MARTA, designed to reach a temperature of -40℃ with a cooling power of 300W at -30℃. MARTA is remotely controlled by the slow control application through the MODBUS protocol.
All monitored data are published and subscribed through OPC UA and stored in a local influxDB. The visualization of monitoring data and the control of the system is implemented in an harmonized GUI with the Grafana web application, see Figure 2.
A block diagram of the system showing all the main components and their interactions can be found in Figure 3.
The operating temperature of ITk sensors is expected to be -30℃ at the end of HL-LHC which impose very challenging requirements for the QC at the loading sites. The thermal properties of PANDORE herein presented are assessed through thermal cycles with a heat load from a remotely controllable heating cartridge that can dissipate up to 400W. The time needed to perform a thermal cycle and the lowest temperature achievable are very important ingredients for the design of the QC procedure.
By documenting the state-of-the-art of PANDORE, this note aims to help the wide OB community in the discussion for standardizing the QC procedure and equipments of the loaded local supports.

ASIC / 73

First Measurement on TimeSPOT1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End

Authors: Valentino Liberali[1]; Lorenzo Piccolo[2]; Sandro Cadeddu[3]; Adriano Lai[3]; Luca Frontini[4]; Alberto Stabile[5]; Angelo Rivetti[6]

[1] *Università degli Studi di Milano*

[2] *INFN Torino*

[3] *Universita e INFN, Cagliari (IT)*

[4] *INFN and Università degli Studi di Milano*

[5] *Università degli studi di Milano*

[6] *Universita e INFN Torino (IT)*

Corresponding Author: lorenzo.piccolo@to.infn.it

This work presents the first measurements on the Time SPOT1ASIC. As the second prototype developed for the TimeSPOT project, the ASIC features a 32×32 channels hybrid-pixel matrix. Targeted to 4D-Tracking applications in High Energy Physics experiments, the system aims to achieve a timing resolution of 30 ps or better at a maximum event rate of 3 MHz/channel with a Data Driven interface. Power consumption can be programmed to range between 1.2 W/cm^2 and 2.6 W/cm^2. The presented results include operation and performance characterization.

Summary (500 words):

Current plans for particle colliders upgrades aim to increase the statistics on rare events by increasing the beam instantaneous luminosity (up to 7×10 35cm−2s−1). Under this condition the number of pileup events is expected to increase to a value as large as 200, demanding new tracking techniques such as

4D-Tracking to maintain an adequate tracking efficiency and ghost-event rate. 4D-Tracking operates by exploiting both the time and positional information of the particle-detector interaction point. Therefore the development of a system capable of a local high-precision time measurement is critical to sustain the advancement in the field.The TimeSPOT project, by INFN, aims to develop a demonstration 4D-Tracking Detector with a spatial resolution of 55µm and a timing resolution of 30 ps or better. The system will be equipped with sensitive layers of Hybrid-Pixel detectors based on both 3D-Sensors. In this communication we will present the first measurements on the TimeSPOT1 Front-End ASIC, a prototype chip developed in a commercial 28 nm CMOS technology. This chip is the successor of TimeSPOT0,which was comprised of independent test blocks of the components of a FE chain. Compared to the first chip, TimeSPOT1 integrates a 32×32 channels matrix as well as all required logic and drivers for IO operations. The ASIC is testable both stand-alone or coupled with the target sensors via Bump-Bonding. Every Front-End Channel is equipped with a low-jitter (<30 ps) input Charge Sensitive Amplifier (CSA), a discrete time Discriminator and Vernier based Time to Digital Converter (TDC) with an LSB of 10 ps.The CSA features a novel AC-coupled Inverter based core Amplifier with leakage current compensation. The Analog Front-End has digitally configurable power consumption which can be varied between 2.3µW and 32.9µW per channel. The TDC can produce both Time of Arrival and Time over Threshold with an LSB of 10 ps and 1 ns respectively. This TDC power consumption varies with hit-rate per channel, it is estimated to be 20µW when on idle; it consumes 25µW, 45µW and 69µW at 100 KHz, 500 KHz and 1 MHz respectively. Both the 32×32 channels matrix, its service circuitry and power and data paths are integrated in the area that matches the one of the full sensor-matrix. In this way it is possible to build a free from dead-space pixel sensor by correctly routing the input signals to match the sensor grid with the electronics one. The periphery of the chip contains the data-read out paths, LVDS IO drivers and a PLL for clock recovery. Data is derandomized and transmitted to the 8 output driver using an end-of-column readout tree. The system is able to transmit a maximum of 10.24 Gb/s with an estimated power consumption of 100 mW. The system is Data Driven and can be synchronized with an external signal for global time reference.The ASIC has been assembled with its PCB and is now under test. The test comprises the ASIC characterization in different power regimes. Valuable parameters to be extracted from measurement are timing resolution, channels uniformity, peak-datarate and power consumption.

Posters ASIC / 75

Towards a Software-Adaptable Receiver Chain for Particle Detectors

Authors: Lukas Krystofiak[1]; Florian Rössing[2]; christian grewing[3]; André Zambanini[4]; Stefan van Waasen[4]

[1] *Juelich Research Centre*

[2] *Forschungszentrum Jülich GmbH (FZJ)*

[3] *Forschungszentrum Jülich*

[4] *Forschungszentrum Jülich GmbH*

Corresponding Authors: f.roessing@fz-juelich.de, l.krystofiak@fz-juelich.de

Chip design, is a lengthy process, which comes with high development efforts and costs and is a crucial milestone for the overall success of the project. Readout electronics for particle detectors resemble each other to a high degree, thus developing a software-adaptable receiver chain covering a large range of application scenarios is an attractive concept. With a generic approach, designed independently, these risks are shifted to project-independent stages, which substantially reduces development time and costs, enabling also smaller projects and rapid prototyping.
A generic receiver low power system-on-chip is conceptualized. The central block is a software-scalable, high-performance ADC combined with a configurable front-end with adjustable impedance. Succeeded by an SRAM memory as a buffer and a digital signal pre-processing system. The high integration degree and complexity of the system is accompanied by an advanced 28nm CMOS technology, mitigating the area overhead of a generic approach and enabling high-speed electronics at an acceptable power consumption. Common approaches in detector readout use blocks like TDCs for the extraction of information from detector signals. While simpler and inherently efficient, they reduce the options for direct reusability in various application areas and require a repeated design effort. In this novel approach, the sampled waveforms enable sophisticated signal processing, leveraging the potential of a complex system-on-chip in a modern technology. This will enable an increased

resolution for time and energy measurements, as demonstrated by (Jokhovets, 2019). Such methods enable a timing resolution below 100ps from sampling at nanosecond intervals. Furthermore, it will allow a pre-clustering and data reduction on chip, reducing the transmission bandwidth and amount of necessary post-processing hardware. An integrated 16kByte SRAM buffer will allow for local data buffering and reduction of transmission speed, adjustable to the expected hit rates.
For these developments, an in depth study of existing readout solutions was performed, whose results are summarized in this contribution. Additionally, it will give an introduction in the algorithm development process and the developed Simulink framework.
Another focus of this contribution is the software-scalable ADC that consists of similar ADC cores. They can be arranged in different ways to adjust to different specifications. For the core ADC, successive approximation register (SAR) ADCs are implemented as their mostly digital nature scales well with technology, leading to higher performance and decreased chip area. The ADCs can be concatenated which increases the resolution without penalties in sample rate. For the first engineering sample, a high-precision mode with 12 bit resolution and a medium-precision mode with 9 bit is foreseen. The maximum sample rate is 500 MS/s with no bound for the lowest sample rate. For higher rates, the ADCs can also be multiplexed in time (time-interleaving). Using two time-interleaved ADCs for the first prototype, a maximum sample rate of 1 GS/s can be achieved. It is also investigated to use both time-interleaved ADCs independently to read out two channels, gaining flexibility for multichannel designs. The silicon area for the ADC pair is conservatively estimated to 0.24 mm2 , allowing an upscaling of the number of channels in future developments.

Summary (500 words):

A software-adaptable receiver tackles some of the highest challenges in particle detector development. With a generic approach it reach the same performance as a dedicated development, it covers most application fields and can cut down development times and costs. Prototyping and verification of readout methods prior to the building of the complete systems are also facilitated. An in-depth study of existing particle detectors was conducted to define requirements that such a system will have to fulfil. In parallel, a first investigation of configurability is conducted to assess feasibility using an ADC as the central block in the receiver.

Posters Power, Grounding and Shielding / 78

Upgrade of the ATLAS Tilecal High Voltage system

Author: Agostinho Da Silva Gomes[1]

[1] *LIP Laboratorio de Instrumentacao e Fisica Experimental de Part*

Corresponding Author: agostinho.gomes@cern.ch

The high voltage (HV) system of TileCal, the ATLAS central hadron calorimeter, is being upgraded for the HL-LHC, in the so called Phase II Upgrade. In the new configuration for the upgrade, the HV regulation boards are not located inside the detector anymore, they are deployed far from the radiation in a room where there is permanent access for maintenance. This option requires a large number of 100 m long HV cables but removes the requirement of radiation hard boards. HVremote regulation boards and the respective HV supplies boards have been developed and tested, as well as a crate to

Summary (500 words):

he High Voltage system of Tilecal after the Phase II upgrade will consist of HVremote boards and HV supplies boards, located far from the detector in crates, connected to the detector by 100 m long cables. Inside the detector there will be passive HVbus boards that are used to bring the HV to each of the photomultiplier tubes (PMTs) located in mini-drawers inside the girders of the modules.
The HVremote boards are the boards that regulate the HV for each individual PMT of Tilecal. The number of boards needed for the Tilecal operation is 256. There is one input HV (-830 or -950 V) for each 24 channels and the voltage of each channel can be regulated down individually in a range of the order of 350V as in the current Tilecal design [1]. The primary HV is provided by Hamamatsu

C12446-12 modules located in the HV supplies boards, and two primary HV inputs are used to provide HV for 48 channels in the case of the Barrel modules or for 32 channels in the case of the Extended Barrel ones. Relative to the current Tilecal HV system, the main functional improvement is the addition of on/off control for each group of 4 channels complemented by a jumper for each individual channel. The operation in the absence of radiation allowed the simplification of the regulation loops with the removal of some transistors. The control and monitoring, that in the current Tilecal version is done with HVmicro boards [1] that communicate with the DCS PCs via CANbus, was completely redone.
The communication and control is done via SPI bus through an ethernet interface. Most of the tests and development of the control and monitoring of the HVremote and HV supply boards was done using Raspberry Pi, with the solutions being later moved to a System on Chip solution (Zybo Z7 Zynq) that allows the simultaneous usage of two SPI buses, one for the HVremote boards and the other one for the HV supply boards.

HVremote and HV supply boards prototypes have been tested in the laboratory and performance results will be presented.
[1] R. Chadelas et al., "High voltage distributor system for the Tile hadron calorimeter of the ATLAS detector", ATLAS-TILECAL-2000-003, 2000, https://cds.cern.ch/record/436230

Posters Systems, Planning, Installation, Commissioning and Running Experience / 79

The TileCal TDAQ interface module for the Phase II Upgrade of the ATLAS Tile Calorimeter

Authors: Xiaoguang Yue[1]; Tigran Mkrtchyan[1]

[1] *Ruprecht Karls Universitaet Heidelberg (DE)*

Corresponding Authors: tigran.mkrtchyan@cern.ch, xiaoguang.yue@cern.ch

In order to meet the requirements for the High Luminosity-Large Hadron Collider (HL-LHC), a completely new architecture will be used to redesign the readout electronics of the ATLAS Tile Calorimeter (TileCal) system for the ATLAS Phase-II Upgrade. In the new Trigger and Data AcQuisition (TDAQ) architecture, the output signals of the Tile detector cells will be digitized in the front-end electronics and transferred for every bunch crossing to the off-detector Tile PreProcessor (TilePPr) modules through high-speed optical links. The TilePPr will then reconstruct energy deposited in each cell from the digitized samples and transfer the pre-processed cell energy data further

Summary (500 words):

In order to meet the requirements for the High Luminosity-Large Hadron Collider (HL-LHC), a completely new architecture will be used to redesign the readout electronics of the ATLAS Tile Calorimeter (TileCal) system for the ATLAS Phase-II Upgrade. In the new Trigger and Data AcQuisition (TDAQ) architecture, the output signals of the Tile detector cells will be digitized in the front-end electronics and transferred for every bunch crossing to the off-detector Tile PreProcessor (TilePPr) modules through high-speed optical links. The TilePPr will then reconstruct energy deposited in each cell from the digitized samples and transfer the pre-processed cell energy data further to the Tile TDAQ interface (TileTDAQi) modules. The TileTDAQi will then group the cell energy data to generate trigger primitives with different granularity and implement interfaces based on different requirements from the Feature Extractor (FEX) and other trigger processor modules. At the same time, the TilePPr will also store the energy information in pipeline memories and send selected data out to the ATLAS data acquisition system. The TileTDAQi module will be implemented on an Advanced Telecommunications Computing Architecture (ATCA) Rear Transition Module (RTM) format and will operate under the ATCA framework. This contribution will provide an overview of the new TileCal back-end electronics architecture and present the design and implementation of the TileTDAQi prototype together with preliminary test results.

Posters Radiation Tolerant Components and Systems / 80

Readiness of the radiation tolerant link Daughterboard for the High Luminosity upgrade of the ATLAS Hadronic Calorimeter

Author: Eduardo Valdes Santurio[1]

[1] *Stockholm University (SE)*

Corresponding Author: eduardo.valdes@cern.ch

The upgrade of the ATLAS TileCal for the HL-LHC uses a Daughterboard that serves as a hub interfacing the on-detector with the off-detector electronics. The Daughterboard design features ProASIC FPGAs, Kintex Ultrascale FPGAs and CERN GBTx ASICs. The design minimizes single points of failure and radiation damage by employing a double-redundant scheme, using TMR and Xilinx SEM strategies, adopting CRC verification in the uplinks and FEC in the downlinks, and using a dedicated SEL protection circuitry. We present a summary of the studies on the Daughterboard revision 6 performance and the radiation qualification tests of the design components.

Summary (500 words):

The upgrade of the ATLAS Hadronic Calorimeter for the High Luminosity Large Hadron Collider (HL-LHC) has motivated progressive redesigns of a radiation tolerant link Daughterboard that serves as a hub interfacing the on-detector with the off-detector electronics via two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks powered by four SFP+ Optic transceivers. Configuration commands and LHC timing are received by the downlinks to be propagated to the front-end through two Microsemi ProASIC FPGAs, two CERN radiation hard GBTx ASICs and two Kintex Ultrascale FPGAs. In parallel, the Kintex FPGAs send continuous high-speed readout of digitized PMT samples, detector control system and monitoring data through the uplinks. The Daughterboard design minimizes single points of failure and radiation damage by employing a double-redundant scheme, using Triple Mode Redundancy (TMR) and Xilinx Soft Error Mitigation (SEM) in the FPGAs to mitigate Single Event Upset (SEU) rates, adopting Cyclic Redundancy Check (CRC) error verification in the uplinks and Forward Error Correction (FEC) in the downlinks, and using a dedicated Single Event Latchup (SEL) and over-current protection circuitry to avoid hardware damages.

Around 930 Daughterboards will be produced as the contribution of Stockholm University to the the ATLAS Upgrade for the HL-LHC era. Before settling on a final board design that could be taken into a production stage, radiation test campaigns have taken place to qualify the different components of the board for Total Ionizing Dose (TID), Non Ionizing Energy Losses (NIEL) and Single Event Effects (SEE). The Kintex Ultrascale FPGA firmware has a complex clock distribution and a timing scheme with multiple clock inputs, some of them to be multiplexed accordingly to the firmware needs. The clock inputs come from various sources such as the two GBTxs, an oscillator and the six ADCs sitting on a MB side. The PCB design and the firmware was optimized so that the Kintex ultrascale FPGA can manage more than 18 independent clock inputs to drive all the required functionalities. Besides testing the clocking scheme, the set of tests performed to verify the DB core functionalities include GTH link reliability and stability tests, IDDR-SERDES readout reliability and stability tests, GBTx-ConfigBus configuration bus interface, current and power monitoring system.

We present a summary of the studies that took place to verify the reliability if the Daughterboard revision 6 design performance, and the radiation qualification tests of the components used for the design.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 81

TEPX as a high-precision luminosity detector for CMS at the HL-LHC

Author: Mykyta Haranko[1]

[1] *CERN*

Corresponding Author: mykyta.haranko@cern.ch

The CMS BRIL project upgrades its instrumentation for the Phase-2 detector to provide high-precision luminosity and beam-induced background measurements. A part of the CMS Inner Tracker - the Tracker Endcap Pixel Detector (TEPX) - will allocate a fraction of the read-out bandwidth for luminometry. In the talk, the advantages and implications of the proposed approach are highlighted. A dedicated luminosity trigger distribution system is introduced together with its demonstrator system. A demonstrator of the real-time on-FPGA pixel cluster counting algorithm is also presented.

Summary (500 words):

The High-Luminosity LHC is expected to provide instantaneous luminosity a factor of five larger than provided by the existing accelerator system. This enables a higher precision for physics measurements, but also implies higher radiation levels. The precision target of the luminosity measurements is 2% real time and 1% with final calibration. In addition, the upgraded layout of the CMS Tracker also necessitates the replacement of the currently operated dedicated luminosity detectors. The BRIL Phase-2 strategy relies largely on the use of trigger primitives generated by various subsystems to measure luminosity by installing a dedicated histogramming firmware module on the back-end FPGAs. The TEPX system does not provide trigger primitives and features triggered read-out. However, TEPX modules are designed to allow a trigger bandwidth of up to 1 MHz, while physics trigger rates of only 750 kHz are expected. This allows to allocate additional bandwidth (+10% amounting to 75 kHz) to luminosity triggers. A dedicated luminosity trigger distribution system, also referred to as BRIL Trigger Board (BTB) will be built based on the Phase-2 ATCA hardware. For each group of TEPX modules, triggered luminosity data will be acquired by a back-end card and forwarded to a luminosity processor, both based on the Apollo ATCA platform. Each luminosity processor will be running an instance of the pixel cluster counting algorithm for each CMS Read-Out Chip (CROC) connected to the ATCA card. Cluster counts will be accumulated in histograms and then forwarded to the BRIL online software for final processing. This structure will allow to include TEPX in the BRIL luminosity measurement infrastructure. In addition, a part of TEPX, known as Disk 4 Ring 1 (D4R1), will not be used for tracking due to the lack of a sufficient number of tracking points and therefore will be dedicated entirely to the BRIL project. This opens a potential to use the full trigger bandwidth for luminosity measurement. The independence of the system will also allow to use it for the beam-induced background measurements even when CMS is not in data-taking mode. The latter implies the requirement for the TEPX D4R1 front-end and back-end to run during the LHC acceleration cycles, when the bunch clock frequency is not fixed. A set of tests was performed to prove the possibility of such operation, including tests of the prototype front-end modules, the back-end links and the development of the BRIL Trigger Board demonstrator firmware. In order to validate the design for real-time cluster counting with an affordable number of luminosity processors, a demonstrator pixel cluster counting algorithm has been developed and tested using CMSSW event simulations as input.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 82

SRS-based Timepix3 readout system

Author: Markus Gruber[1]

Co-authors: Jochen Kaminski [1]; Klaus Desch [1]; Leonie Richarz [1]; Tobias Schiffer [1]; Tomasz Hemperek [1]

[1] *University of Bonn (DE)*

Corresponding Author: markus.gruber@cern.ch

Based on Timepix3 several detector types can be built by combining it with a sensor or a photolithographically postprocessed gas amplification stage. With these combinations applications like beam telescopes and gas-based X-ray detectors can be realized.
The detectors can range from single- to multichip and from low- to high-rate applications, thus a modular and scalable system is needed. It is based on the basil framework and supports several

FPGAs. Furthermore, it offers optional monitoring interfaces for detector parameters.
I will present the readout system, its scalability and how it offers the needed functionality for different detector types.

Summary (500 words):

With the combination of the highly granular pixel ASIC Timepix3 by the Medipix-3 Collaboration and several technologies like bump-bonded sensors, microchannel plates (MCP) and photolithographically postprocessed gas amplification stages (InGrid) we are developing a range of detectors. For example, we are using the combination of the ASIC and an InGrid for the development of X-ray detectors for X-ray polarimetry and for axion search at CAST and IAXO. Based on the combination of the ASICs and silicon sensors we are developing a tracker or respectively a beam telescope. The combination of the ASIC and a microchannel plate will be used for neutron detectors.
As this range of detectors has several requirements towards the readout system and a wide range of designs from low- to high-rate (Hz to MHz) and from single- to multichip, a versatile readout system is needed which adapts these applications without producing too much overhead for the others. To fulfill these requirements, we are developing a modular and scalable readout and control system based on the basil framework - a modular data acquisition system and system testing framework. The fully open-source implementation uses Verilog for the firmware and Python for the software. The system supports several FPGA boards to offer different applications a range of capabilities. One of these FPGA boards is the Scalable Readout System (SRS) by RD51 which offers scalability in low to medium rate applications. For high-rate applications we are working towards the firmware implementation on Xilinx adaptive compute acceleration platform.
Besides the scalability, the system offers an optional monitoring interface via a microcontroller for monitoring chip temperatures and power supply voltages. Additionally, further external sensors could be connected to the monitoring system for example via I²C or SPI. For controlling the full system, the software offers a command line interface and a graphical user interface. Both interfaces also include an online event display to monitor the raw data. Additional meta data and data of the monitoring system is stored in a database and can be visualized with the monitoring tool Grafana.
This contribution will give an overview of the full system, its current state and further developments. It will be shown how the scalability and the modular design are implemented as well as how the different requirements for the applications are realized.

Trigger / **83**

The Ocean and Octopus designs for the Phase-2 upgrade of the CMS L1 muon trigger

Authors: Michail Bachtis[1]; John Jones[1]; Maxx Tepper[1]

[1] *University of California Los Angeles (US)*

Corresponding Author: michail.bachtis@cern.ch

The throughput and processing requirements of the CMS L1 Trigger for HL-LHC require platforms with high-end FPGAs and many high speed optical links. The Ocean platform features the largest ZYNQ Ultrascale+ SoC and 72 transceivers connected to on-board optics reaching rates up to 28 Gbps. The Octopus^2 design targeted for the CMS Muon Trigger at HL-LHC features a Virtex Ultrascale+ 13P FPGA in and 128 bi-directional links connected through copper to QSFP and QSFP-DD optics. Signal integrity results, comparison of different layout strategies and heat management for large FPGAs featuring lidless packages will be discussed.

Summary (500 words):

The CMS Phase-2 L1 Muon Trigger performs combined muon reconstruction in the CMS experiment using both the tracker and the muon system. The system requires a throughput of about 20 Tbps and large FPGA processing logic. The latest Ultrascale+ FPGAs
by Xilinx satisfy the processing and I/O requirements but impose challenges on PCB design, power, and heat management.
The Octopus^2 mezzanine features a VU13P FPGA in the A2577 package and 128 optical transceivers

that reach speeds up to 25 Gbps. The board features 16 Samtec Accelerate connectors (8 per side) that connect 128 serial transceivers to optics reaching speeds up to 28 Gbps. The PCB was designed using High Density Interconnect (HDI) techniques achieving a layer count of 14 and a form factor of 15x12.5 cm. In spite of the small size, the board supports core power up to 300 W and features a second smaller assisting Kintex 7 FPGA with DDR3 memory and novel custom build board to board connectivity through flex. The PCB is optimized for conduction cooling and the small size of the mezzanine allows it to be mounted on a large heatsink minimizing mechanical PCB deformations and optimizing heat dissipation. Heat management is optimized further by deploying lidless FPGAs and designing a custom heatsink that provides direct contact to the die. The Samtec accelerate technology enables several types of supported optics. The board connects to an optical module that features cutting edge QSFP-DD optical transceivers that support 200 Gbps I/O bandwidth per cage. The design strategies will be described together with results for heat management and signal integrity with different optics and different trace geometries. Results from operation of the mezzanine on an Advanced TCA board will be shown.
The signal integrity results and operational capabilities of the board will be compared to the previous generation Ocean processor that is the first board in CMS that features one large single System-On-Chip (ZU19EG) and 72 optical transceivers reaching speeds up to 28 Gbps.

Posters Programmable Logic, Design Tools and Methods / 84

Versatile free-running ADC-based data acquisition system for particle detectors

Author: Lioubov Jokhovets[1]

Co-authors: Pawel Kulessa [2]; Andreas Erven [3]; Christian Grewing [3]; Tanja Hahnraths von der Gracht [3]; Markus Harff [3]; Henner Ohm [3]; Krzysztof Pysz [4]; James Ritman [5]; Christian Roth [3]; Mario Schlösser [3]; Thomas Sefzick [3]; Valeriy Serdyuk [3]; Stefan van Waasen [3]; Peter Wintz [3]

[1] *Forschungszentrum Jülich GmbH*

[2] *Forschungszentrum Jülich, GSI Darmstadt*

[3] *Forschungszentrum Jülich*

[4] *Institute of Nuclear Physics, Cracow*

[5] *Forschungszentrum Jülich, GSI Darmstadt, Ruhr-Universität Bochum*

Corresponding Author: l.jokhovets@fz-juelich.de

A high density data acquisition system integrating over 2000 channels inside of a single OpenVPX crate is intended to be used in different applications e.g. gaseous or scintillator-based particle detectors. 14 payload slots, controller and data concentrator communicate one with other via multi-gigabit backplane. Each payload slot consists of a front module for digital and a rear transition module for analog processing. This single pair implements 160 full chains including amplification/shaping, sampling, and feature extraction. Sampling rate and ADC resolution are configurable for 80-1000 MS/s, 8-14 bit. The system has been tested at COSY at Jülich Research Center (Germany).

Summary (500 words):

In this work a configurable free-running data acquisition (DAQ) platform for large scale experiments is presented. This DAQ is intended to be used in different applications, such as gaseous detectors, neutron scattering experiments or PET-TOF detectors. The detector electronics consists of a number of sensors (photodetectors, straw tubes, etc.) coupled to the Nyquist filters, amplifiers, free-running ADCs, and a processing unit (FPGA) delivering events, energies and arrival time marks to a backend in real time. The DAQ is implemented inside of an OpenVPX crate. It includes all analog and digital processing stages and currently uses discrete electronics. However, increasing of the integration level is possible by step-by-step replacing of discrete components with ASICs.
There are 16 slots in the crate: 14 payload, one controller and one data concentrator slot. The slots are connected one with other via backplane with multi-gigabit bandwidth. The OpenVPX standard permits that modules can be plugged into the crate from both the rear and front sides. The backplane connects a module from rear side to its adjacent module on front side. This allows analog and digital processing

units to be inserted from different sides. They can be developed and modified independently. The crate room is effectively used increasing the number of processing channels integrated in the crate. The analog unit includes 160 amplification/shaping channels and a row of Samtec connectors for sensor signals. The amplified/shaped signals pass through the backplane connector to the digital unit where 160 sampling channels and single processing FPGA are placed. Thus, one pair of modules provides 160 signal chains, and the whole single 19“-crate offers 2240 channels. It is foreseen, that data can be delivered to the backend system with bandwidth over 100 gigabits per second, and the system can be synchronized via such nets as White Rabbit or SODANET.
The high system flexibility relates to a wide range of sampling rates (from 80 up to 1000 MS/s). It is caused also by FPGA capability to implement different processing algorithms. In addition, the multi-gigabit backplane for data exchange between all slots benefits application specific functions, such as time sorting, cluster building, pre-tracking, and coincidence search. The number of processing channels is reduced at higher sampling rates (over 250 MS/s).
A proper choice of shaping parameters, sampling rate and timing algorithm results in a low power consumption of a single analog/sampling/processing chain (below 350 mW). Careful length-matched board routing and synchronization based on zero-delay clocks allow on-FPGA data capturing without individual channel setup delay. Thus, all channels are captured and processed as a single one.
The DAQ has been tested in the proton beam with gaseous particle detector – straw tube tracker at COSY (Cooler Synchrotron) at Jülich Research Center (Germany). The firmware for arrival timing, energy calculation and pile-up reconstruction as well as FPGA resource usage are also reported in this work.

Posters Optoelectronics and Links / 85

Development of a high bandwidth readout chain for the CMS Phase-2 pixel upgrade

Author: Caleb James Smith[1]

[1] *The University of Kansas (US)*

Corresponding Author: caleb.smith@ku.edu

The CMS collaboration is building a new inner tracking pixel detector for the High-Luminosity LHC. Each pixel chip will be controlled with a single serial input stream at 160 Mbps and will send out data via four CML 1.28 Gbps outputs. The modules will be connected with up to 1.6 m long low-mass electrical links to the low power gigabit transceivers (lpGBT) and versatile transceivers (VTRx+) that send the data optically to off-detector electronics at 10 Gbps. The development and the characterization of these components will be presented along with system tests of the readout chain.

Summary (500 words):

The High-Luminosity LHC (HL-LHC) will provide CMS with a peak instantaneous luminosity of 7.5 × 10^(34) cm^(−2) s^(−1) starting in 2027. Compared to the LHC, the HL-LHC will have up to 200 proton-proton collisions (pileup) per event and will shower CMS with a higher radiation fluence. To prepare for this data taking environment, the CMS Tracker will be fully replaced in the Phase-2 upgrade. The new inner tracker (the pixel detector) will have about two billion silicon pixels installed.

The detector will be built using hybrid pixel modules, and the sensor data will be processed by a custom readout chip (ROC) developed by the RD53 collaboration. The data from these pixel modules will be sent over up to 1.6 m long low-mass electronic links at 1.28 Gbps to port-cards mounted on the support structure inside the detector. The port-cards are dedicated printed circuit boards carrying the low power gigabit transceivers (lpGBT) and versatile transceivers (VTRx+) that concentrate the 1.28 Gbps electrical signals, convert them to 10 Gbps optical signals, and send them to back-end electronics that are based on FPGA boards.

The prototype low-mass electrical links are being developed and characterized with a series of measurements. The signal quality is assessed using eye diagrams to quantify the amplitude and jitter as well as identifying any distortion. Cross talk effects over electrical links bundled closely together are also studied. As a next step, single ROC cards and pixel modules are read out by electrical links connected

to an FPGA board and/or a scope. These tests are used to understand the transmission characteristics of the ROC and the flex circuit on the module and how to optimize the transmission parameters of the CML drivers (amplitude, pre-emphasis) of the chip. Eye diagrams and bit error rate tests are used to quantify the signal integrity and identify any source of distortion in the electrical part of the readout chain. In parallel, dedicated setups with the port-cards reading out single ROC cards with short coaxial cables have been used to test the prototype port-card and validate the optical part of the readout chain. Finally, the entire readout chain is put together in an ultimate readout system test where pixel modules are read out by long electrical links connected to port-cards, which send the optical signals to the back-end FPGA boards. The developments and test results described above will be presented in this contribution.

ASIC / **86**

First experimental results with the version TOFHIR2X of the front-end ASIC of the MTD/BTL detector in the CMS experiment

Authors: Edgar Albuquerque[1]; Ricardo Bugalho[1]; Luis Ferramacho[2]; Miroslaw Firlej[3]; Tomasz Andrzej Fiutowski[3]; Rui Francisco[None]; Michele Gallinaro[4]; Marek Idzik[3]; Jakub Moron[3]; Tahereh Sadat Niknejad[5]; Luis Oliveira[6]; Jose Carlos Rasteiro Da Silva[5]; Joao Varela[5]; Krzysztof Piotr Swientek[3]; Miguel Silveira[4]; Rui Silva[7]

[1] *PETsys Electronics*

[2] *PETSys Electronics SA*

[3] *AGH University of Science and Technology (PL)*

[4] *LIP Lisbon*

[5] *LIP Laboratorio de Instrumentacao e Fisica Experimental de Part*

[6] *DEE, CTS-UNINOVA FCT-UNL, Caparica*

[7] *LIP*

Corresponding Author: tniknejad@lip.pt

TOFHIR2 is the front-end ASIC for the barrel timing layer (BTL) of the MIP timing detector for the CMS upgrade for HL-LHC, aiming at 30-60 ps resolution throughout HL-LHC lifetime. The BTL consists of LYSO:Ce crystals coupled to SiPMs which will suffer radiation damage. Relative to the first version of the front-end ASIC (TOFHIR2A), TOFHIR2X implements improved circuitry for mitigation of the SiPM dark count noise (DCR) as well as a new current mode discriminator. We present an overview of the TOFHIR2 requirements and design, simulation results and the first measurements with TOFHIR2X silicon samples associated to LYSO/SiPM prototype sensors.

Summary (500 words):

The MIP Timing Detector (MTD) will provide timing of charged particles with high precision allowing to extend to the time domain the association of charged particles to the ~200 concurrent proton collision vertices occurring at each bunch crossing in the High-Luminosity LHC (HL-LHC).

The MTD will consist of barrel and endcap timing layers, BTL and ETL respectively. The BTL is a thin standalone detector based on scintillation LYSO:Ce crystal bars read-out on both ends by silicon photomultipliers (SiPMs). The full BTL detector has about 330 thousand SiPM channels.
Dedicated ASIC electronics will be used to readout the SiPM arrays. The readout solution uses the new TOFHIR2 (Time-of-Flight at High Rate) chip. The main requirements for the BTL electronics are: (1) to measure the timing of minimum ionizing particles (MIP) with a precision of 30 (65) ps at the beginning (end) of HL- LHC; (2) to provide a measurement of the signal amplitude with <5% precision for time-walk corrections. Additionally, the chip has to cope with a MIP input rate of 2.5 M hit/s corresponding to the expected maximum channel occupancy of 7% and to have an output bandwidth of 640 Mb/s. The chip should have a static power consumption lower than 15 mW per channel.
The ASIC has 32 channels, each channel containing one pre-amplifier, two post-amplifiers for timing and energy measurements, three leading edge discriminators, two time-to-amplitude converters (TAC) and one charge-to-amplitude converter (QAC) sharing one 40MHz 10-bit SAR ADC and local control logic. The input pre-amplifier provides a low impedance input to the sensor's current signal. The input

current is replicated into three branches for timing, energy discrimination and charge integration.
Pulse filtering is included in the post-amplifiers to mitigate the deterioration of time resolution due to the large dark count rate (DCR) induced by radiation (up to 55 GHz) and due to pile-up of LYSO pulse tails. The filter creates an inverted and delayed replica of the input current that is added to the original signal. The processing is done in current mode which allows for large bandwidth in a simple implementation. The delay line is implemented as a set of RC nets with programmable taps.
The first full version of TOFHIR2 (32 channels and complete functionality) has been tested. The performance of TOFHIR2A match well the simulation expectations. The service blocks, digital readout, front-end amplifiers, DCR noise cancellation, TDCs and QDCs were validated. Successful TID and SEU radiation tests have been performed.
The second version, TOFHIR2X, has an improved version of the front-end amplifiers and DCR cancelation module, as well as fast current discriminators, instead of voltage discriminators, matching directly the current output of the pulse filters. Simulation results show that a time resolution of ~23 ps (~65 ps) at the beginning (end) of HL- LHC can be achieved (figure 1).
TOFHIR2X ASIC prototype will be received for testing by the end of May. At the conference first measurements with TOFHIR2X silicon samples associated to prototype LYSO/SiPM sensors will be presented.

Posters ASIC / 87

Event driven readout system with non-priority arbitration for radiation detectors

Authors: Dominik Górni[1]; Grzegorz Deptuch[1]; Sandeep Miryala[1]; D. Peter Siddons[1]; Anthony Kuczewski[1]; Abdul Rumaiz[1]; Gabriella Carini[1]

[1] *Brookhaven National Laboratory*

Corresponding Author: dgorni@bnl.gov

A new data driven readout architecture for highly granular pixel detectors is presented. It incorporates, inter alia, an asynchronous arbitration tree based on Seitz' arbiters thanks to which there is no imposed prioritization and protection against glitches during readout is provided. The system allows not only reading the pixel activity, but also retrieving additional data, both analog and digital, from them. A novel in-channel logic allows the entire readout process to be split into consecutive phases for additional flexibility. All operations are controlled by only one edge of the clock signal so there is no dead time between readouts.

Summary (500 words):

A new data driven readout architecture for highly granular pixel detectors is presented. The area occupied by the arbitration tree and the channel logic is small and allows minimizing the pixel size. A block diagram of the system is shown in Fig. 1. It incorporates, inter alia, an asynchronous arbitration tree based on Seitz' arbiters, thanks to which the imposed prioritization, known from prior art, was eliminated in favor of arbitration with memory elements. Therefore, a glitch-free protection against switching over to other channels during the readout procedure is gained on one hand, and snapshotting of the states of the channels prior to the arbitration is not needed on the other hand. The system allows not only reading the pixel activity as their addresses, but also retrieving additional data from the them. Novel, yet simple, is in-channel logic, shown in Figs. 2 and 3, that allows dividing the entire readout transaction into multiple phases, with the possibility of dynamically configuring their number. This function is suitable for reading out neighbors in the case of charge sharing. Another advantage of the presented system is the simplification of the entire readout scheme, as it is controlled by only one edge of the clock signal sent into the arbitration tree and the clock's duty cycle does not necessarily have to be fixed as long as well-known timing dependencies are met. There is no dead time between readouts from different pixels either, as shown on the waveforms in Fig. 4, where a readout from the next requesting pixel follows almost immediately previous one. The both latter features are related to the method of synchronization with the external acquisition system, which takes place almost naturally on the global logic side, so that no distribution of the system clock to each of the channels is required (leading to power savings). Each readout is initiated only during an active level of the clock, and the duration of the inactive level of the clock is the minimum guaranteed time the bus has for settling down

new data from the channel. Simultaneously with the change of the clock to the active state, data from the bus are latched in the output periphery and a new acknowledge is generated and distributed. Data latched in the periphery are sent, e.g. serially, to the acquisition system as a bitstream. If there are no channels requesting being read out, a mechanism to keep the synchronization with external system self-activates. Using the pull-ups and pull-downs, an empty data pattern is set on the data bus and is latched in the output periphery in the same way as regular channel data. The described architecture is developed, for reading out multichannel radiation detectors, particularly pixels detectors, where data sparsification is required. It is suitable for new generation of X-ray and charged particles detectors such as the new ITS3/EIC pixel detector. However, it can also be used to read channels one by one in the so-called imaging mode.

Posters Systems, Planning, Installation, Commissioning and Running Experience / **88**

Electronics Integration for the GE2/1 and ME0 GEM Detector Systems for the CMS Phase-2 Muon System Upgrade

Authors: Stephen Butalla[1]; Marcus Hohlmann[1]

[1] *Florida Institute of Technology (US)*

Corresponding Author: stephen.butalla@cern.ch

With the projected five-fold increase in instantaneous luminosity resulting from the High Luminosity upgrade of the Large Hadron Collider, the CMS experiment is in the process of upgrading its muon spectrometer. Two triple-GEM detector systems—the GE2/1, which is currently in the early mass-production phase, and the ME0, currently in the prototyping phase—are undergoing frontend electronics integration. This presentation discusses the current status of the electronics integration effort on full-size chamber prototypes by the CMS GEM collaboration, including results of grounding studies to reduce noise in the system, and the future prospects of the frontend electronics readout system.

Summary (500 words):

With the precipitous increase in muon flux rate in the forward region of the Compact Muon Solenoid (CMS) experiment resulting from the High Luminosity upgrade of the LHC, the muon spectrometer of the CMS experiment is undergoing its Phase-2 upgrade. This talk presents the frontend electronics integration effort by the CMS GEM collaboration on two new triple-GEM detector systems for the CMS experiment—the GE2/1, which is currently in the early mass-production phase, and the ME0, currently in the prototyping phase. Specifically, we discuss the challenges of noise reduction in the GE2/1 detector system and our solution, as well as a summary of the overall status of electronics integration, aligning with the Systems, Planning, Installation, Commissioning, and Running Experience category.

The frontend electronics and their calibration and readout procedure of the GE2/1 are at relatively mature stage of development. The frontend electronics consist of a GEM electronics board (GEB) which is secured to the readout board of a GE2/1 module, and is responsible receiving the rest of the frontend electronics. These include five FEASTMP CLP DC-DC converters, 12 VFAT3 ASIC chips mounted on Plugin Cards, which connect to the readout board and the GEB, and the Optohybrid (OH) board, which is an Artix-7 FPGA-based board which serves to collect and distribute the trigger/DAQ information between the frontend ASICs and the backend advanced mezzanine card via optical signals from Versatile TransReceiver and Versatile Twin-Transmitter modules on the OH. Figure 1 displays a photo of a GE2/1 chamber instrumented with frontend electronics.

The electronics integration procedure for the GE2/1 chamber consists of tests that connect, calibrate, and program the VFAT3 ASICs. The first is a connectivity test, which establishes communication with the various ASICs on the OH and checks the functionality of the trigger links, programs the FPGA, and performs phase scans to align and program the VFAT3 ASICs with a common data transmission phase. The next procedure consists of characterizing the Digital-to-Analog Converters (DACs), with subsequent noise measurements made in two different manners: one via the data path and one via the trigger path. Figure 2 displays an example noise distribution of all 128 channels for each of the 12

VFAT3 ASICs on one GE2/1 module. This type of noise scan is used to quantify the baseline and overall reduction in noise from the various grounding schemes considered.

The frontend electronics and their integration procedure for the ME0 system are still in their infancy, but are similar to the GE2/1 detector system. This system features a GEB and plugin cards with VFAT3 ASICs. The role of the OH in the GE2/1 system is performed by the ASIC and Gigabit Optics (ASIAGO), which contains Low Power Gigabit Transfer ASICs, and transmits data via a Versatile Link PLUS to the backend. Power is provided by bPOL DC-DC converters. At the time of writing, only basic functionality tests are implemented for the ASIAGO, which are currently conducted through an adapter board, known as the Prototype Interface Mezzanine (PIZZA) mounted on a GE2/1 module's GEB.

Systems, Planning, Installation, Commissioning and Running Experience / 89

The CMS HGCAL Silicon Region Architecture Specification and Optimisation

Author: Matthew Noy[1]

[1] *CERN*

Corresponding Author: matthew.noy@cern.ch

An overview of the electronics readout/trigger architecture for the CMS HGCAL will be given. To respond to physics performance requirements, data rates, trigger-primitive generation and radiation tolerance has been extremely challenging. Each HGCAL endcap includes ~300m² of active silicon in 50 layers, with a largely inhomogenous layout with limited commonality between layers. An agile, python-based counting scheme was implemented that creates tables of component counts. These are subsequently incorporated in the architecture specifications document and costbook, providing critical input to the mechanical design and integration optimisation.

Summary (500 words):

The CMS High Granularity CALorimeter (HGCAL) project is in the process of designing two identical endcaps to be installed as part of the phase 2 upgrades of the CMS detector. The architecture is based on a sampling calorimeter with 50 active layers. These are instrumented with silicon diode pads in the electromagnetic region (CE-E), which runs from layers 1-28 inclusive, and a mixture of silicon and plastic scintillator tiles instrumented with on-tile SiPMs in the hadronic region: layers 29-50 (CE-H). There are two diode pad size variants and 3 doping layer thicknesses. The absorber is a mixture of lead, copper, tungsten and steel giving a total weight of nearly 250 tonnes per end-cap. The requirements are legion and impose demanding and sometimes conflicting constraints on the design of the read-out electronics. These include, but are not limited to: an intense and non-uniform radiation environment; highly non-uniform data rates: very high at high η to moderate at low η; Trigger Primitive Generation; tightly limited Z space; 10s of ps (RMS) shower time resolution; and a detector envelope that varies with Z and hence layer. The baseline architecture that attempts to respond to as many of these as possible is somewhat inhomegeneous. A description will be given along with the main motivations for some of the key design choices that attempt to simplify this architecture by concentrating some of the complexity into key components with the goal of reducing the design effort required, as well as the production testing by reducing the number of complex variants. Despite this focus, a large number of variants exists in the baseline design. A software tool was written in python that reads the architecture description and, running through all these variants, produces component count tables that feed into the project cost book and part provisioning. Additional outputs are also programmed in that facilitate the mechanical design and integration, power cable and read-out fibre routing and channel mapping. The ethos behind this approach is to be able to more easily understand the importance and consequences of changes in the baseline architecture during the detector optimisation phase.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 90

ZynqMP-based board-management mezzanines for Serenity ATCA-blades

Authors: Torben Mehner[1]; Luis Ardila[2]; Matthias Norbert Balzer[1]; Oliver Sander[1]; Denis Tcherniakhovski[3]; Michael Schleicher[1]; Giacomo Fedi[4]; George Gimas[4]; Gregory Michiel Iles[4]; Mark Pesaresi[5]; Duncan Parker[4]; Andrew William Rose[4]; Thomas Schuh[6]

[1] *KIT - Karlsruhe Institute of Technology (DE)*

[2] *KIT-IPE*

[3] *Karlsruhe Institute óf Technology*

[4] *Imperial College (GB)*

[5] *Imperial College*

[6] *Rutherford Appleton Laboratory (GB)*

Corresponding Authors: torben.mehner@kit.edu, luis.ardila@kit.edu

In the context of the CMS Phase-2 tracker back-end processing system, two mezzanines based on the Zynq Ultrascale+ Multi-Processor System-on-Chip (MPSoC) device have been developed to serve as centralized slow control and board management solution for the Serenity-family ATCA blades.

In this talk, we present the current revision of both Serenity baseboards and the developments on the MPSoC mezzanines to execute the Intelligent Platform Management Controller (IPMC) software in the real-time capable processors of the MPSoC. In coordination with the Shelf Manager, once full-power is enabled, a CentOS-based Linux distribution is executed in the application processors of the MPSoC.

Summary (500 words):

In the context of the CMS Phase-2 tracker back-end processing system, two mezzanines based on the Zynq Ultrascale+ Multi-Processor System-on-Chip (MPSoC) device have been developed to serve as centralized slow control and board management solution for the Serenity-family ATCA blades.

The Serenity family consists of two ATCA-sized boards designed to explore alternative configurations. Serenity-A is designed around a single Virtex US+ FPGA with up to 128 high-speed transceivers, each with a line rate of up to 25 Gb/s. 120 high-speed lanes are connected to Samtec Firefly optical transceivers; four are used for the DAQ path, one is used for the CMS timing and clock distribution (TCDS), and the remaining links for slow-control and management tasks provided by the MPSoC mezzanine in the "FMC+" format.

Serenity-Z contains two sites that utilize Samtec z-ray interposer technology mounting removable FPGA-based daughter cards. Each site is connected to 18 Samtec Firefly optical transceiver sites. All of them can take the form of x4 or x12 (16 Gb/s or 25 Gb/s) depending on the daughter card used. The choice of slow-control and board management is as well flexible between the combination of a com-express (CMX) Computer-on-Module (CoM), a DIMM-based IPMC, or an integrated MPSoC mezzanine in the "CMX-Extended" format.

In this talk, we present the current revision of both Serenity baseboards and the developments on the MPSoC mezzanines to execute the Intelligent Platform Management Controller (IPMC) software in the real-time capable processors of the MPSoC. In coordination with the Shelf Manager, once full-power is enabled, a CentOS-based Linux distribution is executed in the application processors of the MPSoC.

Trigger / **91**

A CMS Level-1 Track Finder for the HL-LHC

Author: Brian Lee Winer[1]

[1] *Ohio State University (US)*

Corresponding Authors: yates.313@osu.edu, brian.winer@cern.ch

The High-Luminosity LHC will put significant demands on trigger systems. To control trigger thresholds, the CMS Collaboration is designing a novel Level-1 track trigger. The Outer Tracker will use modules with pairs of sensor layers to read out hits compatible with charged particles above 2-3 GeV. The system will combine these front-end trigger primitives to reconstruct tracks, providing a measurement of P_T, \eta , \phi, and z_0. This presentation will introduce the CMS L1 track finding system: the algorithm and its estimated performance, hardware prototypes, and the unique challenges associated with this system.

Summary (500 words):

The High-Luminosity Large Hadron Collider (HL-HLC) expects to become operational later this decade and deliver an instantaneous luminosity of approximately 7.5 x 1034 cm-2 s-1. This luminosity will create an average of 200 proton-proton collisions for each bunch crossing of the beams. This creates a very busy environment that is challenging for the trigger and data acquisition systems of the collider experiments. To explore the physics topics of interest, such as further study of the Higgs boson, the trigger thresholds need to be kept as low as possible. However, trigger rates must also be controlled and new approaches need to be developed. One method for controlling trigger rates is using charged track reconstruction at the earliest possible stage of the trigger decision. The CMS Collaboration is designing a Level-1 Track Finder (L1TF) for the trigger system in the HL-LHC era.

The L1TF will use trigger primitives from the CMS Outer Tracker, a silicon-based detector being developed for the HL-LHC. The trigger primitives are "stubs", which are pairs of hits in closely space silicon sensors. These stubs will be required to be consistent with those created by charged particles with PT > 2 GeV. As the charge particles traverse the tracking volume, a 3.8T magnetic field will bend the charged particles into a helical path. Reconstructing that path and measuring the curvature allows a measurement of the particle's momentum transverse to the beamline. Performing tracking is a massive pattern recognition problem and there are many challenges involved in achieving this within a trigger system: a large input data rate of about 20–40 Tb/s; processing a new batch of input data every 25 ns, each consisting of about 15,000 stubs with precise position measurements and rough transverse momentum measurements of particles; performing the pattern recognition on these stubs to find the trajectories; and fitting the trajectories to determine optimal trajectory parameters (P_T, \eta , \phi, and z_0) to produce the list of tracks all within 4 microseconds.

The L1TF will be built on an FPGA architecture using Xilinx Virtex® UltraScale+TM FPGA technology and using a custom-designed Track Finding card. The algorithm within the FPGA is pipelined into ten distinct processing steps with intermediate results being stored in internal memories. The processing steps are being implemented in HLS within Vivado. The presentation will discuss each stage of the processing and the expected performance of the algorithm. The presentation will also discuss Monte Carlo studies that have shown that we expect to achieve a PT resolution of ~1%, a zo resolution of ~2mm, and an efficiency above 95%. The timeline for further development leading up to installation will be briefly described. This system represents the most ambitious track trigger ever attempted in particle physics.

Posters Power, Grounding and Shielding / **92**

Smart Switch based High Voltage Distribution System for Mu2e Electron Tracker

Author: Waqar Ahmed[1]

Co-authors: Ed.V Hungerford [1]; Aseet MukherJee [2]; L.Vadim Rusu [3]

[1] *University of Houston*

[2] *Fermilab*

[3] *Fermilab*

Corresponding Author: waqar.ahmed@cern.ch

The design and development of a High Voltage distribution system (HVDS), Smart Switch (SS) which acts as a Demultiplexer, to distribute one high voltage(HV) input into six High Voltage output channels. It provides, and independently voltage and current monitors. Each output channel of the SS has independent, ON-OFF, current and HV monitoring, as well as filtration, isolation, and a crowbar for over-current protection. The inter-communication system is based on TCP/IP protocol through a Raspberry Pi. The performance of the HVDS was found to be comparable to commercial High Voltage Power supplies.

Summary (500 words):

The descriptions of the HVDS, are summarized below. The Electron Tracker (ETD) consists of eighteen stations with each station containing 1152 straw detectors. stations has 2 planes and each plane has six panels of 96 straw detectors. Each plane has independent HV input, control, filtration, and crowbar systems. The high voltage power supplies have active, over-voltage protection for each plane. A ground reference for the HV-power return is established at the panel by a connection to the station ground. There is a supply and return cable for each panel, and power connections are made through vacuum penetrations which are isolated electrically from the supporting structure.
Ground loops are eliminated by using isolated power supply outputs. Each plane has independent HV input, control, filtration, and crowbar systems. Safety ground is provided by station ground connections. To minimize delay and provide a fast crowbar trip, the detector HVDS is placed near the stations. A straw drift field voltage of 1.45 to 1.5 kV, with a maximum, supplied current of 250μA (beam on target) is provided. The accuracy of a voltage is approximately 0.1V The current readout is better than 15 bits (10 nA @ 250μA max). There are four connections to the HVMB; A low voltage output and ground and two outputs to interface with an Arduino board. Each panel has independent HV input, and a filtration and crowbar system. The high voltage power supplies have active, over-voltage protection to each unit when an abnormal fault is sensed. A ground reference for the HV-power return is established at the panel by a connection to the station ground. There is a supply and return cable for each panel, and power connections are made through= vacuum penetrations which are isolated electrically from the supporting structure. Ground loops are eliminated by using isolated power supply outputs. Safety ground in this design is provided by station ground connections. To minimize delay and provide a fast crowbar trip, the detector HVDS is placed near the stations. A straw drift field voltage of 1.45 to 1.5 kV, with a maximum, supplied current of 250uA. A (beam on target) is provided. The accuracy of the voltages is approximately 0.1V and the current readout is better than 15 bits (10 nA @ 250uA). The new High Voltage Mother Board (HVMB) has 12 daughter boards. There are six Smart Switches for each panel, one HVMB for each station. For testing of the SS, we develop HVMB contains six SS boards with the crowbar circuit. It is a small board, “2 x 4”, and has the capability of ON-OFF for individual channels, HV/LV isolation up to 2 KV, filtration, and panel protection if the discharge occurs in a panel. The size of all the SS boards is identical. Each SS has two ADCs one is a voltage monitor using a voltage divider (1000 to 1) and the other a current monitor using a shunt from an isolation amplifier.

Posters Production, Testing and Reliability / 93

Test system for the Service Hybrid of the 2S Module for the CMS Phase-2 Outer Tracker Upgrade

Authors: Alexander Josef Pauls[1]; Christian Dziwok[2]; Daniel Louis[3]; Irfan Özen[4]; Katja Klein[3]; Lutz Feld[5]; Martin Lipinski[1]; Michael Wlochal[None]; Oliver Pooth[3]; Waclaw Karpinski[None]

[1] *RWTH Aachen University (DE)*

[2] *RWTH Aachen*

[3] *Rheinisch Westfaelische Tech. Hoch. (DE)*

[4] *RWTH Aachen University, Aachen, Germany*

[5] *RWTH Aachen University*

Corresponding Author: alexander.pauls@rwth-aachen.de

In the context of the second phase of the CMS Outer Tracker upgrade two complementary systems for the testing of the service hybrids for two-sided silicon strip modules are presented. To enable prototype testing and long term active thermal cycling during series production a dedicated test board for stand-alone operation has been produced. In addition, a test card compatible with a production scale system has been developed. It is embedded in a common test system for all CMS-OT hybrids. The test systems will be introduced and first test results with both systems on prototype 2S service hybrids will be presented.

Summary (500 words):

During the LHC Long Shutdown 3 the CMS experiment's silicon tracker will be replaced to cope with the increase in instantaneous luminosity and radiation exposure. A key feature of the new tracker are modules with two closely spaced silicon sensors. By correlating hits in both sensor planes the transverse momentum of charged particles can be estimated at module level. Track information of tracks with transverse momentum above an adjustable threshold will be forwarded at the bunch crossing frequency of 40MHz to the Level 1 trigger. This enables the experiment's Level 1 trigger to utilize tracking information. The so-called 2S module type features two 10x10cm^2 sensors with two rows of 1016 strips at 90µm pitch on each sensor. Each 2S module is equipped with two front-end hybrids, which perform the readout. Their data output consists of six 320Mbit/s electrical links. The links are serialized on the service hybrid by the lpGBT to a 5.12Gbit/s stream and optically transferred to the back-end via the VTRx+. Trigger and configuration data are transferred in the opposite direction via an additional electrical link per side. The service hybrid also hosts two DC/DC converters to provide 1.25V and 2.5V for the module operation from the input voltage of about 10V. In addition, it filters the sensor bias voltage and supplies it to the sensors. With roughly 7600 2S modules needed for the new tracker, testing all objects before module assembly is a vital aspect of the upgrade effort. Two systems centered around different PCBs were developed to achieve this goal. The test board features two GBTx serializer ASICs and VTRx optical transceivers to provide electrical links to the service hybrid and emulate front-end hybrid data. All three optical links are connected to a FC7 data acquisition board, which provides and verifies the data streams. The test board's Cyclone 3 FPGA is capable to scrutinize the clock and reset signals distributed by the lpGBT. Functionalities that target the testing of DC/DC converter functionalities and the bias voltage distribution as well as the FPGA are controlled by a RaspberryPi single-board computer. Extension cables allow the use of the test board with a cooling setup. Hybrids can be temperature-cycled between -35℃ and room temperature during operation and testing. Direct cooling allows for fast cycling and a defined hybrid temperature. In addition to the test board, that targeted prototype and in-depth testing of small numbers, a test card for production scale testing was developed. It is compatible with a multiplexer backplane that is common for all hybrid types of the Outer Tracker upgrade. Instead of the RaspberryPi a USB-controlled micro-controller is used. The FC7 is electrically connected to the plug-in card so the need for the additional optical links is removed. Temperature cycling is realized by placing the setup inside a climatic chamber. Both, test board and test card, have been produced and tested alongside the cooling setup and service hybrid prototypes. Their concepts will be described and compared, and measurements on final prototype 2S service hybrids will be presented.

Systems, Planning, Installation, Commissioning and Running Experience / **95**

Readout electronics for the CMS Phase II Endcap Calorimeter: system overview and prototyping experience

Author: Nadja Strobbe[1]

[1] *University of Minnesota (US)*

Corresponding Author: nadja.strobbe@cern.ch

The frontend readout system for the silicon section of the CMS Phase II Endcap Calorimeter faces unique challenges due to the high channel count and associated bandwidth, limited physical space, as well as radiation tolerance requirements. This presentation will give an overview of the frontend electronics design and will discuss the recent experience obtained from the first test system that integrates the HGCROC2 readout ASIC, lpGBT, and VTRX+ in a realistic manner, linking together prototypes of the hexaboard, engine board, and wagon board.

Summary (500 words):

The CMS endcap calorimeters will be fully replaced as part of the Phase II upgrade. The upgraded detector (known as HGCAL) will be a sampling calorimeter featuring integrated electromagnetic and hadronic sections, with layers of hexagonal silicon sensors in the highest radiation areas and plastic scintillator tiles where radiation is lower. The detector will also be highly granular, with more than 6 million readout channels. The frontend electronics for the silicon section are separated into several physical boards. The "hexaboard" holds the HGCROC ASIC, which measures and digitizes the charge deposited in the silicon sensors, and provides a precise measurement of the time of arrival. The data are then transmitted to the concentrator ASICs via 1.28 Gbps serial links for either trigger primitive generation or data acquisition. From here the compressed data are then forwarded, still via 1.28 Gbps links, to the lpGBT, which is hosted on the "engine" boards. There, the data are serialized and sent to the off-detector readout via 10.24 Gbps links through the VTRX+. Each engine board is connected to up to 6 hexaboards via the "wagon" boards. The precise mapping is nontrivial, since each layer in the detector is different, and occupancies vary strongly both within and between layers. As a result, wagon boards come in many varieties. These electronics must all be able to withstand the radiation levels present in the detector. The ASICs are designed to handle the 1x10^16 neq/cm2 present in the inner parts of the detector. However, the VTRX+ and the bpol12V DC/DC converters used for powering, cannot withstand this level and must be placed at larger radius. An additional challenge to the electronics design is the limited physical space along the z-direction. The engine and wagon boards, along with the DC/DC board, must all fit within a 5mm wide gap between the hexaboard and the cover plate, which places constraints on board thickness, connector stacking heights, and inductor coil dimensions. This presentation will cover the recent progress made for these frontend readout electronics. A first test system has been produced that links together an engine with two wagons and five hexaboards, using an FPGA-based emulation of the concentrator ASIC and a ZCU102 as backend system. We will discuss our experience establishing full system communication and will report on signal integrity studies.

Radiation Tolerant Components and Systems / 96

Single Event Effects on the RD53B Pixel Chip Digital Logic and On-chip CDR

Author: Jelena Lalic[1]

Co-authors: Pierre Barrillon [2]; Jorgen Christiansen [1]; Leyre Flores Sanz De Acedo [3]; Denis Fougeron [2]; Eva Renee Anna Joly [4]; Esben Rueskov Madsen [5]; Mohsine Menouni [4]; Piotr Rymaszewski [6]; Mark Standke [6]; Thomas Strebler [7]

[1] *CERN*

[2] *Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France*

[3] *University of Glasgow (GB)*

[4] *Centre National de la Recherche Scientifique (FR)*

[5] *University of Southern Denmark (DK)*

[6] *University of Bonn (DE)*

[7] *CPPM, Aix-Marseille Université, CNRS/IN2P3 (FR)*

Corresponding Author: jelena.lalic@cern.ch

The RD53B chip for HL-LHC upgrades of ATLAS and CMS needs to provide reliable operation in a radiation hostile environment with inevitable Single Event Effects. To answer the challenge, substantial efforts are made to protect and evaluate the critical parts of digital logic with different TMR schemes and to characterize the on-chip CDR. Cross-section for each TMR scheme and its effective SEE sensitivity are measured in several SEE campaigns. The on-chip CDR is characterized by measuring the SEE-induced phase shifts of its output clocks and their implication on the high-speed link stability. Results from these campaigns will be presented.

Summary (500 words):

The RD53B chip is designed with the goal of having a high tolerance for Single Event Effects (SEE). In order to gain an increased immunity for SEEs, critical parts of the digital logic such as chip configuration registers and pixel configuration bits are designed with TMR protection. As a trade-off between area, power consumption and SEE immunity, global configuration registers are protected by TMR protection with auto-correction, while pixel configuration registers lack the auto-correction in their TMR protection scheme.
Measured cross-sections in two SEE campaigns at CRC, Louvain la Neuve, show that adding a triplication scheme with a voter and with no auto-correction to the single latch will decrease its effective SEE sensitivity one to two orders of magnitude, depending on the ion LET. By adding auto-correction to this protection scheme, one more order of magnitude decrease is achieved. The measurements with a 480 MeV proton beam in TRIUMF, Canada, showed that gain achieved with no auto-correction inside TMR scheme is 100, and adding auto-correction will increase this gain to 400. During these campaigns, it has been observed that the 1.28Gbit/s link can lose its synchronization which has led to lost or corrupted data events. However, this behavior was not seen when the required clocks are provided externally by bypassing the on-chip CDR. Motivated by this, a dedicated CDR testing campaign was done in GANIL, France. The goal was to characterize SEE-induced phase shifts in the CDR clocks and their implications on the corrupted data events and overall high-speed link stability. For such a test, two setups were used in parallel. The first one was an oscilloscope triggered on the serializer clock phase shift larger than 400ps in respect to the stable clock reference. The second setup was based on a 10.24Gbit/s clock oversampler inside the FPGA, reaching the resolution of 97ps. All SEE-induced events captured by these 2 setups can be classified into several categories, depending on the behavior of the clock's phase, frequency, biasing, and amplitude. The different nature of captured events points to different chip parts being sensitive to SEEs, such as different blocks of the CDR itself, the LVDS receiver, and the CML driver.
These results, conclusions and setup descriptions are relevant for radiation tolerant systems, general testing and system reliability, as well as an important step in preparing for a stable operation of detectors in HL-LHC.

ASIC / 97

Detection Performance of MIMOSIS-1, a CMOS Sensor Prototype Developed for the CBM-MVD

Author: Roma BUGIEL[1]

Co-authors: Abdelkader Himmi [1]; Andrei Dorokhov [1]; Auguste Besson [1]; Benedict Arnoldi-Meadows [2]; Christian Müntz [2]; Christine Hu-Guo [1]; Claude Colledani [1]; Frédéric Morel [1]; Gilles Claus [1]; Gregory Bertolone [1]; Guy Dozière [1]; Hasan Darwish [3]; Hung Pham [1]; Isabelle Valin [1]; Jan Michel [2]; Joachim Stroth [4]; Jérôme Baudot [1]; Kimmo Jaaskelainen [1]; Marc Winter [5]; Mathieu Goffe [1]; Matthieu Specht [1]; Michael Deveaux [6]; Michal Koziel [2]; Philipp Klaus [2]; Yue Zhao [1]; Ziad El Bitar [1]

[1] *IPHC*

[2] *IKF*

[3] *IKF and IPHC*

[4] *IKF, GSI and HFHF*

[5] *IPHC and IJCLab*

[6] *GSI*

Corresponding Author: roma.bugiel@iphc.cnrs.fr

The Micro-Vertex Detector of the CBM experiment at FAIR/GSI requires very light detector stations equipped with highly granular and thin pixel sensors adapted to hostile running conditions. A specific CMOS pixel sensor, called MIMOSIS, is being developed for this purpose. Inspired by the ALPIDE sensor equipping the ALICE ITS, its design is adapted to higher hit rate and radiation tolerance. The first full scale prototype was fabricated in 2020 with several epitaxial layer variants. The chips were assembled in a beam telescope which was operated at DESY. First results of the signal-to-noise and detection performance evaluations will be presented.

Summary (500 words):

MIMOSIS-1, the first full size pixel sensor prototype developed for the CBM-MVD (FAIR/GSI) was fabricated in 2020 in a 180 nm CMOS imager technology with a 25 μm thick epitaxial layer featuring a resistivity exceeding 1 kΩ·cm. The layer was declined in 6 different doping profiles to enhance its depletion depth and, consequently, the sensor radiation tolerance and charge collection speed.
MIMOSIS-1 features 1024 columns of 504 pixels (27 x 30 μm² wide). Its dimensions (31 x 17 mm²) are those of the final sensor, to be produced in 2023. Fig.1 displays a photograph of a diced sensor. Each pixel includes a pre-amplifier connected to the sensing node and to a shaping and discrimination circuit with tuneable threshold. The depletion of the epitaxial layer is obtained either from usual back bias or from the sensing node, possibly connected to a voltage source. The signal of each hit pixel comes down to its logical address, combined with a time stamp expressing a 5 μs frame read-out time. The pixel read-out proceeds through a data driven architecture similar to the one of the ALPIDE sensor equipping the ALICE-ITS. It is connected to a data processing micro-circuit integrated on the sensor edge, which prefigures the sparse data scan circuitry and elastic buffer to be integrated on the final sensor, suited to deliver up to 2.4 Gbits/s of data. More details may be found in [1, 2].
MIMOSIS-1 incorporates 4 different variants of in-pixel circuitry, each populating a different sub-array. Two sub-arrays host pixels where the sensing node is DC-coupled to the pre-amplifier. The two others feature pixels where the node is connected through a capacitor to the pre-amplification and shaping circuitry. In the latter case, called AC-coupled, the voltage source connected to the sensing diode is decoupled from the in-pixel signal processing circuitry, which allows to raise the diode input voltage to several tens of volts, and thereby extend the depleted volume [2].
For each sub-array, the pixel temporal noise (TN) and the dispersion of the discriminator thresholds (FPN) were estimated on several tens of sensors in the laboratory. The study was performed for 3, out of the 6, different epitaxial layers. The TN and FPN values were derived from a "threshold scan", where the charge injection of all pixels composing a sub-array was repeated while increasing step by step the discriminator thresholds. Most TN and FPN values were found in the ranges 3-5 and 8-15 e- ENC, respectively (see Fig.2).
A two-arm beam telescope was constructed with 4 sensors thinned to 60 μm, complemented with 2 sensors placed in between both arms for a first detection performance evaluation. The talk will present the detection performance observed with particle beams for the 4 different pixel designs and 3 different substrates, as a function of discrimination threshold and depletion voltage.
References:
[1] M. Deveaux et al., "Observations on MIMOSIS-0, the first ...", arXiv : 1909.05614v1
[2] F. Morel, "The MIMOSIS-1 sensor ...", talk pres. at the TIPP workshop (24-28 May 2021)

Posters Programmable Logic, Design Tools and Methods / 98

Easy and structured approach for software and firmware co-simulation for bus centric designs

Author: Michal Kruszewski[1]

[1] *Warsaw University of Technology*

Corresponding Author: michal.kruszewski.dokt@pw.edu.pl

Although software and firmware co-simulation is gaining popularity, it is still not widely used in the FPGA designs.
This work presents easy and structured approach for software and firmware co-simulation for bus centric designs.
The proposed approach is very modular and software language agnostic.
The only requirement is that the firmware design is accessible via some kind of bus.
The concept has been used for testing DAQ system being developed for high energy physics experiment.

Summary (500 words):

Software and firmware co-simulation can save a lot of time and money, as it leads to lower number of HDL project builds and reduces the number of test iterations with the real hardware.
Despite its obvious advantages the co-simulation is still rather rare to see in FPGA designs.
There are at least four reasons for such situation.

The first one is that setting up a co-simulation framework requires knowledge on multiple computing areas.
The second one is that it might be time consuming.
The third one is that ready to use frameworks sometimes do not support some of the desired HDL features, for example handling compound types such as records or arrays.
The fourth one is that ready to use frameworks are strictly coupled with a single programming language.
This work presents modular approach and tries to be inline with the Unix philosophy.
The framework blocks are loosely coupled and each of them can be easily replaced.
The co-simulation framework consists of the following elements: software co-simulation interface, HDL co-simulation interface, HDL BFM (Bus Functional Model), test runner.
The whole test bench additionally consists of the projects software and firmware code.
The co-simulation interfaces are relatively simple and short, and once written they can be reused for different tests within the project.
If different software languages are used for the prototype and target implementation phases it is also easy to write a co-simulation interface for the new language and reuse the co-simulation framework from the prototyping phase.
The BFM can be custom or taken from a library such as UVVM.
The idea is based on the assumption, that all communication is done via the bus.
Not only the regular data is transferred via the bus, but also the test bench specific data.
Such approach is immune to lack of support for compound types.
The proposed approach is not free of drawbacks.
The first one is that the firmware design must have some kind of bus.
This should not be a problem as almost all complex FPGA designs have some kind of bus, Wishbone and AXI being probably the most popular.
The second one is that doing precise timing checking between signals is hard to achieve solely within test bench software.
It requires firmware checker accessible via the bus.
Another approach is using PSL (Property Specification Language) or SVA (SystemVerilog Assertions).
The proposed approach has been used for testing of DAQ (Data Acquisition) system for the CBM (Compressed Baryonic Matter) experiment that is being prepared at FAIR (Facility for Antiproton and Ion Research) in Darmstadt.

Systems, Planning, Installation, Commissioning and Running Experience / 99

The Apollo ATCA design for CMS Track Finder and Pixel Readout at the HL-LHC

Author: Rui Zou[1]

[1] *Cornell University (US)*

Corresponding Author: rui.zou@cern.ch

The challenging conditions of High-Luminosity LHC (HL-LHC) require tailored hardware designs for the trigger and data acquisition systems. The Apollo platform features a “Service Module” (SM) with a powerful system-on-module (SoM) computer that provides standard ATCA communications and application-specific “Command Module”s (CM) with large FPGAs and high speed optical fiber links. The CMS design of Apollo will be used for Track Finder and pixel readout. It features up to two large FPGAs and 100+ optical links with speed up to 25 Gbps. This presentation will give updates on the design and show link quality results and power and thermal performance.

Summary (500 words):

High-performance ATCA blades are gaining popularity among high-energy physics experiments in view of the High-Luminosity LHC. The development for high-energy physics applications has proven to be challenging with many problems that need to be addressed (power, cooling, optical fiber management, communication interfaces and etc.). The APOLLO platform aims to provide a simple hardware environment and firmware and software toolkit which can be used for the development of ATCA blades. It consists of a common “Service Module” that handles standard ATCA communications as well as clock

and power delivering and an application-specific "Command Module" (CM) with large FPGAs and many optical links to accommodate demanding algorithms and large data flow.

The Apollo Service Module is a standard-sized ATCA blade with a 7U x 180 mm cutout to accommodate one Command Module board. It contains standard ATCA power, communication and control infrastructure. It features a Xilinx Zynq System-on-Module (SoM) with embedded Linux OS for control, monitoring and local DAQ functions, a CERN IPMC or OpenIPMC and a Wisconsin ESM Ethernet switch. Standard commercial power entry and conditioning modules are used to deliver 12VDC at up to 30A to the Command Module.

In the CMS experiment, the Apollo platform will be used for the Level-1 Track Finding (TF) system and the Inner Tracker Data Trigger and Control system (IT-DTC). Level-1 TF reconstructs tracks from the Outer Tracker and calculate track parameters for the Level-1 trigger system. IT DTC reads from the Front-End ASIC chips and converts data into compact format. These two applications together require substantial FPGA resources, possible large power consumption and large number of optical links. The CMS design of the Apollo Command Module has the ability to accommodate one or two large Xilinx Ultrascale+ FPGAs with 4 channel bi-directional and 12 channel single-directional Firefly optical engines that sum up to 100+ optical links with speed up to 25 Gbps. We study carefully the design and performance of the board by using customized firmware to test power consumption, heat dissipation under CMS constraints and optical link integrity. This talk will discuss the results of these performance tests, design updates and future plans.

Posters ASIC / 100

Certification of the amplifier-shaper-discriminator ASICs produced for the ATLAS MDT chambers at the HL-LHC

Authors: Sergey Abovyan[1]; Varuzhan Danielyan[1]; Andreas Grasser[2]; Oliver Kortner[1]; Hubert Kroha[1]; Robert Richter[1]; Simeon Simeonov[2]

[1] *Max-Planck-Institut fur Physik (DE)*

[2] *Max-Planck-Institut für Physik*

Corresponding Author: kortner@mppmu.mpg.de

The front-end electronics of the ATLAS muon drift-tube chambers will be upgraded in the experiment's phase-II upgrade to comply with the new trigger and read-out scheme at the HL-LHC. A new amplifier shaper discriminator chip was developed in 130 nm Global Foundries technology for this upgrade. A preproduction of 7500 chips was launched in 2019 and tested in 2020. The functionality of the chips, the test set-up and test procedure and results showing a yield of 92% are presented. The certification of the preproduction was followed by the production of 80,000 chips in fall 2020 showing 92% yield.

Summary (500 words):

The upgrade of the front-end electronics of the ATLAS muon drift tube (MDT) chambers is part of the phase-II upgrade of the ATLAS detector for HL-LHC. The present amplifier shaper discriminator (ASD) chip for the MDT chambers was designed in Agilent 500~nm technology which has become obsolete. For the upgrade a new ASD chip was designed in Global Foundries 130~nm CMOS technology. The design of the new chip follows the design of the present chip, but incorporates a fix of a specific design error of the present chip in the output logic. he chip has a differential charge sensitive preamplifier, bipolar shaping with ion tail cancellation and a Wilkinson ASD for time-walk corrections to the discriminated signals. Each channel is connected to a discriminator providing LVDS output signals. A discriminator threshold common to all the channels can be programmed and generated inside the chip. A preproduction of 7500 chips was launched in 2019 and tested in 2020. The tests were carried out manually using a test board provide by the ATLAS muon group of the Ludwig-Maximilians University of Munich.

The chip tests proceed along the following steps:
* Reject chips which cannot be powered up or cannot be put into operation;

* Reject chips which draw abnormal currents;
* Reject chips with channels that have wrong output LVDS levels;
* Reject chips with dead channels;
* Reject chips with two large thresholds spreads;
* Reject chips with abnormal ADC counts for an input charge of -20~fC.

For the last three tests in the list above pulses with predefined charges are injected to the eight channels of the chip one after the other.

More than 91% of the tested chips pass all criteria. 0.07% of the chips cannot be put into operation. 0.22% chips have bad LVDS output levels. 0.07% of the chips have too low total currents. 1.87% of the chips have dead channels. 1.87% show too large threshold spreads and 4.02% give bad ADC values.

The same very high yield as for the preproduction was found for a sample of 1000 production chips. The remaining 79,000 ASD chips will be tested by a company in a automated procedure.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 101

A Generic Streaming Data Acquisition System for High-energy Physics Experiments

Authors: Tianxing Wang[1]; Junfeng Yang[1]

[1] *University of Science and Technology of China*

Corresponding Author: tx951121@mail.ustc.edu.cn

The data acquisition system is a vital component in the high-energy physics experiment. To reduce duplication of work during development, D-Matrix, a generic platform, has been developed as a unified software/hardware streaming DAQ system and will be used in CSR External-target Experiments in HIRFL-CSR. Its philosophy is to abstract different tasks in the stream processing and encapsulate them as reusable modules with standard inter-module connectors. Furthermore, D-Matrix builds a unified model to integrate software and hardware design so that the system can be built from a global view. This paper presents the architecture of the D-Matrix DAQ.

Summary (500 words):

The architecture of D-Matrix is based on stream processing. It decouples and abstracts the basic processing tasks in the stream processing and presents them as independent modules in both software and hardware form so that users could switch processing platforms anywhere. Furthermore, standard inter-module interfaces and inter-platform plug-in transceivers make it possible to connect modules and platforms arbitrarily so that a customizable processing structure can easily be built. At the same time, D-Matrix describes the spatio-temporal characteristics and superior-subordinate relationship of streams in different processing stages to ease data processing and reconstruction inside modules. The underlying design of D-Matrix is split into three layers as shown in Fig. 1:
1.Source Layer
In the source layer, the majority of data are born as continuous streams and vary in the topic (Stream ID). Each stream will be loaded into a unified data container (see Fig.2 and Fig.3) which is the basis of a unified transmission and processing model. Furthermore, the concept of “Data Domain” is introduced to describe the spatio-temporal characteristics and superior-subordinate relationship in different processing stages of the stream. Developers register all streams before the system runs and provide their “Data Domain Table” which contains the attributes of streams in different domains. These “Data Domain Tables” are applied to the modules in the corresponding “Data Domain” so that the modules can correctly deal with diverse streams in different processing stages.
2.Transport Layer
The transport layer is responsible for the stream transfer between modules and platforms. It is committed to provide a point-to-point transparent channel and reduce coupling between modules. The implementation of the transport layer consists of two parts.

(1)Transfer between platforms: This is conducted by transmitter and receiver(T&R), a unidirectional plug-in module (see Fig.4). By simply replacing the plugs, T&R can send and receive data from the different underlying hardware.
(2)Transfer between modules: "Dual shared memory space" and message queues are used for data transmission between modules in a software platform (see Fig.5). As for the firmware, a customized interface based on AXI4-Stream is developed.
3. Processing Layer
Data processing in physics experiments can be divided into more specific tasks such as stream distribution and aggression(see Fig.6), event building, slow control system(see Fig.7), and data storage which could be implemented as modules to facilitate development.
In particular, the event builder is developed as a generic module which can be configured in multiple dimensions such as the event scope(see Fig.8), the combination granularity(see Fig.9), the cluster size (see Fig.10), and the trigger mode.

In conclusion, D-Matrix has been designed to provide a flexible, scalable, and efficient architecture. More general-purpose modules are in progress. Besides CEE mentioned above, D-Matrix is also used in a deep-sea geological exploration experiment and planned to be used in a neutrino-less double beta decay experiment.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 102

A precision Time of Flight measurement system for the TORCH prototype detector

Author: Rui Gao[1]

Co-authors: Christoph Frei [2]; David Cussans [3]; Didier Piedigrossi [2]; Emmy Pauline Maria Gabriel [4]; Flavia Cicala [5]; James Milnes [6]; Jonas Rademacker [3]; Maarten Van Dijk [7]; Michal Kreps [5]; Neville Harnew [1]; Nick Brook [8]; Roger Forty [2]; Srishti Bhasin [3]; Thierry Gys [2]; Thomas Blake [9]; Thomas Conneely [10]; Thomas Henry Hancock [1]; Timothy Gershon [5]; Tom Hadavizadeh [11]

[1] *University of Oxford (GB)*

[2] *CERN*

[3] *University of Bristol (GB)*

[4] *Nikhef National institute for subatomic physics (NL)*

[5] *University of Warwick (GB)*

[6] *Photek Ltd*

[7] *EPFL - Ecole Polytechnique Federale Lausanne (CH)*

[8] *University of Bath*

[9] *University of Warwick*

[10] *Photek LTD*

[11] *Monash University (AU)*

Corresponding Author: rui.gao@cern.ch

The TORCH detector provides low-momentum particle identification, combining Time of Flight (TOF) and Cherenkov techniques to achieve charged particle pi/K/p separation between 2-20 GeV/c over a flight distance of 10m. The measurement requires a timing resolution of 70ps for single Cherenkov photons. For precision photon detection, customised Micro-Channel Plate Photomultiplier Tubes (MCP-PMTs) with high precision TOF measurement electronics have been developed. The electronics measures time-over-threshold from the MCP-PMT and features a 10-Gigabit Ethernet readout. A 50ps MCP/electronics time resolution has been demonstrated. This paper reports the design and performance of the system with 5120 channels, instrumenting ten customised MCP-PMT devices.

Summary (500 words):

TORCH is being developed to identify B-meson decay products in the upgrade II of the LHCb experiment, but has wider applications in future particle physics experiments. The TOF measurement requires a timing resolution of 70ps for single Cherenkov photon, which translates to the electronics contributing 50ps time resolution or better.

The TORCH prototype uses ten MCP-PMTs detectors that are installed on the periphery of a 660x1250x10 mm3 quartz plate, in which Cherenkov photons are produced on the passage of a charged track. The photons propagate to the periphery of the plate by total internal reflection where they are focused onto the MCP-PMT detectors. Each MCP-PMT has an 8x64-granularity over a 53x53 mm2 area, and is instrumented with four NINO boards that have in total 16x32-channel NINO ASICs [1] for a Time-Over-Threshold (TOT) measurement. The TOT results are digitised with 8 circuit boards, each equipped with 2x32-channel High Performance Time to Digital Convertor ASICs (HPTDCs) [2]. The data are transferred to a computer by two customised readout boards using a Gigabit Ethernet interface, as shown in Figure 1.

During operations, a DAQ PC first initialises the system by configuring the HPTDCs and NINOs, then sets all HPTDCs to start measurement. The HPTDC measures the photon arrival time and TOT (as the pulse width) when a trigger is received. The data are packed into Ethernet packets and sent to the PC that is connected via an Ethernet switch. The switch can route up 24 Ethernet connections to the PC through a 10 Gbit/s uplink port with buffering and traffic control. The switch also distributes configure data and control instructions from the DAQ PC to designated readout boards using their unique MAC addresses. This scheme has replaced the previous round-robin style readout [3] to allow simultaneous readout of all HPTDC boards with intelligent buffering.

Such a system consisting of 40 NINO boards, 80 HPTDC boards, 20 readout boards and 20 back planes has been produced. The system has been integrated into the TORCH mechanical arrangement and the optical components, as shown in Figure 2. Two previous test-beam campaigns have been carried out utilising a pair of MCP-PMTs [4], and a test beam is planned with the fully instrumented system in 2022.

DC-DC convertor-based power supplies have been added to reduce the complexity of Low-Voltage cabling in the previous system [3], only a small amount of additional power dissipation is expected.

During beam tests at the CERN PS, a Trigger Logic Unit (TLU) is used to distribute triggers and clocks to the 20 readout boards. The TLU also synchronises TORCH with other systems, e.g. beam telescopes, Cherenkov counters. Two timing stations are also used both in front and behind TORCH to generate start and stop signals.

The next generation of electronics system based on the latest technology development such as PicoTDC [5], FastIC [6] and lpGBT [7] from CERN is being developed. This new development will improve the TORCH timing resolution, channel density, as well as integration with DAQ structures in the LHCb experiment.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 103

The Microstrip Silicon Detector (MSD) data acquisition system for the FOOT experiment

Authors: Keida Kanxheri[1]; Mattia Barbanera[2]; Giovanni Ambrosi[3]; Gianluigi Silvestre[3]; Silvia Biondi[4]; Riccardo Ridolfi[5]; Mauro Villa[4]; Damiano Aisa[6]; Mirco Caprai[7]; Maria Ionica[7]; Pisana Placidi[3]; Leonello Servoli[3]; The FOOT Collaboration[None]

[1] *INFN - National Institute for Nuclear Physics*

[2] *Universita & INFN Pisa (IT)*

[3] *Universita e INFN, Perugia (IT)*

[4] *Universita e INFN, Bologna (IT)*

[5] *INFN Bologna*

[6] *Universita e INFN (IT)*

[7] *Istituto Nazionale di Fisica Nucleare Perugia*

Corresponding Author: keida.kanxheri@pg.infn.it

The FOOT (FragmentatiOn Of Target) multi-detector experiment aims at improving the accuracy of oncological hadrontherapy for tumor treatment. It studies the nuclear fragmentation due to the interactions of charged particle beams with patient tissues. Among the several FOOT detectors, the silicon Microstrip Detector is part of the charged-ions-tracking magnetic spectrometer. Here we describe the MSD architecture and its data acquisition system whose task is to collect and digitize the detectors output, generating a data packet to be sent to the experiment's central acquisition. This data acquisition system is designed and tested to withstand the high trigger rate and detector's throughput.

Summary (500 words):

Charged Particle Therapy in deep-seated solid tumors permits better effectiveness in cell killing compared to conventional photon radiation due to the depth-dose profile of charged particles. However, there is still room for improvement as there are no precise experimental data to feed into the Treatment Planning Systems (TPS) to compute the delivered dose along the particles path due to the fragments generated by the nuclear interaction that occurs between the charged particles beam and patient tissues. To this purpose, a new experiment FOOT (FragmentatiOn Of Target) has been proposed. It will use the inverse kinematic approach to measure the double differential cross-section of nuclear fragmentation, hence it is composed of different detectors with the aim of being portable among ion beam accelerators and capable of multiple measurements of the kinematic quantities of the charged fragments over a 10° cone around the beam axis. In this work we present the architecture of the Micro Strip Detector (MSD), the last x-y silicon measurement station of the experiment, which is just after the magnetic volum, and has the task of evaluating the Linear Energy Transfer LET (dE/dx) and the nuclear fragments momentum. It consists of 3 layers, each composed of 2 planes of silicon detectors made by Hamamatsu Photonics in which 640 150-um-thick microstrips are oriented orthogonally (one plane of 640 strips for the x axis and another plane for the y axis) to provide space points (x,y,z) along nuclear fragment tracks. The microstrip detectors are hosted in custom printed circuit boards where the output analog signal is preamplified, shaped, sampled and held by several IDE1140, an application specific integrated circuit (ASIC) for the readout of silicon strip radiation detectors. The analog data from each pair of x-y planes are passed to 12-bit high speed, low power ADCs (AD7276) with throughput rates up to 3 MSPS hosted in custom boards (ADC boards). The digitized data from each x and y plane is then collected by a DE10-Nano board, a commercial system-on-chip with a hard processor and an FPGA to complete the final module detector readout chain (one DE10-Nano board for each x- y plane).
The MSD complete subsystem can receive and recognize the signals sent from the central trigger board and instructions sent from the experiment central DAQ system. It contains an adequate number of registers for configuration and monitoring, reads out the data from the detectors when an external trigger occurs, and sends the acquired data to the central DAQ system. For each event, a sequence of headers and footers is added for event recognition as well as for timing information.
The entire path of the data from the raw sensors of the MSD sub-detector system to the central DAQ is an innovative custom data acquisition system relatively small in size and easily portable, which permits over 2 kHz acquisition rate capable of following the characteristics of the beam without generating bottlenecks for the entire experiment and the efficient management of both detectors frontend control and generated data delivery.

Systems, Planning, Installation, Commissioning and Running Experience / 105

The Mu3e Detector

Authors: Luigi Vigani[1]; Thomas Rudzki[2]

[1] *Ruprecht Karls Universitaet Heidelberg (DE)*

[2] *University Heidelberg*

Corresponding Author: luigi.vigani@cern.ch

The Mu3e experiment searches for the lepton flavour violating decay μ⟶ eee with an ultimate aimed sensitivity of 1 event in 10^16 decays. This goal can only be achieved by reducing the material budget per tracking layer to X/X0 ≈ 0.1%. For this purpose, the vertex detector is based on HV-MAPS thinned to 50 μm. Also, the powering and data transmission is performed by means of kapton-aluminum HDIs, which serve as mechanical support as well. This talk will show the detector concept, focusing on the technical aspects of the pixel tracker and its several challenges.

Summary (500 words):

With a maximum electron energy of 53 MeV and a magnetic field of 1 T, the task of tracking recurling electrons produced in muon decays with silicon sensors is very challenging. In these conditions, multiple Coulomb scattering becomes a key factor in the track momentum resolution. Nevertheless, with a material budget per tracking layer of 0.1%, the Mu3e experiment is expected to achieve a momentum resolution of less than 1 MeV. This is achieved by several means, which will be explained in the presentation. The chosen sensors are 50 micron thin High-Voltage Monolithic Active Pixel Sensors, the Mupix sensors, where the readout is implemented inside the detection substrate itself. This solution allows fast and efficient tracking without using the thick hybrid sensors. Furthermore, in the tracker's acceptance region the electric circuitry is implemented in the support structure into High Density Interconnects (HDIs). There, Aluminum traces are etched in thin polyimide substrates. Also, all sensors are connected through Single-point Tape Automated Bonding (SpTAB), which allows to connect the Aluminum traces without additional bonding material. Following the path towards material budget minimization, a Helium based cooling system has been designed. It is conceived to keep the temperature in the tracker below 35 C against a power dissipation of 200 mW/cm2.
Furthermore, the triggerless readout system presents major complexities: 2844 HV-MAPS pixel sensors deliver data from about 3000 LVDS channels at 1.25 Gbit/s. The data is then filtered through a system of boards and then fed to a GPU-based online track reconstruction farm. This readout configuration allows to perform event selection without a hardware-based trigger system.
With the construction phase quickly approaching, all these aspects have been investigated and the responses to the several challenges are implemented in detail. To prove the mechanical concept of the pixel ladders, a thermo-mechanical mockup has been produced with Silicon heater chips. This emulates the power consumption and heat dissipation of the tracker, and is ultimately used to verify the solidity of the whole structure and the efficiency of the cooling system. The electrical properties of the ladder themselves, instead, are investigated with test HDIs. Thanks to them, a single chip can be configured and read through Aluminum traces up to 24 cm long, whereas the maximum distance in the tracking system is 18 cm. As for the DAQ system, several testbeam runs have been organized, where the DAQ components are operated with different slices of the experiment. The characterization of the Mupix devices shows an efficiency of 99.5 % with less than 25 ns time resolution.
Since the Mu3e experiment implements novel and challenging solutions for several cutting-edge applications, reporting the results of the pre-production phase in such a large audience conference will be very fruitful. It could benefit both the possibly interested viewers and the Mu3e members themselves, as they may receive important inputs to further improve the design of their experiment for the Phase 2 of the experiment, where rates will be 20 times higher.

ASIC / **107**

The ETROC1: The first full chain precision timing prototype for CMS MTD Endcap Timing Layer (ETL) upgrade

Author: Tiehui Ted Liu[1]

[1] *Fermi National Accelerator Lab. (US)*

Corresponding Author: tiehui.ted.liu@cern.ch

The Endcap Timing Readout Chip (ETROC) is being developed for the CMS MTD Endcap Timing Layer (ETL) for the HL-LHC, to process LGAD signals with time resolution down to 30ps per track. The ETROC1 is the first full chain precision timing prototype, including preamplifier and discriminator, as well as a new low power TDC design that performs time-of-arrival (TOA) and time-over-threshold (TOT) measurements. It also includes a 4x4 pixel array with precision clock distribution

network that is scalable to the final full size 16x16 array. The performance of ETROC1 with bench test and beam test results are presented.

Summary (500 words):

The development of the ETROC ASIC is divided into three prototyping phases (in 65nm CMOS technology). ETROC0 consists of a single channel analog front-end with preamplifier and discriminator only, ETROC1 is 4x4 array with full chain precision timing signal processing including a new TDC stage for TOA/TOT measurements, while ETROC2 is the first full size and full functionality prototype chip (16x16). The ETROC0 chips have been demonstrated in beam with time resolution of around 33 ps from the pre-amplifier waveform analysis and around 42 ps from the discriminator pulses analysis. A subset of
ETROC0 chips have also been tested to a total ionizing dose (TID) of 100 MRad using X-ray machine at CERN and no performance degradation observed. The ETROC0 design is successful and is directly used without modification for ETROC1. The ETROC1 has 5x5 pixel arrays with a 4x4 pixel array H-tree style clock distribution network that is scalable to the final full size of 16x16. The ETROC1 is the first full chain precision timing prototype, aiming to study and demonstrate the performance of the full signal processing chain, with the goal to achieve 40 to 50 ps time resolution per hit with LGAD (~30ps per track
with two detector layer hits). One of the challenges of the ETROC design is that the TDC is required to consume less than 200 μW for each pixel at the nominal hit occupancy of 1%. To meet the low-power requirement, we use a single delay line for both the Time of Arrival (TOA) and the Time over Threshold (TOT) measurements without delay control. This TDC is based on a simple delay-line approach originally
developed in FPGA implementation. A double-strobe self-calibration scheme is used to compensate for process variation, temperature, and power supply voltage. The overall performances of the TDC have been
evaluated and meet the CMS ETL upgrade requirements. The TOA has a bin size of 17.8 ps within its effective dynamic range of 11.6 ns. The TOT has a bin size of 35.4 ps within its measured dynamic range of
9.8 ns. The effective measurement precisions of the TDC are 5.6 ps and 9.9 ps for the TOA and 10.4 ps and
16.7 ps for the TOT with and without the nonlinearity correction, respectively. The bare ETROC1 chips have been tested extensively using charge injection, and the measured performance agrees well with the
simulation, including the power consumptions. The bump bonded ETROC1 chips (with LGAD sensors) have been also extensively tested using charge injection, laser and test beam. The timing performance of the
full signal processing chain as well as the 4x4 pixel array clock distribution network has been studied. This
talk will briefly describe the ETROC1 design including the new TDC and clock tree distribution network,
and then focus on the bench test and beam test results of the bump bonded ETROC1 chips, and how the knowledge gained from bump bonded ETROC1 testing are applied to guide the on-going full size ETROC2 design.

Power, Grounding and Shielding / 108

48V input rad-hard DCDC converters for HEP experiments: development and results

Authors: Pablo Daniel Antoszczuk[1]; Stefano Michelis[1]; Giacomo Ripamonti[1]; Stefano Saggini[2]; Federico Iob[2]

[1] *CERN*

[2] *University of Udine*

Corresponding Author: pablo.daniel.antoszczuk@cern.ch

Two new radiation-hard DCDC converters are in development, which tolerate a higher input voltage (up to 48V) and provide a larger output power compared to existing solutions. They are called bPOL48V and rPOL48V, and they employ Gallium Nitride devices. bPOL48V can provide 12A of output current with 90% efficiency and is close to production readiness, while rPOL48V is in an early stage of development and is designed to provide an output current up to 30A. A linear regulator (linPOL48V) able step down the voltage from up to 48V with maximum output current of 200mA has been also designed and tested.

Summary (500 words):

In the past, a compact, rad-hard and efficient power distribution strategy for HEP detectors has been presented, based on two cascaded Point-of-Load DCDC converters: a first-stage converter (bPOL12V) having as input a 12V line creates a 2.5V domain, which powers the opto-electronic components. Second-stage converters (bPOL2V5) further step down the voltage from 2.5V to supply the front-end analog and digital circuits. bPOL12V and bPOL2V5 are today in production for HL-LHC.
In this work, a new conversion stage is introduced, able to step down the voltage from up to 48V. It can provide a larger output power compared to existing converters and can be used to supply bPOL12V, allowing to significantly reduce the current in the long cables from the off-detector power supplies.
Two converters with different architectures (bPOL48V and rPOL48V) are in design phase. Both use commercial Gallium Nitride (GaN) devices as power switches, which offer a reduced on-state resistance and a faster switching speed compared to silicon MOSFETs, leading to increased efficiency. In addition, GaN devices are highly tolerant to radiation. In particular, the commercial GaN power stage adopted for bPOL48V has been successfully tested for radiation (Total Ionizing Dose, TID, up to 100Mrad, Linear Energy Transfer, LET, up to 45 MeV*cm2/mg and displacement damage up to 1e15 n/cm2 1MeV eq).*
bPOL48V is a buck converter able to provide a maximum output current of 12A. Its output voltage can be programmed down to 1.2V, making it usable also for the 12V-20V to 1.2V-2.5V conversion. Its controller has been designed at CERN using a high-voltage commercial 0.35µm CMOS technology. It features several internal linear regulators to provide the correct voltages to the control circuitry, a predictive logic to optimize the dead times and a voltage-mode control loop.
*The measured efficiency at full load is around 90% (for Vin=48 and Vout=12V), the converter has been tested up to a TID of 50Mrad without appreciable change in the performance, while single event tests showed that there are no destructive events up to an LET of 40 MeV*cm2/mg. Only rare Single Event Transient on the output voltage have been found, with variations of less than 5% for LET=28.8 MeV*cm2/mg and less than 10% for LET=40 MeV*cm2/mg. Displacement damage tests are ongoing.
rPOL48V is today in an early stage of development. It is based on a resonant architecture, which allows using significantly smaller inductors compared to bPOL48V. It has a fixed conversion ratio of 4 and features very high efficiency and current capability up to Iout=30A. A non-rad-hard version of this converter is under development using commercial components: commercial GaN devices for the power stage, commercial drivers, while the control is implemented in an FPGA. In parallel, a rad-hard version of the drivers and of the controller is being designed at CERN.
A rad-hard linear regulator, linPOL48V, has been also developed. It can provide a selectable voltage (minimum 1.2V) from up to Vin=48V. The maximum current rating is 200mA and it has been already tested for TID and SEE, with similar performance to bPOL48V.

Programmable Logic, Design Tools and Methods / 109

PAM-4 implementation study for future high-speed links

Authors: Chaowaroj Wanotayaroj[1]; Eduardo Brandao De Souza Mendes[1]; Sophie Baron[1]

[1] *CERN*

Corresponding Author: ma.x@cern.ch

With the ever-increasing amount of data from HEP experiments, the transmission rates must keep up. To mitigate the exponential growth of the total loss due to the increased frequency, the 4-Level Pulse-amplitude Modulation (PAM-4) could be envisaged, allowing to reach 56 Gbps or even 112 Gbps in extremely high-end applications. A system using PAM-4 encoders and transceivers has been built based on FPGA as a proof-of-concept to demonstrate potential future links. In this talk,

the PAM-4 modulation will be introduced, the performance of this initial system will be presented and the challenges for future links will be discussed.

Summary (500 words):

With the ever-increasing amount of data produced by the High Energy Physics experiments, the transmission rates from the detectors to the back-end stages must keep up. To mitigate the exponential growth of the total loss due to the increased frequency, the 4-Level Pulse-amplitude Modulation (PAM-4) could be envisaged. Where the line rate of Non-Return to Zero (NRZ) modulated signals is capping at 28 Gbps per lane, PAM-4 allows to reach 56 Gbps or even 112 Gbps in extremely high-end applications. Investigating the implementation of such links in FPGA is one of the activities carried out by the Work Package 6 of the CERN EP Research and Development programme. In this framework, a proof-of-concept system of high-speed links using NRZ-28 Gbps and PAM4-56 Gbps has been built, based on a Xilinx Virtex evaluation platform and various commercial optoelectronics transceivers. 53.1 Gbps PAM-4 and 26.6 Gbps NRZ eye pattern have been analysed using high-end oscilloscopes and optimized using various equalization schemes. PAM-4 standard Forward Error Correction (FEC) codes have also been implemented and characterized over electrical and optical layers in terms of coding gain and latency. Finally, the telecom and datacom markets were investigated to identify development perspectives for the research and development for future links.
In this talk, the PAM-4 modulation scheme will be introduced, the performance of the proof-of-concept implementing these high-speed links will be presented and the current and future challenges for an error-free communication will be discussed.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 110

CMS Muon Drift Tubes HL-LHC Slice Test

Author: Barbara Alvarez Gonzalez[1]

[1] *Universidad de Oviedo (ES)*

Corresponding Author: barbara.alvarez.gonzalez@cern.ch

To tolerate the High Luminosity LHC (HL-LHC) data taking conditions on the detector electronics of the CMS Drift Tubes (DT) chambers need to be replaced during Long Shutdown 3. The first prototype of the HL-LHC electronics for the On detector Board for the DT chambers (OBDT) have been installed in CMS connected to the DT chambers of one out of sixty sectors and integrated in the central data acquisition and trigger system. The signals from the chambers are split and reach both the legacy and Phase 2 demonstrator chains, which will allow them to operate in parallel during LHC collisions.

Summary (500 words):

After delivering an integrated luminosity of more than 160 fb-1 until the end of Run 2, at the beginning of 2019, LHC was shut down for two years (LS2) in order to get its accelerator-chain and detectors upgraded for the HL-LHC phase. During this LS2, the Compact Muon Solenoid (CMS) experiment aims to upgrade its electronics and detector performance to improve the data taking and a precise reconstruction of all the particles in high pile-up conditions of HL-LHC. The Drift Tube (DT) chambers are one of the important parts of the CMS muon system responsible for identifying, measuring and triggering on muons by the precise measurement of their position. The electronics of the CMS DT chambers will need to be replaced for the HL-LHC operation [1]. A DT muon station consists of an assembly of chambers around a fixed value of radial distance R, with four barrel stations labelled as MB1 to MB4, being MB1 the closest to the interaction point. Along the beam axis z DTs are divided into 5 slices, called wheels, with wheel 0 centered at z=0 and wheel+1 and wheel+2 in the positive z direction and wheel-1 and wheel-2 in the negative z direction. Within each wheel, chambers are arranged in 12 sectors at azimuthal angle. The first prototypes of the HL-LHC electronics for the CMS On detector Board for the Drift Tube chambers (OBDT) have been installed in one out of sixty sectors (wheel+2 sector 12) of DT chambers on the CMS detector, in the so-called Slice Test, and integrated in the central data acquisition and trigger system during LS2. The four chambers in this sector were instrumented with OBDT prototypes [2]. DT

Chamber frontend pulses carrying the time information of the chamber hits reach both the legacy on detector electronics, so called minicrate, and the OBDTs through specifically designed splitter boards that take consideration to the signal integrity. Thirteen OBDTs distributed in five mechanical frames which also take care of the thermal interface to the water cooling loop are installed in this sector. The Phase 2 backend functionality (slow control, trigger generation and DAQ) is implemented in FW running on DT uTCA boards (TM7 [3]) developed for the Phase 1 upgrade. The stability and performance of the Phase 2 electronic demonstrator in cosmic events will be shown in this talk and compared with the present system. We plan to run this Phase 2 parallel system in collisions during Run 3, which will allow us to test final pre-production prototypes under realistic conditions (radiation, magnetic field) and further refine trigger algorithms.

[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Muon Detectors, CERN-LHCC-2017-012, CMS-TDR-016,2017. [2] Andrea Triossi et al, Electronics Developments for Phase-2 Upgrade of CMS Drift Tubes https://pos.sissa.it/343/035/pdf [3] Andrea Triossi, A New Data Concentrator for the CMS Muon Barrel Track Finder, http://cds.cern.ch/record/1712905

Posters Production, Testing and Reliability / 111

Blade-board for stability studies of the slow-control functionality of the CMS muon DT uTCA backend

Authors: Dmitry Eliseev[1]; Uwe Boettger[1]

[1] *Rheinisch Westfaelische Tech. Hoch. (DE)*

Corresponding Author: dmitry.eliseev@cern.ch

In recent years, some minor issues were observed during operation of CMS Muon specific TM7 blade-boards, which are data concentrators for the hit-data from Drift-Tube chambers. These blade-boards reside in the uTCA crates in the service cavern of CMS. Talk presents a recently developed test-board, which is used as an inexpensive substitution of TM7. The developed test-board implements a Module Management Controller (MMC) and some further functional aspects of TM7. It facilitates extensive tests for observing operational stability with many TM7-alike blades within one uTCA crate. Along with presenting the test-board and its firmware, talk also covers ongoing stability studies.

Summary (500 words):

The CMS muon Drift-Tube (DT) System uTCA crates carry a number of TM7 blade-boards, which concentrate the hit-data received from the DT chambers. The Module Management Controler (MMC) functionality of a TM7 is implemented by the firmware, running on a dedicated microcontroller within the TM7's circuit. In general, the implemented MMC circuit and functionality replicate the CERN MMC Mezzanine. During the run activity in the last years some minor issues in the behaviour of the TM7 boards were observed. These issues mainly concern the TM7 slow-control activity. In order to provide detailed observations of the behaviour of a fully occupied uTCA crate, without having to use a number of expensive TM7 boards, an imitator test-board was developed. The central component of the developed test-board is the ATmega128 microcontroller, the same as the one present at the CERN MMC Mezzanine. This test-board completely includes the MMC functionality and parts of TM7 circuitry. Along with the MMC, the board also includes an I2C-switch and a Phased-Locked-Loop (PLL) components. Connectors in the front part of the board enable safe access to the LHC clock signal, which is originally sourced from the backplane of the uTCA crate. A PLL-passed clock signal is available with the front panel connectors as well. The functional pins of the microcontroller are connected to a number of breakout pins. In order to emulate high-power load in the respective uTCA slot, the test-board carries a set of switchable power resistors. With the listed features the developed test-board potentially may be used as a cost effective debug instrument which emulates the slow-control activities between a uTCA blade-board and the crate. Use of the test-board may also be possible in order to test some changes in the MMC firmware, before flashing it in the MMC-microcontroller of the TM7 board. This talk describes the developed board and presents the ongoing stability studies.

Systems, Planning, Installation, Commissioning and Running Experience / 112

The CMS Inner Tracker electronics system development and tests

Author: Stella Orfanelli[1]

[1] *CERN*

Corresponding Author: styliani.orfanelli@cern.ch

A new Silicon Tracker will be built for the Phase 2 Upgrade of the CMS experiment. The innermost part, called the Inner Tracker, will be featuring high-granularity pixelated silicon sensors and will need to cope with extreme radiation levels and hit rates. The pixel electronics system is based on innovative solutions such as a new pixel ASIC developed by the RD53 collaboration, the novel serial powering scheme and advanced technologies for the high bandwidth readout system. The recently optimised design of the CMS Inner Tracker electronics system will be presented along with system test results with prototype components.

Summary (500 words):

A new Silicon Tracker will be built for the Phase 2 Upgrade of the CMS experiment to fully exploit the physics potential during the HL-LHC era. The innermost part, called the Inner Tracker (IT), will be featuring silicon sensors with a pixel size of 2500 μm^2 and covering an active area of 4.9 m^2. The IT system will be composed of 3892 pixel modules and the total number of readout channels will be around 2 billion.

For the ultimate HL-LHC scenario of 4000 fb^-1, the radiation levels will be reaching the unprecedented values of 1.9 Grad and 3.5E16 n.eq./cm^2 and the hit rates will go up to 3.7 GHz/cm^2 in the innermost layers. A simple installation and removal scheme is supported as the detector needs to be removed during each long shutdown giving also the possibility to replace and repair parts, if needed. The mass of the detector has to be as low as possible to avoid degradation of the tracking performance. These requirements pose significant challenges for the design of the electronics system. Novel solutions and advanced technologies are deployed for the design of a low-mass and radiation-hard pixel detector of high performance.

A new pixel readout chip has been designed in 65 nm CMOS technology by the RD53 collaboration. In 2021, the prototype CMS pixel chip will arrive including fixes for known bugs of previous chip versions as well as all the production required features. Serial powering will be used to power up to 12 pixel modules in series based on Shunt-LDO regulators integrated on the chips. The sensor bias will be following the modularity of the serial power chains. The pixel modules will be readout/controlled by low-mass electrical links at 1.28 Gbps/160 Mbps which will be reaching the opto-conversion boards, known as portcards. A new, optimised design of the portcard will host three pairs of lpGBT and Vtrx+ and will be powered independently by a power mezzanine with a two stage DCDC converter scheme. The portcards will be installed on a cartridge at higher radius such that their components can withstand the radiation levels. The design of this cartridge has been significantly improved in order to minimise the radiation induced attenuation along the optical fibers. A data acquisition system based on FPGA boards is developed for the back-end electronics to calibrate, control and readout the pixel modules and send the data to the central CMS DAQ. The back-end power supply system has also been greatly simplified decreasing the required design effort and cost.

In this contribution the optimised design of the CMS Inner Tracker electronics system will be presented along with system test results of serial power chains with RD53A pixel modules with sensors mounted on realistic mechanical structures, operated at cold temperatures and readout by prototype electrical elinks and portcards studying both powering and signal integrity aspects of the system.

Production, Testing and Reliability / 113

The lpGBT production testing system

Author: Nour El Houda Guettouche[1]

Co-authors: Daniel Hernandez Montesinos [2]; Julian Maxime Mendez [3]; Szymon Kulis [3]; Stefan Biereigel [3]; Paulo Rodrigues Simoes Moreira [3]; Ken Wyllie [3]; Sophie Baron [3]; David Porret [3]; Pedro Vicente Leitao [3]

[1] *Centre National de la Recherche Scientifique (FR)*

[2] *GBTx - BE Group*

[3] *CERN*

Corresponding Author: nour.el.houda.guettouche@cern.ch

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC designed to implement multipurpose high-speed bidirectional serial links in HEP experiments. Having more than 320 programmable registers, the ASIC is highly configurable. Its test must cover a large variety of functionalities which will be validated at three different power-supply voltages, two temperatures and over more than 1000 parameters. As more than 175 000 chips will be produced, optimizing the test duration is also a strong requirement. In this talk, an overview of the lpGBT v1 production test system will be given, challenges will be presented, and performance will be discussed.

Summary (500 words):

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC designed to implement multipurpose high-speed bidirectional serial links in HEP experiments. Being data agnostic, it is typically used as the interface between the on-detector and off-detector electronics. It has a highly flexible front-end interface, supporting multiple serial links with configurable data rates for downlink and uplink data streams and also providing slow control features. Having more than 320 configurable registers and 11 configuration pins, the ASIC also provides a large number of programmable options to enable its efficient use in a wide variety of front-end applications. A new version of the ASIC, the lpGBT V1 is being produced to be installed in the experiments. More than 175 000 components will be distributed amongst the users.
The first testing phase will start in Q4 2021. More than 18 000 devices will be individually tested in order to deliver only devices that meet specific criteria based on their performance. The full production lot will be launched immediately after this first batch is tested and will be completed in Q4 2022.
The lpGBT tester runs up to 17 checkers to validate the device functionality. These tests cover all the chip's interfaces and features including high-speed links, PLLs, digital circuits as well as analog blocks such as ADCs and DACs. Additionally, to check all corners, the full test will be performed at three different power-supplies voltages, at -30℃ and at room temperatures. More than 1000 parameters will be measured per chip. Due to the number of components and the complexity of the test, one of the biggest challenges is to minimize the running time while maximizing the coverage.
To achieve this requirement, a specific test environment has been designed allowing the exchange of data and control signals between a Xilinx Virtex-7 FPGA VC707 Evaluation Kit, a custom lpGBT mezzanine board and a sophisticated test software. Finally, the test procedure is controlled via a general-purpose system developed at CERN, handling Graphical User Interface, data storage and postmortem analysis. The complexity of the tester also implied to use the state-of-the-art versioning tool, GitLAB, and a big part of the functionality it provides.
In this talk, an overview of the lpGBT v1 production test system will be given, the development process and the challenges will be presented, and performance will be discussed.

Posters Optoelectronics and Links / 114

The Versatile Link+ Demo Board (VLDB+)

Author: Daniel Hernandez Montesinos[1]

Co-authors: Sophie Baron [2]; Nour El Houda Guettouche [3]; Julian Maxime Mendez [2]

[1] *GBTx - BE Group*

[2] *CERN*

[3] *Centre National de la Recherche Scientifique (FR)*

Corresponding Author: daniel.hernandez.montesinos@cern.ch

The Versatile Link Plus Demonstrator Board (VLDB+) is a board designed by CERN's EP-ESE group to provide an evaluation kit for the new Versatile Link ecosystem (VL+). This reference design gathers three custom and radiation hard devices, namely, the Low-Power Gigabit Transceiver (lpGBT), the Versatile Link Plus Transceiver (VTRx+) and the FEASTMP DCDCs. These components are common to some of the HL-HLC experiments and constitute the main elements of the board. The VLDB+ is already being extensively used by several experiments to get acquainted with the whole ecosystem in order to facilitate their final Front-end system design.

Summary (500 words):

The Versatile Link Plus Demonstrator Board (VLDB+) is a board designed by CERN's EP-ESE group to provide an evaluation kit for the new Versatile Link Plus ecosystem. This reference design includes only qualified radiation hard components, also designed at CERN, such as the Low-Power Gigabit Transceiver (lpGBT), the Versatile Link Plus Transceiver (VTRx+) and the FEASTMP DCDCs, common to some of the HL-HLC experiments, as ATLAS and CMS, and composing the main elements of the board.
In the VLDB+, the lpGBT and the VTRx+ work together to support the main interface of the board: the high-speed bidirectional data transmission link over the optical fiber. In addition, the lpGBT features ad hoc electrical interfaces called eLinks. These eLinks are provided through a second interface that are the two FPGA Mezzanine Card connectors (FMC), which share all the eLink inputs and outputs. Additionally, not only the eLinks are available on the FMC interface: the lpGBT's GPIOs, Analog Peripherals, I2C master and the Resetout signal are also present.
As the dual FMC interface housed in the VLDB+ complies with the VITA standard, the board can be connected as a mezzanine to a compatible FPGA Evaluation Kit, as the VC707. This FPGA-VLDB+ system provides an optimal way to work with the lpGBT-VTRx+ pair: the FPGA can interface with the VLDB+ as a back-end (via the VTRx+ and the optical link) and a front-end (via the FMC) system at the same time.
The VLDB+ can also be used as a standalone board. In this case, the connectivity is of course limited with respect to the mezzanine mode, but there is still access to some clock signals, test outputs as well as slow control features available on the board – enough to check ad-hoc lpGBT configurations or to try out some slow control functionalities.
Moreover, in the VLDB+ the control of the lpGBT using the I2C interface is performed through a 10-pin connector, so that a custom external RaspberryPI Kit (RPI Kit), composed of a Raspberry Pi 4 and a Translator Board, can be connected to it. The RPI Kit operates with a web interface called PiGBT and offers a simple way to control the lpGBT configuration.
The VLDB+ board offers an excellent opportunity to be introduced to and get acquainted with the extremely versatile VL+ ecosystem. This presentation describes in depth a wide range of board features that will enable the users to obtain the best hardware configuration for their initial needs.

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Towards Optical Data Transmission for High Energy Physics Using Silicon Photonics

Author: Theoni Prousalidi[1]

Co-authors: Anthony Frederick Bulling [2]; Carmelo Scarcella [2]; Christophe Sigaud [2]; Csaba Soos [2]; Jan Troska [2]; Lauri Olantera [2]; Leonardo Marcon [2]; Max Archie Hamish Court [3]; Milana Lalovic [4]; Stella Orfanelli [2]; Stephane Detraz [2]; Ulrik Sandven [2]

[1] *National Technical Univ. of Athens (GR)*

[2] *CERN*

[3] *University of Bath (GB)*

[4] *University of Belgrade (RS)*

Corresponding Author: theoni.prousalidi@cern.ch

Future upgrades of CERN Experiments will require low power optical data links to support ever-increasing data-rates at ever-higher radiation levels. Silicon Photonics is a CMOS optoelectronics technology compatible with such requirements. We present the results of an optical transceiver proof of concept based on a Silicon Photonic Integrated Circuit coupled to existing radiation tolerant ASICs.

Summary (500 words):

A new generation of radiation tolerant optical links is being developed to cope with the increased data volume and radiation levels in the innermost regions of the HL-LHC.

The architecture of optical data links for particle detectors developed so far combines custom rad-tolerant optical transceivers deployed at the front-end with commercial off-the-shelf (COTS) optics and electronics deployed at the other end of the link in a radiation-free area. Optical transceivers (TRx) are bidirectional modules with the receiver (Rx) channel converting data from the optical to the electrical domain and the transmitter (Tx) channel doing the opposite (electrical to optical). The radiation tolerance of the optoelectronic technology currently used (based on VCSELs and pin photodiodes) does not allow the use of optical link components in the innermost regions of the detectors.

Within the CERN EP R&D program we are investigating the use of Silicon Photonics (SiPh) for the rad-tolerant optical transceiver that will be installed close to the readout electronics of silicon particle sensors. SiPh leverages CMOS fabrication processes to realise optical components and circuits on silicon chips. Recent studies have shown high levels of radiation tolerance of SiPh components to Total Ionizing Dose (TID) and Total Fluence.

The test vehicle used to carry out this research activity is a Photonic Integrated Circuit (PICv2) that we designed and fabricated through a multi project wafer (MPW) using the imec Silicon Photonics foundry. The chip integrates various optical components and circuits that can be used to build data transmission lab demonstrators and to study the radiation tolerance of the SiPh technology.

In this work, we present the result of a front-end transceiver demonstration that uses optical components integrated onto PICv2 together with existing rad-tolerant ASICs. The Tx is based on a micro-Ring Modulator (RM) driven by the lpGBT, a radiation tolerant SerDes developed at CERN for the HL-LHC detectors. The RM was connected to the differential CML output of the lpGBT Tx. This implementation shows a wide open 10.24 Gb/s eye diagram of the signal transmitted through the single-mode optical fiber (SMF), validating the compatibility of CML signals with driving RMs. The Rx is based on a Germanium (Ge) high-speed photodiode coupled to the GBTIA, a radiation tolerant transimpedance amplifier widely used for the front-end receiver of optical data links at CERN (the common projects Versatile Link and Versatile Link+). We demonstrated the compatibility of integrated Ge photodiodes with the existing rad-tolerant TIA that was designed to operate with discrete pin photodiodes. The receiver, when operating at 4.8 Gb/s, shows a sensitivity of approximately -10 dBm. The optical signal was fed into the receiver using standard SMF, and the use of polarization splitting grating couplers makes the receiver polarization insensitive. In synergy with the CMS development for phase-3 Inner Tracker upgrade, we plan to transmit data from RD53 Pixel Read-out Chips over optical fiber using rad-tolerant SiPh TRx for the first time.

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Power, Readout and Service Hybrids for the CMS Phase-2 Upgrade

Author: Angelos Zografos[1]

Co-authors: Adam Erik Hollos [1]; Georges Blanchot [1]; Irene Mateos Dominguez [1]; Mark Istvan Kovacs [1]; Nikola Rasevic

[1] *CERN*

Corresponding Author: angelos.zografos@cern.ch

The CMS Tracker Phase 2 Upgrade modules integrate DCDC powering stages and an optical transceiver to power and control the front-end hybrids. The strip-strip (2S) module contains a Service Hybrid (2S-SEH) with two stage DC-DC power conversion, an lpGBT with optical interface (VTRx+), high voltage biasing and temperature sensor ports. The pixel-strip (PS) module utilizes a separate two stage DCDC converter circuit (PS-POH) and a Readout Hybrid (PS-ROH) containing the communication interface. The design and performance of these three hybrids and their integration in their respective modules will be presented.

Summary (500 words):

Two module types (2S and PS) will be used in the Compact Muon Solenoid (CMS) Tracker Phase 2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC). The 2S modules contain a double strip sensor configuration with an active area of (10 × 10) cm2, wire bonded to two front-end hybrids that are powered and controlled by a service hybrid. The PS modules contain a strip sensor and a macro-pixel sensor of (5 × 10) cm2 wire bonded to two front-end hybrids interconnected with a power hybrid on one side and with an optical readout hybrid on the opposite side. The service and readout hybrids enable the optical transmission of clock, control and data at transmission speeds up to 5 Gbps for the 2S modules and up to 10 Gbps for the PS modules in the cold and radioactive environment of the Tracker.
The 2S-SEH integrates a two stage power converter. The first stage is using the BPOL12 ASIC to deliver 2.55V for the BPOL2V5 and the laser driver of the VTRX+ transceiver. The second stage is based on a BPOL2V5 ASIC, delivering 1.25V for the rest of the ASICs. Custom air core coils and shields were developed to fit with the constrained height and area of this hybrid and achieve the low noise requirements. The hybrid includes an lpGBT and a VTRx+ optical module. The hybrid is a five layers flexible circuit laminated on a carbon fibre stiffener, compensated against thermal expansion mismatches. A tight folded over area accommodates the high voltage biasing and temperature monitoring connectivity for both sensors.
The PS-POH is half the size compared to the 2S-SEH and is a four plus one layer polyimide and FR4 rigid-flex circuit. It integrates one BPOL12V ASIC, followed by two second stage BPOL2V5 ASICs, delivering 2.55V, 1.25V and 1.05V for the two front-end hybrids and the distant readout hybrid. To achieve a robust power integrity at module level, an additional flexible cable connects the power hybrid to the readout hybrid. Similarly to the 2S-SEH custom air core coils and micro-milled aluminium shield with solderable plating were used for the confined volume of this hybrid.
The PS Readout hybrid is made of a four layer carbon fibre stiffened flexible circuit containing the lpGBT ASIC and the VTRX+ transceiver to provide the readout and control of the PS module. It also provides auxiliary 1V25 power path from the flexible power cable to the front-end hybrids.
The PS-POH, PS-ROH and 2S-SEH were evaluated with test cards and prototype modules were built. In this contribution, the design considerations and practices for developing these circuits along with the monitor and control features that they support, will be presented. Power integrity simulations will be compared to measurements on the actual hybrids. Thermal performance and efficiency of the PS-POH shall be analysed. Finally, the performance of full PS and 2S skeletons (modules without sensors) constructed using these power, readout and service hybrids connected to their respective front-end hybrids, will be shown.

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The Fast Beam Condition Monitor as a standalone luminometer of the CMS experiment at the HL-LHC

Author: Mohammad Sedghi[1]

[1] *Isfahan University of Technology (IR)*

Corresponding Author: mohammad.sedghi@cern.ch

In the Phase-2 CMS upgrade, a luminosity uncertainty of 1% is targeted. To achieve this goal, measurements from multiple luminometers with orthogonal systematics are required. A standalone luminometer, the Fast Beam Condition Monitor (FBCM) is being designed for online bunch-by-bunch luminosity measurement. Its fast timing properties also enable the measurement of beam induced background. In this talk, the hardware architecture and the read-out protocol of the FBCM is described. The expected performance with a simple behavioral model of the front-end comprising a

constant fraction discriminator is discussed, though the final implementation in the ASIC is still under discussion.

Summary (500 words):

A fast beam condition monitor (FBCM) is being designed as a standalone luminometer to run independently of the CMS central trigger and data acquisition systems at the HL-LHC and to provide bunch-by-bunch luminosity measurement in real time. The ultimate goal of 1% luminosity uncertainty after final calibration implies a deviation from linearity of less than 0.02%/(Hz/μb). To meet this goal, the FBCM will utilize silicon-pad sensors with a zero-counting algorithm of the observed hits and it will provide the time of arrival (ToA) and the time over threshold (ToT) of the signal pulse with a few ns resolution. The FBCM will have a semi-digital readout to transfer these data to the back-end, with the front-end chip producing a non-clocked output pulse upon the creation of an ionising signal in the silicon-pad sensor.
The lpGBT (Low Power GigaBit Transceiver, an ASIC widely used for data transmission and control in the Phase-2 projects) will receive the semi-digital output i.e. called e-links via flex cables. It will continuously sample the front-end output pulse every 0.78 ns corresponding to the e-link speed (1.28 Gbps), then transmit it to the back-end over an optical transceiver, the VTRx+. At the back-end, an ATCA (Advanced Telecommunications Computing Architecture) digital processing unit finds the rising edge and pulse duration and tags the ToA and the ToT, respectively, after synchronizing to the LHC clock. The ATCA unit histograms the number of hits per bunch-crossing per sensor. The probability of zero-hit occurrence and the mean number of hits – assuming a Poisson distribution for the hits – are computed from these histograms. The timing information provides the capability to measure beam-induced background, as well. To optimize resources, the FBCM ASIC design will be launched in early 2022, and make the most use of existing 65 nm blocks, optimized for the functionality and performance of FBCM.
In this talk, the expected performance of the FBCM with a simple front-end behavioral model is presented. The model includes a fast analog amplifier with 14 ns settling time from peak to baseline, shapers and a constant fraction discriminator (CFD) with the capability of adjusting the thresholds to tune the rising edge to the signal peak. The rising edge of the front-end output pulse corresponds to the peak of the amplified analog signal (using 2 ns and 0.51 for the CFD delay and the fraction, respectively) and the pulse duration is equivalent to the ToT. The pulse width of the semi-digital output is a monotonic function of the signal amplitude, which is also beneficial to monitor the MIP amplitude spectrum and thus the sensor's radiation damage.
Simulation results also show that the FBCM will provide the required statistical uncertainty and deviation from linearity by employing 336 silicon-pad sensors, each with an area of about 3 mm^2. In addition, the front-end with sensitivity to at least 6000 electrons will satisfy the longevity constraints for an exposure of 1 MeV neutron equivalent fluence of 3.5×10^{15} per cm^2.

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Precision luminosity measurement at CMS with the Pixel Luminosity Telescope

Author: Andres Guillermo Delannoy Sotomayor[1]

Co-authors: Paul Lujan [2]; Francesco Romeo [3]

[1] *University of Tennessee (US)*

[2] *University of Canterbury (NZ)*

[3] *Vanderbilt University*

Corresponding Author: andres.delannoy@cern.ch

The Pixel Luminosity Telescope (PLT) is a silicon pixel detector dedicated to luminosity measurement at the CMS experiment. It is arranged into 16 "telescopes" of three planes each, with eight telescopes arranged around the beam pipe at either end of the CMS detector, outside the pixel endcap. In the talk, the commissioning, calibration, operational history, and performance of the detector during Run 2 (2015-2018) of the LHC is presented. Studies of detector performance and the monitoring and mitigation of radiation damage effects will be highlighted.

Summary (500 words):

The PLT was installed during the LHC's Long Shutdown 1 as part of the CMS Phase 1 upgrade and consists of silicon sensors arranged into 16 "telescopes" such that particles originating from the CMS interaction point will pass through all three planes in the telescope. It takes advantage of the "fast-or" readout mode built into the CMS phase-0 PSI46v2 pixel readout chip (ROC) which can be processed at the full LHC bunch-crossing frequency of 40 MHz to determine the instantaneous luminosity from the rate of triple coincidences. The readout electronics for this signal path require custom FPGA firmware developed for the PLT to histogram the number of triple coincidences in each telescope. The full pixel information, including hit position and charge, is read out at a lower rate of ~3.3 kHz and organized by a Token Bit Manager chip which distributes clock and trigger signals, coordinates the readout of the three individual ROCs, and produces a single readout for each telescope. The analog signals corresponding to a fourth of the detector reach the opto-motherboard (OMB) where they are converted into optical signals using analog optohybrids. The OMB also contains a digital optohybrid that receives and distributes optical clock, trigger, and control signals from the back-end hardware. The silicon sensors are actively cooled using C6F14 at a temperature of -15 °C and provided by a cooling structure fabricated from titanium powder using a selective laser melting process, resulting in cooling tubes of 2.8 mm in diameter with several small-radius bends. A full rebuild of the PLT is scheduled to be installed for Run 3 of the LHC, which incorporates a new OMB slow hub chip design to coordinate I2C control signals and includes an extensive burn-in period under thermal cycles for the assembled components. Several detailed studies were carried out to determine the impact of radiation damage on the performance of the detector. In particular, the depletion voltage can be determined for each telescope by processing data from configurable and automated bias scans in order to anticipate the need for changes in the operational high voltage. Furthermore, pulse heights and sensor efficiencies, which rely on the full pixel readout, were examined and shown to be complementary measurements of the detector performance. Careful consideration of the quality of gain calibrations and effects such as time-walk and noise was required in order to get conclusive results from the analysis of pulse heights. The measurement of sensor efficiency relies on track reconstruction to determine the fraction of events where a hit is expected in all three sensors but is not reported by one of them and includes the optimization of track selection designed to reduce contributions from background tracks. The lessons learned from Run 2 and outlook for Run 3 will be highlighted, with emphasis on the monitoring of detector performance and mitigation of the effects of radiation damage.

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FastIC: A Fast Integrated Circuit for the Readout of High Performance Detectors

Authors: Sergio Gomez Fernandez[1]; Jerome Alexandre Alozy[2]; Michael Campbell[2]; Jose Maria Fernandez-Tenllado Arribas[2]; Rafel Manera[3]; Juan Mauricio Ferre[1]; Carolina Pujol[3]; David Sánchez[None]; Anand Sanmukh[3]; Andreu Sanuy[3]; Rafael Ballabriga Sune[2]; David Gascon[1]

[1] *University of Barcelona (ES)*

[2] *CERN*

[3] *University of Barcelona*

Corresponding Author: sgomez@fqa.ub.edu

This work presents the 8-channel FastIC ASIC developed in CMOS 65nm technology suitable for the readout of positive and negative polarity sensors in High Energy Physics experiments, Cherenkov detectors and Time-of-Flight systems. The front-end can be configured to perform analog summation of up to 4 single-ended channels before discrimination in view of exploiting area segmentation. The outputs encode the Time-Of-Arrival information and linear Energy measurement in the 5uA – 20mA input range, with a power consumption of 12mW/ch with preset settings. Measurements of Single Photon Time Resolution with a red-light laser source and a Hamamatsu SiPM S13360-3050CS are ~140ps FWHM.

Summary (500 words):

This work presents the 8-channel FastIC (Fast Integrated Circuit) developed in 65 nm technology suitable for High Energy Physics experiments, Cherenkov detectors and, other Time-of-Flight systems, based on the classic multi-branch architecture (i.e., time, energy, and trigger information) with similarities to the HRFlexToT ASIC. The front-end stage processes the signals in current mode with an input impedance below 20 Ω and can be programmed to cope with positive and negative polarity sensors, such as photomultiplier tubes, microchannel plates, and Silicon Photomultipliers. The 8 channels can be configured to work as 4 differential channels. Alternatively, 4 single-ended sensor signals can be summed, and the discrimination is performed on the resulting pulse. This active summation functionality is integrated to explore the impact of segmenting a large sensor area to improve time jitter.
Each FastIC channel provides the information of Time-Of-Arrival and a linear energy measurement of the detected photons. Time measurement is generated through a leading-edge comparator whose output provides a non-Linear ToT response encoding the arrival time of the events in the rising edge of a pulse. The signal processing path for energy measurement generates a binary pulse whose width is proportional to the collected charge (using the same processing scheme as the HRFlexToT ASIC) with a linearity error below 3% over the entire dynamic range from 5 uA to 20 mA. Different trigger methods with configurable thresholds are available to indicate when a valid event is captured. The output driver can be programmed in CMOS single-ended or differential Scalable Low-Voltage Signaling. Alternatively, internal analog signals can be readout by means of a high-speed analog driver per channel.
The power consumption of FastIC is 12 mW/ch in single-ended mode (full channel functionality) or 6 mW/ch when only the time branch is used (non-linear ToT operation). The maximum hit rate per channel is 2 MHz using the linear ToT and about 50 MHz when employing the non-linear ToT. Simulation results using a Hamamatsu SiPM S13360-3050CS model at 4.5 V over-voltage and parasitic interconnections, resulted in a predicted electronics jitter of 30.9 ps rms Single-Photon Time Resolution (SPTR) in single-ended positive polarity configuration. This predicted SPTR decreased to 16.8 ps when segmenting this 3x3 mm2 sensor into four 1.5x1.5 mm2 SiPMs.
SPTR laboratory measurements using a red-light laser source and a Hamamatsu SiPM S13360-3050CS are ~140 ps Full Width at Half Maximum (FWHM) at 10.6 V over-voltage. The HRFlexToT ASIC tested in the same conditions yielded an SPTR of 161.5 ps FWHM at 10.5 V over-voltage and thus showing that FastIC provides a lower electronic jitter. Note that the measured SPTR is the convolution of the SPTR of the sensor, the laser FWHM and the electronic jitter. A Hamamatsu PMT R5900 producing pulses with ~5 ns FWHM, and a theoretical transient time spread of 330 ps FWHM, was tested using the same red-light laser resulting in an SPTR of 340 ps FWHM after time walk correction showing that the FastIC does not degrade the time response for this detector, nor the pulse shape.

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A Dual-mode NRZ/PAM4 Transmitter IP Purposed for Advanced CMOS Technology Nodes

Author: Thomas Gardiner[1]

Co-authors: Mark Lyndon Prydderch [2]; Stephen Bell [3]; Lawrence Jones [3]

[1] *STFC*

[2] *Science and Technology Facilities Council STFC (GB)*

[3] *Science and Technology Facilities Council*

Corresponding Author: thomas.gardiner@stfc.ac.uk

While the potential of PAM4 is becoming more practical, many designs still choose the NRZ approach. This paper presents a customisable dual-mode PAM4/NRZ transmitter IP (with 4/2-tap channel equalisation) deployable in multiple CMOS technologies. IP has been fabricated in 65nm (28Gbps/14Gbps), 180nm (10Gbps/5Gbps) technologies. A radiation-hardened 65nm (20Gbps/10Gbps) flavour is in active development. The serialization process is achieved using 16 self-generated synchronised clocks and produces 2 data streams with 4 equalisation streams to minimise inter-symbol inference. IP can be customised to transmit 1 PAM-4 (non-standard encoding) or 2 NRZ (Aurora 64b66b) data streams (with additional IO) prior to fabrication.

Summary (500 words):

Following on our previous successful design of a 10Gbps Aurora 64b66b NRZ transmitter in 65nm technology, presented at TWEPP 2018, significant design improvements have been made to increase maximum operating frequency, power efficiency and area consumption. Furthermore, the design now generates 2 streams of data and 4 additional streams for channel equalisation to minimise inter-symbol interference. The improved dual-mode transmitter IP makes use of an inductor-capacitor oscillator PLL to produce a high-quality clock, short-channel CMOS circuitry for energy efficient low frequency operations, and current-mode logic for both high performance high frequency operations and to drive the outputs. The IP has been fabricated in 65nm and 180nm CMOS technologies, and a 65nm radiation-hardened flavour is planned for fabrication in December 2021. The target speeds for these devices are 28Gbps PAM4/14Gbps NRZ, 10Gbps PAM4/5Gbps NRZ and 20Gbps PAM4/10Gbps NRZ respectively. The data encoding used by the IP is Aurora 64b66b for NRZ and for PAM4, a non-standard encoding protocol based on 256b257b with grey coding is used. The serialization process, which produces 2 streams of high-speed data, relies on 16 synchronised clocks for interleaved clock multiplexing. The 16 synchronised clocks are generated from a single high-speed clock driving interweaved clock circuitry; this is achieved by high performance flip-flops and multiplexers rather than complex synchronisation circuitry. The architecture has been engineered in such a way that simple modifications can determine whether a twin pair of NRZ serializers or a single PAM4 serializer is produced. This is achieved by swapping the digital encoding module in a hierarchical digital system, and the analogue line-driver circuit that drives the output, with the rest of the circuitry remaining the same. The PAM4 option can be configured (post-fabrication) to operate in NRZ and produce a single stream of data. The fabricated designs produced on Multi-Project Wafer runs and subsequently wire-bonded to test-boards for evaluation. The NRZ lanes will be evaluated by FPGA synthesized PRBS data checkers whereas the PAM4 lanes will be evaluated through eye-diagrams and waveforms from a high sample-rate oscilloscope. The transmission links will be evaluated with varied track lengths and the additional optional use of a TI Retimer IC (NRZ), or a SAMTEC FireFly optical transceiver (NRZ); Performance gain will be evaluated. We will present the results from the electrical characterization, and expand further on the development of the rad-hard 65nm design and the future plans for a planned 28nm design.

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Experimental characterisation of the RD50-MPW2 High Voltage-CMOS sensor chip

Authors: Samuel Powell[1]; Gianluigi Casse[1]; Eva Vilella Figueras[1]; Joost Vossebeld[1]; Chenfan Zhang[2]; Matthew Franks[None]

[1] *University of Liverpool (GB)*

[2] *University of Liverpool*

Corresponding Author: samuel.powell@cern.ch

The CERN-RD50 collaboration aims to develop and study High Voltage-CMOS (HV-CMOS) sensors for use in very high luminosity colliders. Measurements will be presented for the RD50-MPW2 chip, a prototype HV-CMOS pixel detector with an active matrix of 8 x 8 pixels. The active matrix is tested with injection pulses, a radioactive source and a proton beam. This talk will cover the FPGA based DAQ system, the software and firmware developed to take and analyse data. Proton test-beam telescope measurements will be presented as well as the detector gain and noise characterisation using charge injection and radioactive source measurements.

Summary (500 words):

RD50-MPW2 is a prototype pixel detector chip in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry. It contains several circuits and test structures, including an 8 x 8 active matrix with two flavours of high granularity pixels (60 µm x 60 µm) that use different methods to reset the sensing diode. These methods are named continuous-reset and switched-reset. Pixels with continuous-reset use a continuous current to reset the Charge Sensitive Amplifier (CSA) after a particle hit, resulting in a dead time that is proportional to the number of electrons collected by the sensor. With this pixel flavour, it is possible to process a particle hit that generates 10k electrons within 90 ns only. Pixels with switched-reset use the output of the discriminator to switch on and off a larger reset current. The switched current resets the CSA in 15 ns and shortens the dead time to 45 ns, independently of the

number of collected electrons. As the larger reset current is active for a very short time only, the power consumption is kept low.
The DAQ system to measure RD50-MPW2 is composed of a Xilinx ZC706 FPGA board, a Caribou data acquisition board and the dedicated chip board. The Zynq-7000 XC7Z045 SoC on the ZC706 is programmed with a custom version of the Peary Caribou firmware, a processor side coded in C and logic side coded in VHDL. A custom C++ GUI has been developed to communicate with the firmware to configure and readout the chip. This allows a simple interface to be used to select a pixel for injection, perform a hit map scan, generate a response curve to calculate the gain, generate s-curve data to calculate the noise, modify the internal DACs of RD50-MPW2, adjust the internal DC baseline level, set thresholds and control the analogue multiplexer. An overview of the entire DAQ chains hardware and firmware/software will be presented.
Results of a recent test-beam at the Northumbria Rutherford Cancer Centre in the UK will be presented. Measurements were taken using an IBA Proteus One – S2C2 Synchrocyclotron proton beam, using a range of energies from 70.2 to 200 MeV.

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The CMS Barrel Calorimeter Processor demonstrator (BCPv1) board evaluation

Authors: Nikitas Loukas[1]; Stephen Goadhouse[2]

Co-authors: Alberto Belloni [3]; Ales Svetek [4]; Alexander Madorsky [5]; Bob Hirosky [2]; Colin Jessop [1]; Jesra Tikalsky [4]; John Charles Hakala [2]; Joseph Patrick Mariano [1]; Ka Wa Ho [1]; Luis Alberto Perez Moreno [6]; Lynne Lutton [1]; Marcelo Vicente [7]; Nancy Marinelli [1]; Thomas Andrew Gorski [4]; Thomas Bruce Hurt Anderson [2]; Tullio Grassi [8]

[1] *University of Notre Dame (US)*

[2] *University of Virginia (US)*

[3] *University of Maryland (US)*

[4] *University of Wisconsin Madison (US)*

[5] *University of Florida (US)*

[6] *Princeton University (US)*

[7] *Stanford University (US)*

[8] *Univ. of Maryland (USA)*

Corresponding Author: nikitas.loukas@cern.ch

For the Phase 2 of the LHC, the central electromagnetic (EB) and hadronic (HCAL) calorimeters of the CMS experiment require a new back-end electronics for its readout. The first version of the ATCA-based blade, the Barrel calorimeter processor (BCPv1), has been developed with a large flexibility to allow evaluation of the different strategies. The performance of the optical links as well as clock distribution options are presented. BCPv1 is tested together with new Front-End and Trigger boards, as well as with the DAQ and trigger interface board, namely DTH, in order to demonstrate that it meets the required specifications.

Summary (500 words):

On the roadmap to a final hardware platform, the Barrel Calorimeter Processor demonstrator board (BCP demo) or BCPv1 has been produced and tested. This ATCA blade has been designed as a development platform that fulfills ECAL Barrel (EB) and HCAL subsystems (HB, HF, HO) as well as Trigger, DAQ and TCDS requirements in CMS. It hosts one KU115 Xilinx Kintex UltraScale and provides 56 bidirectional optical links, running any serial protocol that is synchronous or asynchronous to the LHC (~40.08MHz) within line rates from <1Gb/s to 16Gb/s. The aim of this design was not to build a powerful processor board like the final BCP platform which will host a large FPGA, but instead to have a hardware platform flexible enough to be able to evaluate all required functions and define margins. BCPv1's board infrastructure includes: A System-on-Chip (SoC) in a Xilinx ZYNQ device based on the Embedded Linux Mezzanine (ELM) that controls the board. A ZYNQ-IPMC based on RealTime OS (RTOS) to monitor and manage the power acting within micro-seconds. An Ethernet Switch Module (ESM) to interconnect 5

ports. An FPGA fansink, I/O SMAs, and an RJ45 to make testing on the bench easy. SAMTEC Fireflys, SFPs and Jitter cleaners support the optical links. A 4x lane SSD up to 5G and 10GBASE-T PHY supports custom readout. Five BCPv1 have been produced from which three are operating at CERN performing integration tests with other prototypes for CMS and two in the USA serving more tests. All are fully functional and testing them did not reveal any major issue while minor fixes are noted to be applied in the coming next design (BCPv2). Eye scans of the optical links for all BCPv1 are presented. Compatibility with the Phase-2 DAQ and TCDS Hub (DTH) card also is presented. The successful implementations of the 15.66Gb/s flavor of SlinkRocket links for the DAQ interface and the symmetric TCLinks for the TCDS interface are shown. The distribution of the high precision "LHC" clock to the new ECAL Barrel On-Detector electronics with Jitter performance was measured. Clock jitter is critical on phase 2 EB because inadequate performance affects timing and energy resolution of Trigger Primitives. The Trigger Datapath was also tested with the BCPv1 sending data patterns to the new Trigger card (APd1) running 16.0Gb/s links using 64b/66b encoding. Finally, the BCPv1 to BCPv1 interface was also tested using the same protocol as the trigger. BCPv1 thermal measurements are presented with firmware utilizing large resources. Many firmware projects were developed in order to support these tests. In addition, a unified firmware was developed to support the CMS ECAL Barrel vertical test where the BCPv1 is accessing the new Very Front-End chip (LiTeDTU) through lpGBTs hosted in the new Front-End electronics. The BCPv1 base firmware is based on APx-FS developed for the APd1 card. It supports among others features the SF66 protocol used in the calorimeter trigger. We present the prototype BCPv1 design verification results in the ongoing CMS phase-2 upgrade project.

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Design, Production, Burn-in and Tests of the hybrid circuits of the Upstream Tracker at the LHCb detector

Authors: Federico De Benedetti[1]; Paolo Gandini[2]; Nicola Neri[1]; Marco Petruzzo[3]; Nadim Conti[1]

Co-authors: Andrea Capsoni [1]; Mauro Citterio [1]; Fabio Manca [4]; Andrea Merli [1]; Fabrizio Sabatini [1]; Elisabetta Spadaro Norella [1]; Alessandro Andreani [1]

[1] *Università degli Studi e INFN Milano (IT)*

[2] *INFN Milano (IT)*

[3] *INFN Milano*

[4] *Università degli Studi e INFN Milano*

Corresponding Author: federico.de.benedetti@cern.ch

Abstract: We present a detailed description of the design, prototyping and production of the hybrid circuits for the front-end electronics of the Upstream Tracker at LHCb. The multilayer flexible circuits are design to host the front-end chips, ensure a low radiation length and withstand the harsh environment conditions of the data taking.

Summary (500 words):

The Upstream Tracker is a tracking detector at the LHCb experiment, placed just upstream of the dipole magnet. It consists of four layers of silicon strip sensors with high granularity and low radiation length. We have designed produced and delivered the hybrid circuits that host the ASICs developed for the detector front end. The inner part is read out by 8-chip hybrids (80 in total), while the outer part of the detector uses 4-chip circuits (888 in total). This contribution covers the design and prototyping process of those flexible circuits, organized in "panels", and the challenges deriving from their mass production and delivery to the final assembly laboratory. The full chain of electronics tests and burnin process in order to avoid early failures on chips is also described.

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Verification methodology of a multi-mode radiation-hard high-speed transceiver ASIC

Authors: Adithya Pulli[1]; Iraklis Kremastiotis[1]; Szymon Kulis[1]

[1] *CERN*

Corresponding Author: adithya.pulli@cern.ch

The second version of Low Power Giga Bit Transceiver (lpGBTv1) addresses the functional and radiation-related issues discovered during the testing of lpGBTv0 prototype. Considerable changes to the chip configuration architecture and flow were required. The Universal Verification Methodology (UVM) based verification environment was extensively refactored to address the functional verification challenges posed by the architectural changes in the chip. Additionally, a novel SEE verification strategy was proposed and implemented. In this paper we present the revamped UVM verification framework of lpGBTv1 and discuss the verification process, tools, techniques and metrics used to sign-off the design before submission.

Summary (500 words):

In modern ASIC development, verification accounts for about 60% of the overall project time. Effort spent in improving the quality of the radiation tolerant ASIC designs before manufacturing greatly minimizes the risk of running into unexpected functional errors and Single Event Effects (SEEs) in the fabricated chip which in-turn saves time-consuming silicon debug effort and costs of respin. The primary focus of any verification activity is to ensure the highest possible quality of the design under test by identifying functional errors and SEE vulnerabilities in the design before tape-out. To efficiently address the challenges of verification, the underlying verification framework must be capable of supporting modular implementation of constrained random verification content along with the required checkers and coverage.

The lpGBT is a versatile radiation-hard ASIC designed to provide high speed multi-purpose bidirectional links for high energy physics experiments. The versatility of the chip is managed through the vast configuration space exposed to the user through multiple configuration interfaces. This configurability coupled with supported configuration flows increase the state space of the chip resulting in verification complexity.

The new lpGBTv1 testbench architecture, built using UVM, is modular and extensible, which enabled easy development of highly randomized functional tests closely representing the use-cases of the chip. Various advanced UVM techniques such as agent/sequence layering and register abstractions were used while developing the UVM environment. The refactored UVM environment also enabled thorough SEE verification with same level of randomization in the stimuli as used for functional verification. High level of randomization implied that each test had to be rerun multiple times with different random seeds to completely cover the state-space of the stimulus. Oracle Grid Engine (OGE) based batch system was extensively used to parallelize multiple test executions. Metrics such as code coverage, functional coverage, fault coverage, regression pass-rate and verification plan score were used and tracked over the project life-cycle to obtain quantitative view of the progress and quality of verification. The contribution will present processes, technologies, tools, techniques and metrics used during the verification and sign-off of lpGBTv1 along with a brief summary of the bugs discovered in the process. Besides providing examples worth replicating in verification of complex SEE robust ASICs, we will also discuss approaches that did not work.

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Design of a IoT based multi-channel temperature monitoring system

Authors: Barbara Clerbaux[None]; Pierre-Alexandre Petitjean[None]; Yifan Yang[None]; Daniel Gomez de Gracia[1]

[1] *ULB*

Corresponding Author: daniel.gomez.de.gracia@ulb.be

In the scope of the Jiangmen Underground Neutrino Observatory (JUNO) project, 6 back-end card (BEC) mezzanines connected to one BEC base board are in charge of compensating the attenuated incoming data from 48 front-end channels over 48 100-meters-long ethernet cables. Each of the mezzanines has 16 equalizers that may be subject to overheating. It is important to monitor their temperature in real time. However, collecting data from a relatively large (1080) number of mezzanines is not a trivial task. In this work we propose a solution based on Wi-Fi mesh. Both technical details and test results will be reported.

Summary (500 words):

Gathering information from many electronic devices for real-time analysis can be a challenging task. In the context of the Jiangmen Underground Neutrino Observatory (JUNO), there is an electronic system in charge of capturing the interactions of electron antineutrinos issued from nearby nuclear reactors. This system starts at the in-water electronics, where 18000 large (20-inch) Photomultiplier Tubes (PMTs), 25600 small (3-inch) PMTs, and 2000 PMTs installed in the surrounding water pool send hit information by groups of three to the Global Control Units (GCUs). The GCUs digitize and store the received signals in a large local memory under the control of a Field-Programmable Gate Array (FPGA). They wait for the trigger decision and send out event data as well as trigger requests to the outside-water system. On the surface, a back-end card (BEC) is used as a concentrator to collect trigger requests from 48 GCUs, and each of the incoming trigger request signals passes through an equalizer to compensate for the attenuation due to the long cables. There are 180 BECs in the system, each containing 6 Mezzanines equipped with 16 equalizers. This makes up for a total of 17280 equalizers. The main challenges are measuring the temperatures of multiple equalizers and sending them to a central computer. This is necessary to make sure the equalizers perform stably and don't overheat.
Three i2c-compatible temperature sensors were placed on the bottom layer of one BEC base board to monitor 96 equalizers installed on the top layer of 6 Mezzanine cards. The three sensors can be accessed through a single i2c bus. We propose to use an esp32-pico development board to read out the temperatures from 3 sensors sitting on the same base board, and to link it to the central computer through Wi-Fi. Due to the possibility of having diminished performance caused by channel overlapping when too many devices are connected to a same Wi-Fi network, a Wi-Fi mesh group consisting of 180 ESP32 boards might be a more suitable solution to link all the boards to the central computer.
Some experiments were performed to validate the implementation. Two thermocouples were attached to two reference equalizers and were connected to a digital thermometer. This allowed to determine the difference between the equalizer's true temperatures and the temperatures measured by the sensors, which are placed 8mm apart from the equalizer. The wireless range of the ESP32 was assessed to ensure it met the requirements of our implementation. The server's bandwidth was also measured and found to be of 35000 80-byte messages per second, which is enough to deal with the required message rate of 36 80-byte messages per second. Additionally, the complete implementation was tested on a reduced network of 30 boards. The group was established successfully and run smoothly with negligible loss of information over a period of seven days. Given these results, we believe the system can scale to a 180-board mesh.

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The Caribou DAQ System – Current Status and Ongoing Developments

Author: Eric Buschmann[1]

[1] *CERN*

Corresponding Author: eric.buschmann@cern.ch

Caribou is a flexible open-source DAQ system designed for laboratory and high-rate beam tests and easy integration of new silicon-pixel detector prototypes. It uses common hardware, firmware and software components that can be shared across different projects, thereby reducing the development effort and cost for such readout systems significantly.

Summary (500 words):

The Caribou flexible readout system consists of a Xilinx Zynq System-on-Chip (SoC) board that runs the Peary DAQ software and detector-specific firmware, and the Control and Readout (CaR) board, which contains programmable power
supplies, current sources, ADCs and DACs, clocks, high- and low-speed communication interfaces, and is connected to an application-specific chip-board that interfaces with the detector.
The CaR board provides the resources used by typical detector prototypes therefore simplifying the detector-specific chip-boards. Data transmission, processing, and detector control is performed by the software and firmware on
the SoC-board and can take advantage of the common components provided by Caribou. Through this versatile hardware and the modular design, the turnaround time for supporting new detectors is minimized.
It can operate standalone and also provides EUDAQ2 integration for operation in test beam environments.

Caribou is developed and maintained as a collaborative effort within the EP R&D silicon work packages of the strategic R&D programme of the CERN Experimental Physics Department (EP R&D) and the RD50 and AIDAinnova collaborations.
Currently 10 participating institutes use the Caribou platform with custom chip boards for 7 types of pixel-detectors, and several more are under development. Caribou is also used for automated testing of calorimeter front-end electronics.

This contribution presents the Caribou system and gives an overview of recent developments, such as a new and improved hardware revision, integration of external waveform sampling, integration of the new ATTRACT FASTPIX chip for
sub-nanosecond timing, and current efforts to migrate the system to the Zynq UltraScale+ platform using a commercial System-on-Module with a custom carrier board.

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Augmenting Quality and Throughput of Functional Testing and Device Characterization for the ABCStar ATLAS-ITk Strips Readout ASIC Through a Semiconductor Test Industry Partnership

Authors: James Michael Botte[1]; Thomas Koffas[1]; Bryce John Norman[1]; Robert Scouten[2]

[1] *Carleton University (CA)*

[2] *DA-Integrated*

Corresponding Author: james.michael.botte@cern.ch

To instrument the 60 million ATLAS ITk Strips Sensor channels, CERN developed the mixed-signal ABCStar front-end readout ASIC. Over 350,000 devices on 753 wafers containing 466 ASICs each will be extensively tested to provide the chips required for sensor modules. Carleton achieved a 3-10 times improvement in throughput, without compromising test coverage or data collection, by developing new tools and techniques in partnership with a specialist wafer testing company – jointly overcoming the methodological, technical, and semantic divides that exist between physics laboratories and the semiconductor test industry, and opening new possibilities in ASIC testing for future particle physics projects.

Summary (500 words):

The Department of Physics at Carleton University has a venerable history of involvement in detector conceptualization, design, construction, and testing. Due to the growing prevalence of Application Specific Integrated Circuits (ASICs) in experiments of all scales – and an identified need for more capacity around all aspects of their design, production, and testing – in 2015 we undertook to gain the required

expertise to test unpackaged ASICs at the wafer level as part of the Canadian contribution to the silicon-strips portion of the new ATLAS Inner Tracker (ITk) for the HL-LHC.

ASICs for particle physics have traditionally been tested at academic or government facilities that allow for extensive research and experimentation, and where generous access to human resources and bespoke equipment is the norm. While many of these ASICs were of exceptional complexity and presented immense difficulties to test, the semiconductor testing industry is routinely dealing with far more challenging designs than those being used in, for instance, ITk. Rather than duplicating existing approaches, we partnered with a specialist ASIC testing company to leverage their expertise and infrastructure with the intent of achieving significant improvements in wafer testing capabilities and throughput, and shorter test engineering and implementation cycles, while learning how to navigate the constraints inherently imposed by such a service-oriented commercial-industrial environment. We achieved a 3-10 times improvement in throughput over existing approaches, without compromising test coverage or data collection, by developing new tools and techniques with our industry partner – jointly overcoming the methodological, technical, and semantic divides that exist between our laboratories and the semiconductor test industry, and opening new possibilities in ASIC testing for future particle physics projects.

In 2018, we successfully tested our first ITk silicon-strips ABC130 interim front-end readout ASIC wafer using tests reverse-engineered from the ITSDAQ system – that we translated into custom C++ test software and stimulus vectors for the industry standard Advantest Smart Scale V93000 automated wafer test system. For the much-enhanced next generation ABCStarV0 readout chip in 2019, we started from scratch with the test requirements and the ASIC design specification to create a comparable test suite of our own that leveraged what we learned from the ABC130 and the capabilities and limitations of the V93000. Notably, we developed a macro compiler to generate test vectors and C++ code from assembler-like commands for direct import into the Advantest system, leveraged an advanced tester technique called Digital Source dynamic vectors to improve performance by an order of magnitude, and were able to "port" the Verilog validation tests from the ASIC simulation environment to the Avantest system using Cadence Xcelium. In 2020, we received ABCStarV1 wafers and adapted and enhanced our test suite as part of the pre-production phase.

Over 350,000 devices on 753 wafers containing 466 ASICs each need to be extensively tested before they are diced to provide high confidence the chips used for sensor module assembly are in compliance with all design specifications. Carleton and DA-Integrated have committed to test half of these wafers over two years.

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Development of AC-LGADs for high-rate Particle Detection

Authors: Hartmut Sadrozinski[1]; Abraham Seiden[2]; Nicolo Cartiglia[3]; Simone Mazza[4]; Gabriel Saffier-Ewing[None]

[1] *University of California,Santa Cruz (US)*

[2] *SCIPP-UC Santa Cruz*

[3] *INFN Torino (IT)*

[4] *SCIPP - UC Santa Cruz*

Corresponding Authors: gabe@anadyneinc.com, hartmut@ucsc.edu

Low-Gain Avalanche Detectors (LGADs) are thin silicon detectors with moderate internal signal amplification yielding excellent time resolution of close to 10's ps. AC-LGADs (aka Resistive Silicon Detectors RSD) have un-segmented gain layer and N-layer, and a di-electric layer separating the metal readout pads, guaranteeing a 100% fill-factor. The high spatial precision of few 10's μm is achieved by using the pulse height information from multiple pads.
We present an evaluation of the high-rate suitability of AC-LGADs based on focused IR-Laser scans wrt the limitations that high-speed readout ASICs can expect from high-flux charged particles and X-rays.

Summary (500 words):

Development of AC-LGADs for high-rate Particle Detection
(UC Santa Cruz, INFN Torino, Fondazione Bruno Kessler)
Low Gain Avalanche Detectors (LGADs) are thin silicon detectors with moderate internal signal amplification (up to a gain of ~50) [1]. LGADs with 50 μm thickness have been shown to be capable of providing timing measurements for minimum-ionizing particles with resolution of about 30 picoseconds [2], [3]. In addition, the fast rise time (as low as 150 ps for 20 μm thickness) and short full charge collection time (around 1 ns) of LGADs are suitable for high repetition rate measurements in photon science and other fields [4].
The first implementation of this technology will be with the High-Granularity Timing Detector (HGTD) in ATLAS and the Endcap Timing Layer (ETL) in CMS. The addition of precise timing information from LGADs will help mitigate the increase of pile-up and improve the detector performance and physics sensitivity. The LGAD pads planned are 1.3mmx1.3mm. The current major limiting factor in granularity is due to structures preventing breakdown caused by high electric fields in near-by segmented implants.
We present here an evaluation of the high-rate suitability of AC-LGADs (also named Resistive Silicon Detectors RSD) that can be made with much greater segmentation for the charge collection while maintaining a 100% fill factor. This is achieved by employing un-segmented (p-type) gain layer and (n-type) N-layer, and a di-electric layer separating the metal readout pads. The design allows great flexibility in the choice of the geometry of the metal readout pads, both in terms of pitch and size. The high spatial precision is achieved by using the information from multiple pads, exploiting the intrinsic charge sharing capabilities of the AC-LGAD provided by the common N-layer. It depends on the location, and the pitch and size of the pads. A version of these LGADs has been shown to provide spatial resolution on the few 10‘s of micrometer scale [4].
We tested the performance of AC-LGAD with focused IR-Laser scans directed alternatively at the readout side on the front and the bias side on the back of the AC-LGAD, which allows to investigate the following detector parameters: sheet resistance and termination resistance of the n-layer, thickness of the isolation di-electric, doping profile of the gain layer, pitch and size of the readout pads and the bulk thickness.
We use the data to evaluate the limitations high-speed readout ASICs can expect from high-flux charged particles and X-rays and from constraints of power consumption in the readout chain.

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Production, Testing and Reliability / 135

Hybrids Acceptance Tools for the CMS Phase Two Tracker Upgrade

Author: Irene Mateos Dominguez[1]

Co-authors: Adam Erik Hollos [2]; Angelos Zografos [1]; Georges Blanchot [1]; Inna Makarenko [3]; Magnus Loutit [4]; Mark Istvan Kovacs [1]; Sarah Seif El Nasr [4]; Younes Otarid [5]

[1] *CERN*

[2] *Budapest University of Technology and Economics*

[3] *Universite Libre de Bruxelles (BE)*

[4] *University of Bristol (GB)*

[5] *DESY*

Corresponding Author: irene.mateos.dominguez@cern.ch

Up to fifty thousand front-end and service hybrids are required for the CMS Tracker Phase Two Upgrade. These hybrids, which are built on carbon fibre stiffened circuits and contain several flip-chip

ASICs, will be glued in module structures, making repairs almost impossible. Due to their complexity, testing within production is a very important aspect. A multiplexed testing infrastructure, based on custom crates and test cards will be presented. This testing hardware is supported by software tools to enable the exhaustive verification of hybrids at the manufacturing sites and for their acceptance within the collaboration.

Summary (500 words):

The Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) is based on two main types of modules, the strip-strip (2S) and the pixel-strip (PS). The 2S modules contain two parallel strip sensors of 10 × 10 cm2 and two front-end hybrids interconnected with a service hybrid. The PS modules contain a strip sensor and a macro pixelated strip sensor of 5 × 10 cm2 and two front-end hybrids interconnected with a power and a data service hybrid. These modules require state of the art High Density Interconnect (HDI) front-end hybrids assembled with fine pitch flip-chip front-end ASICs, connectors and passives. Ten different front-end hybrid variants and five additional service, power and readout hybrid variants are today completing their prototyping phase for the upgraded Tracker.
The complexity and difficulty of repair of these hybrid circuits requires them to be tested during production. Therefore, a test system has been developed to support the testing during production.
This test infrastructure is based on a 3U 19 inch sub-rack with custom developed multiplexer backplanes enabling the testing of twelve hybrid circuits in one crate. The backplanes are designed to multiplex high speed differential signals, USB, control lines and to distribute power. The backplane connects to a data acquisition FPGA, the FC7, which controls the multiplexer and processes the data. The FC7 is connected through Ethernet to a computer running the test.
To connect to the multiplexing rack, five plug-in test cards were developed, one to test each type of hybrid: the 2S Front-end hybrids, the 2S Service hybrids, the PS Front-end hybrids, the PS Readout hybrids and the PS Power hybrids. In order to avoid designing different plug-in cards for each hybrid type variant, they are mounted on interchangeable sockets and specific interconnection circuits are designed to connect them to the test cards. All the test cards have been prototyped and they were used to qualify all the received hybrids.
The Phase Two Acquisition and Control Framework developed by the Data Acquisition team served as baseline for the implementation of test procedures compatible with the test cards. The plug-in test cards are controlled through USB, using a custom driver. A supervising user interface able to control up to three crates identifies the installed test cards and the hybrids under test, loads the corresponding firmware in the backend card, executes the associated test procedures and archives the test results in a production database. The tool monitors the extraction of the tested hybrids and provides instructions to the operator to tag the hybrid as functional or non-functional. This tool ultimately enables the testing at contractor sites for the whole production and will maximize the yield of functionally tested hybrids. The same tool will be used for acceptance controls within the collaboration in order to guarantee the full functionality of hybrids delivered finally to the module assembly sites.

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QTIA, a 2.5 or 10 Gbps 4-Channel Array Optical Receiver ASIC in a 65 nm CMOS Technology

Authors: Hanhan Sun[1]; Xing Huang[2]; C.-P. CHAO[3]; S.-W. CHEN[3]; Binwei DENG[4]; Datao Gong[5]; Suen Hou[6]; Guangming Huang[7]; Szymon Kulis[8]; C.-Y. LI[3]; Chonghan Liu[1]; Tiankuan Liu[9]; Paulo Rodrigues Simoes Moreira[8]; Quan Sun[10]; Jingbo Ye[11]; Li Zhang[None]; Wei Zhang[1]

[1] *Southern Methodist University*

[2] *Southern Methodist University (SMU)*

[3] *APAC Opto Electronics Inc.*

[4] *Hubei Polytechnic University*

[5] *Southern Methodist Univeristy*

[6] *Academia Sinica*

[7] *Central China Normal University*

[8] *CERN*

[9] *Southern Methodist University (US)*

[10] *Fermi National Accelerator Lab.*

[11] *Southern Methodist University, Department of Physics*

Corresponding Author: hanhans@smu.edu

The Quad Transimpedance and limiting Amplifier (QTIA) is a 4-channel array optical receiver ASIC, developed using a 65 nm CMOS process. It is configurable between the bit rate of 2.56 Gbps and 10 Gbps. QTIA offers careful matching to both GaAs and InGaAs photodiodes. At this R&D stage, each channel has a different biasing scheme to the photodiode to look for the optimal coupling. A charge pump is implemented in one channel to provide a higher reverse bias voltage, mitigating radiation effects on the photodiodes. QTIA circuit functions pass preliminary but successful tests.

Summary (500 words):

High-speed optical data communication is widely used for on-detector readout electronics in high-energy physics (HEP) experiments. In these applications, the transmitter and receiver of the optical link need to be radiation tolerant to the detector operation environment. In applications near the interaction points, radiation-induced degradation of the photodiode is the most challenging issue nowadays. This degradation causes many parameters to change and is different between GaAs and InGaAs photodiodes. There are many studies on photodiodes in radiation, mostly by CERN. For InGaAs photodiodes, radiation results in an increase of the dark current (up to 1 mA) and a rise in the junction capacitance (up to several pF). GaAs photodiodes suffer from a significant loss in responsivity due to radiation. Based on these findings, we designed and prototyped a quad transimpedance and limiting amplifier (QTIA) ASIC to research mitigation options.

QTIA is selectable to operate at 2.56 or 10 Gbps data rate. It adopts a fully differential architecture. Photodiodes are AC coupled to the TIA using on-chip capacitors. The integrated bias circuits provide proper biasing to the photodiode. The bias circuits in all channels are different. The Up-bias circuit is realized by PMOS with source degeneration in channel 2. The Down-bias circuit is composed of NMOS with source degeneration in channel 3. Both Up-and Down-bias circuits are used in channel 1 and channel 4. The bias voltage is tied to a 2.5 V power supply in channel 2 and channel 3. A charge pump (CP) is implemented in channel 1 to raise the bias voltage to photodiode to a level determined by its leakage current. In channel 4, the bias voltage is provided through an external power pad.

A fully differential cascade TIA with programmable feedback resistance is designed to achieve low noise and high bandwidth. The limiting amplifier has two stages with shared inductors and two active feedback stages to simultaneously achieve high gain and bandwidth. The output driver has adjustable output amplitude and drives a 100-ohm differential output load.

QTIA is 2 mm × 2 mm. It has been fabricated and assembled in the ultra-small and lightweight optical module, QTRx, together with a 4-channel array laser driver, QLDD. Preliminary tests at 2.56 Gbps indicate that channel 4 with the bias circuits on both sides and the external bias voltage display the best performances, with a sensitivity of – 17 dBm for a BER of 1E-12. For -6 dBm input, the total jitter is 46.7 ps with a random jitter of 2.7 ps and a deterministic jitter of 12.5 ps. The preliminary and conservative result of channel 1 sensitivity is -12 dBm with the charge pump output over 6.5 V. The nominal differential output amplitude remains 400 mVpp even for small input signals. The power consumption is below 72 mW per channel (without CP). A full set of optical and irradiation test results with different photodiodes will be carried out. We will present the results we have by the time of the conference.

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Development of a 20 Gbps PAM4 Data Transmitter ASIC for Particle Physics Experiments

Authors: Li Zhang[1]; Deng Binwei[2]; Chao C.-P.[3]; s.-w. Chen[4]; Rui Francisco[5]; Datao Gong[6]; DI GUO[6]; Dongxu Yang[6]; Suen Hou[7]; Guangming Huang[8]; C.-Y. Li[4]; Chonghan Liu[9]; Tiankuan Liu[9]; Paulo Moreira[5]; Jeffrey Prinzie[10]; Xiangming Sun[8]; Hanhan Sun[1]; Quan Sun[11]; Szymon KULIS[5]; Jingbo Ye[9]; Wei Zhang[1]; Wei Zhou[9]

[1] *Southern Methodist University and Central China Normal University*

[2] *Hubei Polytechnic University*

[3] *APAC Opto Electronics Inc.,*

[4] *APAC Opto Electronics Inc.*

[5] *CERN*

[6] *Southern Methodist University*

[7] *Academia Sinica*

[8] *Central China Normal University*

[9] *Southern Methodist University*

[10] *KU Leuven*

[11] *FNAL*

Corresponding Author: zhangli@mail.smu.edu

Abstract: GBS20 is a transmitter ASIC for particle physics experiments. Two serializers each at 5.12 or 10.24 Gbps share a 5.12 GHz PLL clock. The serializers' output is combined to a PAM4 signal that drives a VCSEL. The input data channels, each at 1.28 Gbps, is scrambled by a PRBS7 that is also the internal test pattern generator. Preliminary tests indicate that the prototype works at 10.24 and 20.48 Gbps PAM4 with a TOSA. More tests, including irradiation, will be carried out. The next step is to develop a pluggable transmitter module GBT20 base on this ASIC.

Summary (500 words):

Summary:
High-speed serial data transmission is widely used to send data from on-detector readout electronics to off-detector electronics in high-energy physics (HEP) experiments, demonstrated by experiments on the Large Hardon Collider (LHC). Physics and detector developments call for high data bandwidth yet the opto-electronics components of the optical link on the detector side face challenges such as radiation, low power dissipation and low mass plus small foot print. The lpGBT ASIC developed for the high-luminosity LHC (HL-LHC) upgrades reaches 10.24 Gbps NRZ (non-return-to-zero) data rate. Re-using many of the design blocks of lpGBT and adding the PAM4 (Pulse Amplitude Modulation 4-level) combiner, GBS20 doubles the transmission data rate in the same fiber.

GBS20 has 16 input data channels (each at 1.28 Gbps) that feed the two serializers. The input data is scrambled by a PRBS7 that doubles as an internal test pattern generator. The two serializers, adapted from that in lpGBT, share the 5.12 GHz PLL also from lpGBT. The output from the serializers is combined into a PAM4 signal after through a five stages limiting amplifier. The amplitudes of the MSB and LSB can be independently adjusted to cope with possible nonlinearity in the system. The LSB or MSB driver can also be turned off, providing a way to check the serializer's NRZ output. The PAM4 output driver uses a shared inductor and a CTLE structure to adjust its bandwidth. A programmable capacitive load is added to damp overshooting as in the PAM4 signal case that is more of a problem than in the case of NRZ.

The GBS20 prototype is 2 mm × 2 mm. Test boards are assembled with electrical output through SMA connectors, a TOSA or a VCSEL die under an LC lens. Preliminary tests with the TOSA display good performances. In the single channel output mode, the OMA is 650 μW, the peak-peak jitter is 20 ps. In the PAM4 mode, the maximal OMA is 1 mW and total jitter is around 50 ps. The power dissipation is less than 250 mW when PAM4 work in 2.5 V power supply during VCSEL with maximal bias and modulation current. In some low power dissipation application filed, this ASIC dissipation can reduce to 164 mW with switching power supply to 1.2 V. A full set of optical and irradiation tests will be carried out in the coming months. We will present the results we have by the time of the conference.

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A radiation-tolerant clock generator for the CMS Endcap Timing Layer readout chip

Authors: Hanhan Sun[1]; Quan Sun[2]; Stefan Biereigel[3]; Datao Gong[4]; Rui De Oliveira Francisco[None]; Guangming Huang[5]; Xing Huang[6]; Szymon Kulis[3]; Paul Leroux[7]; Chonghan Liu[1]; Tiankuan Liu[4]; Tiehui Ted Liu[8]; Paulo Rodrigues Simoes Moreira[3]; Jeffrey Prinzie[None]; Jinyuan Wu[8]; Jingbo Ye[9]; Li Zhang[None]; Wei Zhang[1]

[1] *Southern Methodist University*

[2] *Fermi National Accelerator Lab.*

[3] *CERN*

[4] *Southern Methodist University (US)*

[5] *Central China Normal University*

[6] *Southern Methodist University (SMU)*

[7] *KU Leuven*

[8] *Fermi National Accelerator Lab. (US)*

[9] *Southern Methodist University, Department of Physics*

Corresponding Author: datao.gong@cern.ch

We present the test results of the ETROC PLL prototype chip. This chip is based on the latest version of ljCDR from the lpGBT project and is designed to test ljCDR in its PLL mode as the clock generator for the CMS Endcap Timing Layer readout chip (ETROC). An automatic frequency calibration (AFC) block with the data protector is implemented for LC-VCO calibration. Triple Modular Redundancy (TMR) is used for all digital circuits to protect against SEUs. The chip's performance has been extensively tested, including SEU testing with heavy ions from 1.3 MeV.cm2/mg up to 62.5 MeV.cm2/mg.

Summary (500 words):

The MIP Timing Detector (MTD) is a new detector planned for CMS during the High-Luminosity Large Hadron Collider (HL-LHC) era. We have been developing the Endcap Timing Readout chips (ETROC) based on a 65 nm CMOS process as the front-end readout electronics of the Endcap Timing Layer, aiming to measure the arrival time impinging particles with a time resolution of 30~40 ps. In this work, the test results of the ETROC PLL prototype chip are discussed. As the clock generator of the ETROC project, the output clock frequencies to the functional blocks in the ASIC are 40 MHz, 320 MHz, 1.28 GHz, and 2.56 GHz, with the demand of the RMS jitter within 5 ps. ETROC PLL must survive 100 Mrad Total Ionizing Dose (TID) and be insensitive to SEE effects.

ETROC PLL adapted the latest version of ljCDR (January 2020), a mature clock synthesis circuit inside the lpGBT project. The ljCDR is fixed in PLL mode with a 40 MHz reference clock and an integrated LC-oscillator at 5. 12 GHz. The CDR mode is disabled. The prescaler comprises the clock generator (division is 2) and the clock transfer circuits (from differential CML to single-ended CMOS). The feedback divider (division is up to 64) generates clocks with proportional frequencies and employs Triple Modular Redundancy (TMR) to project against SEUs. An automatic frequency calibration (AFC) block with the data protector is implemented for LC-VCO calibration. This digital block searches for the optimal VCO capacitor bank when the tuning voltage is overridden. The calibrated data ("Capsel") is stored and refreshed automatically in the data protector to avoid data crashes and loop unlocks due to SEUs.

ETROC PLL, with the layout area of 1.2 mm × 0.7 mm, was implemented in a standalone test chip (2 mm × 1 mm). Additional circuitries include the input reference clock receiver, the output CML drivers, and a generic I2C from lpGBT. Lab tests indicated that with a 40 MHz reference clock, the PLL loop locks instantly at 5.12 GHz after AFC calibration. ETROC PLL provides the random jitter within 2 ps (RMS) for all output clocks. The Time Interval Error (TIE) jitter is measured to be within ± 5 ps (peak-to-peak). During operation, the power consumption of the PLL core is about 60 mW.

ETROC PLL test chip was tested at the Heavy Ion facility in Louvain, Belgium. Heavy Ion irradiation was performed with LETs between 1.3 and 62.5 MeV.cm2/mg. The PLL circuit itself performed stably during irradiation: no unlocks have been identified. Comparing to the old version in lpGBT, the update of the ljCDR improves SEE immunity as expected in the test. The protection function of the AFC protector was verified successfully. The AFC "Capsel" code was protected correctly; thus, no large phase or frequency jump of the PLL loop was observed. Detailed results will be presented at the conference.

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The Gotthard-II readout ASIC and detector system

Authors: Jiaguo Zhang[1]; Marie Andrae[1]; Rebecca Barten[1]; Anna Bergamaschi[2]; Martin Brueckner[1]; Sabina Chiriotti Alvarez[3]; Roberto Dinapoli[1]; Erik Froejdh[1]; Dominic Greiffenberg[4]; Pawel Kozlowski[1]; Markus Kuster[5]; Carlos Lopez-Cuenca[1]; Markus Meyer[1]; Davide Mezza[1]; Aldo Mozzanica[3]; Marco Ramilli[6]; Christian Ruder[1]; Bernd Schmitt[1]; Xintian Shi[1]; Dhanya Thattil[1]; Gemma Tinti[None]; Monica Turcato[7]; Seraphin Vetter[1]

[1] *Paul Scherrer Institut*

[2] *PSI*

[3] *PSI - Paul Scherrer Institut*

[4] *PSI - Paul Scherrer Institute*

[5] *European XFEL GmbH*

[6] *European X-ray Free Electron Laser*

[7] *European XFEL*

Corresponding Author: jiaguo.zhang@psi.ch

Gotthard-II is a charge-integrating microstrip detector developed for experiments and diagnostics at free-electron lasers using hard X-rays of 5 keV–20 keV. Its potential scientific applications include X-ray absorption/emission spectroscopy, energy dispersive experiments, as well as veto signal generation for pixel detectors. The Gotthard-II ASIC has been designed in several optimization steps in order to meet the requirements of the European XFEL, i.e. single photon sensitivity, large dynamic range as well as a high frame rate of 4.5 MHz. The ASIC design and performance will be presented. The detector system as well as the results from beam tests will be discussed.

Summary (500 words):

The scientific and operational requirements at the EuXFEL are very challenging, and have driven the development of the Gotthard-II readout ASIC. Among all detectors for the European X-ray Free-Electron Laser (EuXFEL), Gotthard-II will be the most widely employed detector for energy dispersive experiments which are well suited for the 1-D geometry of Gotthard. The Gotthard-II detector uses a silicon microstrip sensor with a pitch of 50 ⊠m or 25 ⊠m and with 1280 or 2560 channels wire-bonded to 10 or 20 readout ASICs respectively. In both cases, the length of the sensitive area is 64 mm.

The Gotthard-II readout ASIC is shown in figure 1. It features: (a) a high speed, dynamic gain switching pre-amplifier(PRE) allowing to cope with the 4.5 MHz frame rate. The implementation of the dynamic gain switching circuit enables the detection of up to 10ˆ4 X-ray photons of 12.4 keV maintaining single photon resolution with a Signal-to-Noise Ratio (SNR) greater than 10 for low photon fluxes; (b)an on-chip Analog-to-Digital Converter (ADC) and a Static Random-Access Memory (SRAM) capable of storing all digitized images from the 2700 pulses in a bunch train; (c) an on-chip digital comparison circuit to generate veto signals for pixel detectors, for example the Adaptive Gain Integrating Pixel Detector (AGIPD) and Large Pixel Detector (LPD), which are able to record at most 352 and 512 images, respectively, per bunch train. With the veto signals, memories of the pixel detectors storing empty images due to poor interactions between X-ray pulses and samples in user experiments or due to unqualified X-ray pulses can be re-used for the other forthcoming pulses in the same bunch train. In addition, the Gotthard-II ASIC is capable of taking images continuously at a frame rate of up to 495 kHz for synchrotron experiments, the future upgrade of the EuXFEL to CW mode, and potentially for other FELs which are planned to be operated in CW mode, for example LCLS-II and SHiNE.

The Gotthard-II ASIC has been fabricated in UMC-110 nm CMOS technology. The characterization results show a good single-photon resolution at photon energy > 5 keV with a SNR greater than 5, as well as a large dynamic range up to 10ˆ4 12.4 keV X-ray photons. In addition, the noise is below the Poisson limit over the entire dynamic range for 12.4 keV X-ray photons; the non-linearity is found to be better than 1% over the entire dynamic range as well. A summary of the characterization results are shown in figure 2.

The detector system has been designed and extensive experimental tests at the Swiss Light Source (SLS) as well as at Soleil synchrotron have been performed. The results are promising and the performance of the Gotthard-II detector in energy dispersive experiments has been demonstrated as shown in figure 3.

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Front-end hybrid designs for the CMS Phase-2 Upgrade towards the production phase

Author: Mark Istvan Kovacs[1]

Co-authors: Angelos Zografos [1]; Georges Blanchot [1]; Tomasz Gadek [2]; Irene Mateos Dominguez [1]; Adam Erik Hollos [1]

[1] *CERN*

[2] *ETH Zurich (CH)*

Corresponding Author: mark.istvan.kovacs@cern.ch

Sixteen thousand 2S front-end hybrids and twelve thousand PS front-end hybrids will be produced for the CMS Tracker Phase-2 Upgrade. The hybrids consist of flip-chips, passives and mechanical components mounted on a flexible substrate, laminated onto carbon-fibre stiffeners with thermal expansion compensators. In the prototyping phase, several critical issues have been solved to manufacture these complex circuits. Final designs are now reaching readiness for the full-scale production. High-density circuit design practices, lessons learned during the prototyping phase and different improvements for manufacturability will be presented in this contribution.

Summary (500 words):

Ten front-end hybrid variants for the Compact Muon Solenoid (CMS) Tracker Phase-2 Upgrade for the High-Luminosity Large Hadron Collider (HL-LHC) are currently under development. The upgraded Tracker is based on two main types of modules, the strip-strip (2S) and the pixel-strip (PS). The 2S modules contain two parallel strip sensors of (10 × 10) cm2 and two front-end hybrids connected to a service hybrid. The PS modules contain a strip sensor and a macro-pixel sensor of (5 × 10) cm2 and two front-end hybrids connected to a power and a readout hybrid. These modules require state of the art High Density Interconnect (HDI) front-end hybrids assembled with fine pitch flip-chip front-end ASICs, connectors and passives.

All front-end hybrids are using a four-layer build-up topology with micro-vias with copper filled laser drills ranging from 25-50 µm diameter, captured by a pad of 110 µm. These vias are used as via-in-pad to fan-out the 250 µm and 270 µm pitch ASICs on the 2S and PS front-end hybrids respectively. The minimal track width and spacing is 45 µm in the critical routing areas.

The 2S-FEH has more than 6500 interconnections implemented with more than 18000 µvias on 33 cm2, while the PS-FEH has more than 5000 interconnections implemented with 15000 µvias on 24 cm2. The extremely small feature sizes and very high routing density used in these circuits, represent the leading edge of the Printed Circuit Board (PCB) manufacturing technology.

The hybrids are reinforced with carbon fibre laminates with very high stiffness and thermal conductivity. These laminates, due to the cyanate-esther resin system, are highly sensitive to moisture and their Thermal Expansion Coefficient (CTE) is very different from the Hybrids' CTE. Because of this, the usage of carbon fibre stiffeners is bringing additional complexity into the design, handling and manufacturing of these circuits.

The materials used for the circuit fabrication and assembly processes need to be radiation tolerant and of minimum mass to fulfil the tight material requirements of the CMS Tracker. These constraints further challenge the Hybrid manufacturers.

In order to enable and simplify testing of these circuits, the designs implement features as connectors with test-grade mating parts, test points, alignment holes etc. Therefore, the test system has been designed in parallel with the hybrids, so both sides could be adapted appropriately.

The assembled modules from these circuits have been mechanically and functionally validated. Beam tests and functional tests demonstrated the correct operation and compatibility of these hybrids.

In the first part of the contribution, the PS and 2S module baseline designs and the constraints imposed to the hybrids will be introduced. After the introduction, the circuit designs will be presented with emphasis on HDI design techniques, improvements for manufacturability and reliability along with features related to testing. The difficulties related to the usage of the carbon fibre stiffeners along with the adopted processing solutions will be presented. Finally, the modifications and adjustments introduced for the production scale designs will be explained.

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High-accuracy 4D particle trackers with Resistive Silicon Detectors (AC-LGADs)

Authors: Roberta Arcidiacono[1]; Nicolo Cartiglia[2]; Marco Ferrero[1]; Marco Mandurrino[1]; Luca Menzio[1]; Federico Siviero[3]; Valentina Sola[1]; Marta Tornago[1]

[1] *Universita e INFN Torino (IT)*

[2] *INFN Torino (IT)*

[3] *INFN - National Institute for Nuclear Physics*

Corresponding Author: roberta.arcidiacono@cern.ch

Future particle trackers will have to measure concurrently position and time with unprecedented resolutions, approximately 5 microns and 10 ps respectively. A promising good candidate are the AC-LGADs, silicon sensors of novel design, with internal gain and an AC-coupled resistive read-out to achieve signal sharing among pads. This design leads to a drastic reduction of read-out channels, has an intrinsic 100% fill factor, and adapts easily to any read-out geometry. I will present the challenges in the design, the signal formation, recent test results, and the reconstruction techniques that exploit the distributed nature of the signal, including machine learning.

Summary (500 words):

Future accelerator designs call for trackers with extremely good (~5 microns) position and time (~10 ps) resolutions, very low material budget (less than 100 microns equivalent thickness per layer) and low power consumption. In this contribution, I will present the novel concept of silicon detectors with resistive readout, and outline how this design, coupled with the appropriate front-end, allows meeting such stringent requests.

The structure of a resistive silicon detector is sketched in Figure 1 (A) where the key features, (i) a gain implant, (ii) a resistive electrode, and (iii) AC-coupled read-out, are presented. The working principle of such a sensor is (see Figure 1 (B)): the signal, formed on the n+ electrode, spreads to the AC read-out pads that discharge with a time constant that depends on the read-out input resistance, the n+ sheet resistance, and the system capacitance. The pads surrounding the particle hit see a modified version of the original signal. During the propagation on the n+ resistive surface, the signal becomes smaller, wider, with slower leading and falling edges, and is delayed. Figure 1 (C) shows how the signal, generated by a laser beam, is shared among the read-out pads in a 50-micron thick AC-LGAD prototype. Each of the four pads surrounding the hit point sees a fast signal, with an amplitude that depends on its distance from the hit.

In the presentation, I will show how, exploiting the distributed nature of the signal in AC-LGADs, a spatial resolution of less that 5 micron can be achieved for 200 micron-pitch sensors, while also reaching a time resolution of less than 40 ps. These performances have been tested in prototypes, using a laser setup and beam tests with protons.

To exploit the wealth of information carried by the shared signals induced in the read-out pads, we envisage the use of front-end electronics able to sample the signals in multiple points (for example every 300-500 ps) so that many of its features - amplitude, area, width, the slope of rising and falling edges, time of arrival - can be determined. Two points on the leading and trailing edges should be enough to achieve the goal. The samples from each front-end are sent to a reconstruction code concentrator that combines them to estimate the position and time of the hit. This regression problem can be cast in terms of a multi-channel time-varying regression task that uses many inputs to determine two outputs (position and time).
One significant advantage of the AC-LGAD design with respect to every other silicon design is the amount of space available for the electronics. Given that very large pixels (150-300 micron pitch) are germane to the AC-LGAD design, this leads naturally into much more space available for the electronics and much less use of power.

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A Family of Transient Recorder ASICs for Detector Readout

Authors: Holger Flemming[1]; Peter Wieczorek[2]

[1] *GSI Helmholtzzentrum für Schwerionenforschung GmbH*

[2] *GSI Darmstadt, Germany*

Corresponding Author: h.flemming@gsi.de

A set of highly integrated read out ASICs with a common digitising and data aquisition back end but different front ends is currently under development at the GSI electronics department. The concept consists in using an analogue transient recorder stage for an efficient application of the area and power consuming analogue to digital converter. A focus of these ASICs is the read out of detectors with a large dynamic range. Possible applications could be the electromagnetic calorimeter of the PANDA detector or the GEM TPC of the Super-FRS at FAIR.

Summary (500 words):

Two read out ASICs are under development at GSI with different front ends but a common digitizing and data acquisition back end. This backend is based on an analogue transient recorder which is able to store transients of 16, 32 or 64 samples in an analogue memory. After a pulse is detected the transient is fixed and digitized with an on chip 12 bit pipeline ADC. On chip digital processing is able to correct cell to cell variations of the analogue memory and to extract amplitude and time from the digitised transients.

Two different front ends have been developed. A simple input buffer which can be used to receive signals from external front ends e.g. charge sensitive preamplifiers. The other option is a charge sensitive amplifier (CSA) with an adaptive feedback to obtain a very large dynamic range of five orders of magnitude. This CSA design abstain from a resistive feedback for continuous reset but uses a switched reset which is synchronised to the transient recorder.

The ASICs are designed in a 180 nm CMOS technology and integrate the read out electronics for 16 channels. Each four channels share a pipeline ADC. The maximum sampling rate of the transient recorder is 100 MS/s while the ADCs convert the transients with 33 MS/s. Both front ends have been characterised on separate test chips. For the presentation of the results of these characterisations two dedicated abstracts have been submitted. The analogue memory and the ADC were characterised in previous test ASICs as well and the results will be presented in this contribution. The design of both 16 channel prototypes is finished and taped out to the foundry.

Posters ASIC / 144

The Front End and Trigger Unit for an Analogue Transient Recorder ASIC

Authors: Holger Flemming[1]; Peter Wieczorek[2]

[1] *GSI Helmholtzzentrum für Schwerionenforschung GmbH*

[2] *GSI Darmstadt, Germany*

Corresponding Author: h.flemming@gsi.de

A front end and trigger circuit was developed at GSI which is foreseen to be used in a transient recording read out ASIC. It consists of an input buffer with configurable low pass characteristics and a trigger which could be operated as leading edge discriminator as well as switched capacitor trigger which is sensitive to the first derivative of the input signal. The front end was produced on a test ASIC and characterisation results will be presented.

Summary (500 words):

Currently at GSI a set of read out ASICs is under development which is based on an analogue transient recorder backend. To interface this transient recorder with external front ends an input buffer with a hit detection circuit was developed.

The input buffer is a differential buffer with a high input impedance and an amplification of 1. To suppress high frequency noise and to avoid aliasing effects a configurable low pass filter was realized by integrating switchable feedback capacitors.

The hit detection can be operated in two modes. The first operation mode is using a comparator as a simple leading edge discriminator. The threshold voltage is generated by an internal 10 bit digital to analogue converter. The second operation mode is called switched capacitor mode. Here two operation phases controlled by the sampling clock alternate. In phase one the summ of the momentary input voltage and the threshold voltage is stored in a switched capacitor stage. During phase two the input voltage is compared with the output of the SC stage and the comparator decision is taken at the end of clock phase 2.

This way the trigger is sensitive to the first derivative of the input signal and so the sensitivity of the trigger circuit for low frequency interferences e.g. 50 Hz hum is strongly suppressed.

The front end and the hit detection circuit have been produced on a separate test ASIC in a 180 nm CMOS technology. All main characteristics of the front end, the leading edge discriminator and the switched capacitor trigger have been determined and will be presented. For the presentation of the over all transient recorder and digitising ASIC another abstract (#143) was submitted.

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Onchip digital calibrated 2mW 12b SAR ADC with reduced input capacitance

Authors: Hugo Hernandez Herrera[1]; Marco Bregant[2]; Bruno Sanches[3]; Wilhelmus Van Noije[3]

[1] *Federal University of Minas Gerais*

[2] *Universidade de Sao Paulo (BR)*

[3] *EPUSP*

Corresponding Authors: bregant@if.usp.br, hhernan@ufmg.br

We present a 12-bits asynchronous SAR ADC with a low complexity digital on-chip calibration and just 2pF of total array capacitance. The ADC architecture utilizes a redundant weighting switching of 4fF MOM capacitors consuming 14 clock-cycles to complete the conversion. Taking advantage of redundancy, the weights of the MSB capacitors are estimated using the LSB array, thus it is possible to digitally compensate for the mismatch non-linearity directly over the ADC output. The circuit consumes 2mW on a core area of 300um x 500um in 180nm CMOS technology. ENOB of 11.5-bits was post-layout simulated after calibration. Sample characterization is ongoing.

Summary (500 words):

The growing HEP experimental needs are pushing for improved acquisition systems where ADCs with increased resolution are desired, going even beyond 12 bits, with sampling frequencies in the order of tens of MHz. Small area and power consumption are critical specifications since many channels in a single integrated circuit are a trend in HEP detectors. Successive Approximation Register (SAR) has been shown in the last decade to be an adequate architecture to reach these specifications, but for resolutions greater than 10 bits the capacitive array mismatch limits the effective resolution. Using special techniques for the capacitor array layout and increasing the unit capacitor are strategies often used by the designer to reduce the mismatch, but this generally leads to an excessive increase in power and area consumption. Mismatch calibration is a better solution for high-resolution SAR ADC, then chip-by-chip calibration is not necessary, which will reduce the testing costs. Calibration techniques with bearable

complexity and small area performed during the system startup, without external components or signals, is an attractive strategy for the new generation of ASICs for HEP. Mismatch compensating allows us to reduce the array capacitor unit close to the limit imposed by kT/C noise and thereby leading to considerable energy and area reduction. Minimizing the total capacitance of the SAR ADC will relax the speed requirement of the voltage reference buffer and the input signal driver (analog Front-end output), which are commonly power-hungry blocks. In multi-channel ASIC where many ADC instances are integrated in a single chip, many bond-pads and large decoupling capacitance are required for the voltage reference due to the settling error generated by the bondwire inductance during the bit cycling phase. This effect becomes really critical as the sampling frequency increases. Redundant weighting is a simple way to avoid the conversion errors generated by this, with the cost of consuming more clock cycles to complete the conversion. This work presents the design of a 25MHz 12-bits asynchronous SAR ADC with redundant weighting switching of MOM capacitors in 180nm CMOS technology. The total array capacitance is only 2 pF and the whole ADC consumes less than 2mW on a core area of 300 um X 500 um. A new on-chip digital calibration approach that just lasts some microseconds during the chip start-up is presented. The post-layout simulation results show an ENOB of 11.5 bits after calibration. The chip is being produced and experimental results will be available soon.

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A modular and flexible data acquisition system for a cosmic rays detector network

Authors: Guilherme Tomio Saito[1]; Marco Lisboa Leite[1]; Ricardo Menegasso[1]; Rodrigo Estevam De Paula[1]; Marcelo Gameiro Munhoz[1]; Marcel Keiji Kuriyama[1]

[1] *Universidade de Sao Paulo (BR)*

Corresponding Author: guilherme.tomio.saito@cern.ch

We describe a modular data acquisition system developed as the foundation of a cosmic ray detector network. Each detector setup is composed of an independent hardware device that can be controlled and read out through the Internet. This device is designed to acquire and process the signal of up to eight different detector planes. Each of these detector planes uses plastic scintillator slabs that are optically coupled to silicon photomultipliers (SiPM). The main readout is based on a programmable system-on-a-chip (PSoC), a flexible and re-configurable commodity hardware that is used to implement the trigger and timing logic.

Summary (500 words):

The detection of cosmic rays using simple apparatuses for quantitative data-taking has been explored over the years by several initiatives around the world for outreach and experimental High Energy Physics instrumentation teaching. The possibility to connect geographically dispersed stations synchronized by a GPS timing signal allows for a larger detection area suitable for the identification of high-energy cosmic rays showers. In order for such a system to be deployed in a high school or science museum environment (hence for outreach purposes), it must be safe (no flammable gases or high voltages) and ideally low cost, so the network can comprise as many stations as possible. The use of plastic scintillators, SiPMs, and commodity electronic hardware allows the project to fulfill this objective. The readout, timing, and trigger implementation supports a variety of geometries and even other cosmic rays detection methods (Cerenkov) that can be easily deployed in the system by a simple reconfiguration of the hardware. This enables a variety of experiments to be performed with a single design, thus reducing the complexity and costs of the system construction and operation.
Each station is an autonomous hardware (and firmware) unity that detects cosmic ray events and transmits the raw data to the software stack through the Internet. These stations are composed of up to four Frontend modules, in which the scintillators, SiPMs, and the analog section of the electronics are located in separate boards and a Backend module aggregating the trigger, timing, data acquisition, event building, and network communication functions.
The current system uses 4mm x 4mm SiPMs sensors that can be installed as an array of up to four sensors mounted on dedicated PCBs. The SiPMs are attached to a plastic scintillator slab using optical grease. The current design is able to use scintillator slabs as thick as 20mm. An EEPROM device installed in each detection board allows for matching the inventory of built boards with the boards deployed in a

given site. The system is sealed in a light-proof aluminum container and the connection to the readout electronics made by a flat cable. Two LEDs can be pulsed in order to provide a light signal for debugging and calibration.
Each Frontend holds a two-channel voltage amplifier followed by a discriminator circuit. Each channel can sum up the signal from two SiPMs or be ganged together to sum the signal from four sensors when a thicker scintillator slab is used. A minimum detection system can comprise only one Frontend module with two separate channels, and detect the passage of cosmic rays by requiring the coincidence of the two signals.
The Backend module is a single board responsible for the trigger, timing, and data acquisition. The power for all the station and network connectivity is also provided through the Backend. Up to four Frontend modules can be connected to a single Backend module through a commodity HDMI cable in which the four differential lanes are used to carry two digitized SiPM and two LED calibration signals.

Optoelectronics and Links / **147**

A prototype optical link board with redundancy design for the ATLAS Liquid Argon Calorimeter Phase-2 Upgrade

Authors: Xing Huang[1]; Chonghan Liu[2]; Binwei Deng[3]; Datao Gong[2]; Suen Hou[4]; Tiankuan Liu[5]; Hanhan Sun[2]; Jingbo Ye[6]; Li Zhang[None]; Wei Zhang[2]

[1] *Southern Methodist University (SMU)*

[2] *Southern Methodist University*

[3] *Hubei Polytechnic University*

[4] *Inst. of Physics, AS*

[5] *Southern Methodist University (US)*

[6] *Southern Methodist University*

Corresponding Author: tliu@smu.edu

A prototype optical-link board has been developed for the ATLAS Liquid Argon Calorimeter Phase-2 upgrade. The board consists of 24 lpGBT chips and 8 VTRx+ modules and demonstrates the full optical link design of the future front-end board. The board has 22 simplex optical links to transmit detector data, which are emulated in FPGAs and injected through 6 FMC connectors, to the off-detector electronics. The board implements 2 duplex optical links for clocks, control, and monitoring with redundancy design to improve the system reliability. Major functions of the board have been verified.

Summary (500 words):

An optical link system is being developed for the ATLAS Liquid Argon Calorimeter Phase-2 upgrade. A prototype-link board has been designed to evaluate the full optical links of the future Front-End Board (FEB). The prototype-link board consists of 24 lpGBT chips and 8 VTRx+ modules. Two lpGBT chips, two VTRx+ modules, and two pairs of duplex fibers constitute the control links to distribute clocks and Bunch Crossing Reset signals and control the whole FEB. These lpGBT chips and the VTRx+ modules operate in the transceiver mode. The rest 22 lpGBT chips operating in the transmitter mode, 6 VTRx+ modules with only transmitter channels in operation, and 22 simplex optical fibers form data links. The data links transmit detector data, which are emulated in FPGAs and injected through 6 FMC connectors, to the off-detector electronics. The prototype link board has been tested successfully and major functions of the board have been verified.

The prototype-link board demonstrates the redundancy design of control links. First, the clock distribution is redundant. If a downlink is broken (either the VTRx+ is out of order or the fiber is broken), the corresponding control lpGBT can use a clock from another control lpGBT as the reference clock source. Second, the distribution of BCR signals is redundant. Each control lpGBT has 16 electrical link output ports, each driving an ADC ASIC. Two electrical link output signals from two control lpGBT chips are added and multiple dropped to two ADC ASICs to deliver the BCRs signals. The addition is implemented

in a Y-shape resistor network. If a downward control link is broken, its electrical link driver is set up to output a stable low and the driver from another downward control link can still drive the target ASICs. Third, the redundancy design of I2C configuration has been implemented. All ASICs used on the FEB adopt an I2C interface. Each I2C bus has dual controllers, a primary one and a secondary one. If the control link to the primary I2C controller is lost, the secondary controller can take over the bus. At last, all ASICs, including control lpGBT chips and VTRx+ modules, can be reset or power cycled. Though the failure probability of control lpGBTs is lower than the fibers and optical modules, a malfunctioning control lpGBT and VTRx+ may need a reset or a power cycle. The prototype-link board is divided into two symmetric halves called Halves A and B afterward. The control lpGBT on Half A can reset or power cycle all the ASICs, including the control lpGBT and VTRx+, on Half B, and verse versa. All the redundant designs have been verified on the proto-link board except that the BCR distribution. The redundancy design of BCR distribution has been simulated, is being verified, and will be reported in the workshop.

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2.56 Gbps CML transceiver for the data concentrator ASIC

Authors: Arthur Serazetdinov[1]; Eduard Atkin[2]

[1] *National Research Nuclear University MEPhI*

[2] *NRNU MEPHI*

Corresponding Authors: evatkin@mephi.ru, arserazetdinov@mephi.ru

2.56 Gbps CMOS CML-transceiver is presented. The key feature of the design is capability of working with a specific inductive load at both power consumption and radiation tolerance constraints. The transceiver was designed as an interface part of the data concentrator ASIC, intended for the frontend electronics of the time-projection chamber of the MPD experiment at NICA nuclotron (Dubna).

Summary (500 words):

In the course of the experiments carried out at modern spectroscopic facilities, big data flows are expected to be generated from multichannel detectors. Due to the specific radiation environment, data processing is mostly conducted in a remote room. At the same time a high detector granularity leads to the need of high-speed data transfer from the experimental setup to the remote room under constrained power consumption budget.
The paper presents the design results of CMOS building blocks of the CML receiver and transmitter, working at 2.56 Gbps data rate. Both blocks were included in the interface part of the prototype HUBv1 data concentrator ASIC, designed for the frontend electronics of the time-projection chamber of the MPD experiment at NICA nuclotron (Dubna).
The ASIC was prototyped in November 2020 through Europractice in the Low Power (LP) 65 nm CMOS process of TSMC. For the blocks characterization, a test PCB was designed. The chips, received in April 2021, were tested at lab conditions.

The capability of the 2.56 Gbps operation for both CML receiver and transmitter blocks were studied for wire-bonding the ASIC into the CPGA-120 case. The most critical parasitic parameters in such a case are inductances of bonding wires and package pins. These are estimated to be 3-5 nH in total. Mutual inductive coupling between the bonding wires are also of importance. For the two neighboring wires this is equal 0.5 nH. Thus the blocks are required to work with a specific (mostly inductive) load.
According to the accepted concept of the TPC front-end electronics, data transmission to the remote room is provided over a 1 meter light-weight micro-coaxial cable of the AWG36 type having a characteristic impedance of 50 Ohm. At such cable length the effect of high-energy particles on the readout electronics, moved out of the “hot zone”, is reasonably reduced. At the same time due to the low cable attenuation the signal-to-noise ratio is maintained. That allows correct data post-processing. At the receiving end, the unbalanced constructive parasitic capacitance is allowed not more than 3 pF.
Thus, in the course of CML-transceiver design the following objectives are to be ensured: 1. signal integrity and matching of the signal paths, 2. complex inductive-capacitive load blocks operation (bonding

wire inductance of the leads of CPGA-120 package and capacitive load in a remote room at a distance of 1 m), 3. increased radiation tolerance using advanced design techniques, 4. power consumption reduction.
To compromise these requirements, specific system and circuit solutions were used in the course of blocks design. In particular, methods of waveform restoration using high-frequency correcting circuits and filters were applied. Special attention was paid to the integrity of the power rails in the package with a high value of the bonding inductance. The influence of the PCB parasitics mismatch on the signal integrity was considered, and the circuit of an adjustable calibration filter was designed to ensure the matching of the transmission channel.

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Low Noise Charge Sensitive Amplifier - ASIC with Adaptive Gain Setting and Active Reset

Author: Peter Wieczorek[1]

[1] *GSI Darmstadt, Germany*

Corresponding Author: p.wieczorek@gsi.de

The ASIC design group at GSI developed an Amplifier With Adaptive Gain Setting (AWAGS) chip. The input stage based on a folded cascode architecture followed by a single-ended to differential conversion and output buffers. In difference to usual designs the capacitive feedback is divided in five capacitances with different values. Starting with the smallest one the capacitances were adaptively added to the feedback depending on the input charge. This concept allows to measure over a high dynamic range (upto 50pC) with the highest precision in the individual gain setting.
The AWAGS ASIC is produced in a MPW run 2020.

Summary (500 words):

The GSI ASIC design group submitted 2020 the Amplifier With Adaptive Gain Setting (AWAGS) ASIC. This amplifier is forseen as the input stage of the at GSI developed analogue transient recorder for the Super-FRS at FAIR. The input amplifier stage is based on a single-ended folded cascode design with an nMOS transistor at the input. The feedback consists of one fixed capacitance of C_0=400fF and 4 additional capacitances (C_1-C_4) which can be optionally added. The maximum feedback capacitance results to 50pF. For discharging the capacitances an active reset is triggered.

The amplifier stage follows the single-ended to differential conversion. Therefore a fully differential miller OTA
is placed. The needed reference voltage is generated by a 10 bit DAC. The used output buffers are able to drive 5pF
capacitive load in parallel to a resistive impedance of 1k Ohm at 1V differential output swing.

As operation mode a manual mode or the adaptive gain setting mode can be configured. In the manual mode the value of the feedback capacitance has to be programmed once before the measurement. Different to the adaptive gain setting mode were the incoming charge determines the gain of the amplifier and ensures the best precision for each charge measurement up to 50pC.

The programming (e.g manual or adaptive mode, set DAC value) and the data readout is done with the serial interface on chip. In case of the adaptive gain setting mode is selected the information of the active capacitances in the feedback can be read out via the interface.

The preliminary characterization at room temperature of a readout channel get a noise value of 0.3fC and a maximum
input charge of over 50pC. Therefore a dynamic range of more than 150000 results. The measured linearity is better
than 0.5% over the full dynamic range. For the manual gain setting the stable output voltage is reached after 30ns for

a max. amplitude of 1V. In case of using the adaptive gain setting mode the stable output values are present after
max. 140ns if all feedback capacitances are added.

The ASIC is produced in an UMC 180nm CMOS process on an MPW run middle of 2020 and arrived in April 2021 at GSI.
The final results of the characterization will be presented in this contribution.

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The charge sensitivity calibration of the upgraded ALICE Inner Tracking System

Authors: Shiming Yuan[1]; Johan Alme[1]; Dieter Roehrich[1]; Matthias Richter[2]; Markus Keil[3]

[1] *University of Bergen (NO)*

[2] *University of Oslo (NO)*

[3] *CERN*

Corresponding Author: shiming.yuan@cern.ch

The ALICE detector is undergoing an upgrade for Run 3 at the LHC. A new Inner Tracking System is part of this upgrade. The upgraded ALICE ITS features the ALPIDE, a Monolithic Active Pixel Sensor. Due to IC fabrication variations and radiation damages, the threshold values for the ALPIDE chips in ITS need to be measured and adjusted periodically to ensure the quality of data-taking. The calibration is implemented within the O^2 system, thus it runs in the same framework as the normal operation. This paper describes the concept and implementation of the calibration for the upgrade ALICE ITS.

Summary (500 words):

A Large Ion Collider Experiment (ALICE) is one of the four major experiments conducted at the CERN Large Hadron Collider (LHC). The ALICE detector is currently undergoing an upgrade for the upcoming Run 3 at the LHC, and the new Inner Tracking System (ITS) sub-detector is part of this upgrade. The ALICE Inner Tracking System is the innermost sub-detector in the ALICE apparatus. The ITS is responsible of determining the primary vertices, recon- structing secondary vertices, and improving the resolution of the ALICE Time Projection Chamber.It is composed of ~24,000 Monolithic Active Pixel Sensors (ALPIDE chips) distributed on seven concentric cylindrical layers surrounding the beam pipe. The charge threshold of the chips are key parameters for the performance in terms of data uniformity. Due to IC fabrication variations and radiation damages, the threshold values for all the ALPIDE chips in the ITS need to be measured and adjusted periodically to ensure stability in the qual- ity of the data captured. The calibration of the ITS is implemented within the ALICE Online-Offline computing system, thus it runs in the same framework as used during the normal operation. This paper describes the concept and implemen- tation of the calibration method for the upgrade ALICE ITS. The work focuses on the implementation of the raw data parser for calibration, and the S-curve measurement of the charge threshold of ALPIDE chips.

Radiation Tolerant Components and Systems / 151

Design and qualification of the Mu2e electromagnetic calorimeter radiation monitor system

Author: Franco Spinella[1]

Co-authors: Elena Pedreschi [1]; Franco Cervelli [2]; Sergio Ceravolo [3]; Giovanni Corradi [3]; Stefano Di Falco [4]; Eleonora Diociaiuti [3]; Simone Donati [5]; Antonio Gioiosa [5]; Simona Giovannella [3]; Fabio Happacher [3]; Matteo Martini [6]; stefano miscetti [3]; Luca Morescalchi [2]; Daniele Pasciuto [7]; Fabrizio Raffaelli [2]; Ivano Sarra [3]; Alessandra Taffara [2]; Lorenzo Crescimbeni [7]; Nikolay Atanov [8]

[1] *INFN Pisa (IT)*

[2] *INFN PISA (IT)*

[3] *INFN LNF (IT)*

[4] *Universita & INFN Pisa (IT)*

[5] *Universita di Pisa & INFN (IT)*

[6] *Universita' Marconi & INFN*

[7] *Universita' di Pisa & INFN*

[8] *Joint Institute for Nuclear Research (RU)*

Corresponding Authors: franco.spinella@cern.ch, franco.spinella@pi.infn.it

The Mu2e calorimeter and read-out electronics are hosted inside the superconducting magnet cryostat and exposed to an intense flux of ionizing and non-ionizing particles. The performance of a number of components is compromised by radiation damage. This includes the scintillating crystals and silicon photomultipliers (SiPM) whose performance degrades proportionally to both dose and neutrons fluence. The development of a radiation monitor is of vital importance for a reliable detector operation. A system that measures the dose and neutron fluence based on 24 peripheral stations and 4 master units distributed along the detector was built and calibrated.

Summary (500 words):

The Mu2e electromagnetic calorimeter is hosted inside the superconducting magnet cryostat and is made of 1348 undoped CsI crystals distributed in two identical annular matrices (disks). Each crystal is coupled to 2 large area SiPM directly connected to the front-end amplifier. To reduce the cable length and minimize pass-through connections, also the read-out electronics is placed inside the cryostat on the lateral surface of the disks. The high intensity muon beam interaction with the Al target generates a huge amount of ionizing and non-ionizing particles, mainly photons and neutrons to which the calorimeter is heavily exposed. Monte Carlo simulation estimate the crystals and SiPMs will be exposed to a dose of approximately 100 krad and 10E12 neutrons (1 MeV equivalent) in 3 years of Mu2e data taking (including safety factors). Numerous studies report on the effects of the radiation damage due to neutrons on SiPMs performance. These studies show that neutrons with energies of the order of 1 MeV generate a significant increase of noise and leakage current. This could compromise the performance of such devices in an operational environment characterized by high levels of neutron fluence. For the scintillating crystals, radiation damage generates a decrease of the light output and also phosphorescence effects. In both cases, annealing allows a partial recovery. The development of a radiation monitor for the Mu2e calorimeter was deemed essential for a number of reasons, including performing predictive maintenance and studying the origin of the detector performance deterioration. This monitor system was designed, built and named T-RAD. It consists of a variable number of up to 36 sensor cards connected to 4 master cards that collect data and transmit them via optical fiber to the Mu2e DAQ / slow control system. The sensor boards include 3 different devices: a RADfet model Varadis VT01 with a 100 krad full-scale value, a 1-wire DS18S20 temperature sensor and a SiPM used as neutron fluence sensor. The choice of the SiPM for this application was a spin-off of the original R&D for the calorimeter development which required an intense SiPM qualification campaign. We ran a thorough irradiation test campaign at the FNG-ENEA calibrated neutron facility and we determined the real-time variation of the SiPM dark current as a function of neutron fluence. This was done also in a considerable range of temperatures. This allows to directly use the SiPMs selected for the Mu2e calorimeter also as non-expensive and reduced-size sensors. Tests of the sensor cards for the absorbed dose were performed at the Calliope gamma source at ENEA Bracciano. We verified that the VT01 performance is as expected from the Varadis specifications and that the DS18S20 temperature sensor withstands a dose above 200 krad. In the T-RAD monitor system up to 9 sensor boards are connected to 1 master card. The master card is a modified version of the calorimeter digitizing and readout board.
The design, construction and qualification of the T-RAD system are described.

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The new waveform digitizer (DIRAC-V2) for the Mu2e electromagnetic calorimeter at Fermilab

Author: Elena Pedreschi[1]

Co-authors: Franco Cervelli [2]; Sergio Ceravolo ; Gianni Corradi ; Stefano Di Falco [1]; Eleonora Diociaiuti [3]; Simone Donati [4]; Antonio Gioiosa [3]; Simona Giovannella [5]; Fabio Happacher ; Stefano Miscetti [6]; Matteo Martini [7]; Luca Morescalchi [8]; Daniele Pasciuto [9]; Fabrizio Raffaelli [10]; ivano sarra ; Franco Spinella [1]; Nikolay Atanov [11]; Alessandra Taffara [12]

[1] *Universita & INFN Pisa (IT)*

[2] *infn*

[3] *INFN - National Institute for Nuclear Physics*

[4] *Universita di Pisa & INFN (IT)*

[5] *INFN*

[6] *Istituto Nazionale Fisica Nucleare Frascati (IT)*

[7] *INFN e Laboratori Nazionali di Frascati (IT)*

[8] *INFN - Pisa*

[9] *Universita' di Pisa & INFN*

[10] *INFN Sezione di Pisa, Universita' e Scuola Normale Superiore, P*

[11] *Joint Institute for Nuclear Research (RU)*

[12] *INFN PISA (IT)*

Corresponding Author: elena.pedreschi@pi.infn.it

This paper describes design and performance of the new Digitizer ReAdout Controller of the Mu2e electromagnetic calorimeter, which consists of two 674 CsI crystal annular matrices readout by SiPMs. The 20-channel board performs a 200 MHz sampling of the SiPM signals transmitted by the front-end electronics. The operation in the Mu2e harsh environment, with an expected total ionizing dose of 12krad and neutron fluence of 5x1010n/cm2@1MeVeq(Si)/y, 1T magnetic field, level of vacuum of 10-4 Torr made the design challenging. We report on the board architecture, and design, as well as on the results of the prototype qualification and performance test.

Summary (500 words):

Mu2e aims to measure the ratio of the rate of the neutrino-less muon to electron coherent conversion in the field of an aluminum nucleus relative to the rate of ordinary muon capture.. Mu2e will exploit an intense pulsed muon beam and a detector system where the primary components employed to search for the monoenergetic 105 MeV conversion electron signal are the straw tracker and the electromagnetic calorimeter. The calorimeter provides an additional rejection factor of 200 on cosmic muons, a tracker independent trigger and improve pattern recognition quality and efficiency for the electron tracks. The expected calorimeter performance are $\sigma E/E < 10\%$, $\sigma(t) < 500$ps and a position resolution < 1cm. The calorimeter employs 1348 undoped CsI crystals, arranged in two annular matrices (disks) located inside the detector cryostat. Each crystal is coupled to two SiPMs arrays connected to the Front End Electronics. A mezzanine board controls a group of 20 Amp-HV chips. Groups of 20 differential signals are sent to the Digitizer ReAdout Controller board (DIRAC-V2). To limit the number of pass-through connectors and the length of the cables, the readout and digitization electronics will be located inside the cryostat .This choice has made the DIRAC-V2 design challenging due to the harsh operational environment: neutron fluence 5x1010 n/cm2 @ 1 MeVeq (Si)/y, TID 12 krad, 1T magnetic field, which have required an extended campaign of tests to qualify the employed electronic components, and a level of vacuum of 10-4 Torr, which has required the design of a dedicated cooling system for power dissipation. The DIRAC-V2 is an evolution of the DIRAC-V1 and the improvements derive from the qualification campaign and performance tests carried out on DIRAC-V1. The DIRAC-V2 core is a large FPGA (Polarfire MPF300) with configuration cells immune to Single Event Upset. Data coming from 10 ultralow-power double channels 12-bit 250 MHz ADCs (ADS4229) are handled by the FPGA. Sparsified and compressed data form packets that are optically transmitted through a fiber transceiver (VTRx) to the Mu2e event builder using a custom protocol. The board was required to pass different qualification tests: Total Ionizing Dose up to 12 krad, Single Event Upset, Neutron Displacement Test and magnetic field. An ultra-low noise jitter cleaner (LMK04828) provides a high-performance clock to the FPGA and ADCs, with the option to fine tune relative phases with an accuracy up to 100 ps. The power distribution is handled by 3 DC-DC converters (LMZM33606) and 6 LDO (MIC69502) to provide rails to the analog components. The

DIRAC-V2 board follows a custom form factor (233 mm x 165 mm x 2.127 mm), realized in FR408-HR, and relevant lines controlled impedance. To validate the DIRAC-V2 analog section in terms of dynamic, SNR, bandwidth, and linearity, we assembled a full system chain (one CsI crystal, two FEE board, one mezzanine board and the DIRAC-V2 prototype) for a cosmic ray test. The test demonstrated that the DIRAC-V2 analog section performs satisfactorily: the signals shapes are as expected from the Monte Carlo simulation, and the time resolution is 350 ps

Posters Production, Testing and Reliability / 154

A system test platform for the CERN power converter control electronics

Authors: Gabriela Cabrera Castellano[1]; Robert Grimmer[1]; Peter Haynes[1]; David Nisbet[1]

[1] *CERN*

Corresponding Authors: peter.haynes@cern.ch, gabriela.cabrera@cern.ch, robert.grimmer@cern.ch

The power converters at CERN deliver a broad range of complex functionalities to assure the correct magnetic field throughout the beam acceleration cycle. The power converter controls are composed of remotely programmable electronics, however such flexibility is also vulnerable to regression that requires thorough testing. Further, testing requires a significant investment in infrastructure to allow systems capable of supplying up to 10MW, 100kV and 100kA to be validated. This paper describes a system test platform using continuous integration techniques and hardware-in-the-loop modelling to validate the controls before deployment.

Summary (500 words):

The power converters at CERN deliver a broad range of complex functionalities to assure the correct magnetic field throughout the beam acceleration cycle. These complex functionalities are diverse, for example to assure a precision of the regulated current is better than 100 parts per million, or to minimise the consumed power when delivering up to 31 different current functions on a pulse to pulse modulation basis.
To be capable of delivering such functionality, by design the power converter controls must be remotely programmable electronics. The controls platform is composed of both microprocessors and DSPs running software, and FPGAs running firmware. In total there are more than 100 different compiled codes that must be deployed in different combinations to the accelerator power converter control systems. Such flexibility is vulnerable to regression that requires thorough testing, however this is in itself a challenge, as the target systems vary in size and can be rated up to 10MW, 100kV and 100kA. Traditionally thorough lab testing has been made before final installation and commissioning, however this model is no longer adequate for platforms that can now change even after operation has begun.
To meet the challenge of validating the electronics controls, a platform that can test the electronics controls using continuous integration techniques has been developed. The python code to control the tests is running in a gitlab repository from which the continuous integration and continuous deployment (CI/CD) environment is configured. In particular, to meet the challenge of testing large power systems, models of the systems have been deployed in a hardware-in-the-loop (HIL) platform. These models replicate the behaviour of the power plant when interfaced to the controls platform, thus allowing the controls behaviour to be explored and validated.

This paper describes a system test platform using continuous integration techniques and hardware-in-the-loop modelling to validate the controls before deployment. The hardware and software technologies required for such a platform will be described, and early results of the testing will be presented.
By using continuous integration techniques, and hardware in the loop technology, the ability to validate code for regression can be made whenever a new code compilation is made, or before code deployment. Further, this is possible without the cost of maintaining a high power test platform for a wide range of equipment.

Posters Trigger / 155

The NA62 liquid krypton electromagnetic calorimeter fast readout implementation and data taking performances

Authors: Roberto Ammendola[1]; Andrea Salamon[1]; Giovanni Paoluzzi[2]

Co-authors: Riccardo Aliberti [3]; Mattia Barbanera [4]; Marco Bizzarri [5]; Vincenzo Bonaiuto [1]; Augusto Ceccucci [6]; Bruno Checcucci [7]; Nico De Simone [6]; Riccardo Fantechi [4]; Luca Federici [8]; Adolfo Fucci [1]; Matteo Lupi [6]; Karim Massri [6]; Marco Mirra [9]; Christopher John Parkinson [10]; Elena Pedreschi [4]; Roberto Piandani [11]; Mauro Piccini [12]; Giuseppe Ruggiero [13]; Vladimir Ryjov [6]; Antonino Sergi [14]; Dario Soldi [15]; Franco Spinella [4]; Stefano Venditti [6]; Michal Zamkovsky [16]; Fausto Sargeni [1]; Gaetano Salina [17]

[1] *INFN e Universita Roma Tor Vergata (IT)*

[2] *INFN Roma Tor Vergata*

[3] *Johannes Gutenberg Universitaet Mainz (DE)*

[4] *Universita & INFN Pisa (IT)*

[5] *Universita e INFN (IT)*

[6] *CERN*

[7] *Universita e INFN, Perugia (IT)*

[8] *Universite Catholique de Louvain (UCL) (BE)*

[9] *Universita e sezione INFN di Napoli (IT)*

[10] *University of Birmingham*

[11] *University of Chinese Academy of Sciences (CN)*

[12] *INFN - Sezione di Perugia (IT)*

[13] *Lancaster University (GB)*

[14] *INFN e Universita Genova (IT)*

[15] *Universita e INFN Torino (IT)*

[16] *Charles University (CZ)*

[17] *Istituto Nazionale di Fisica Nucleare*

Corresponding Author: roberto.ammendola@roma2.infn.it

The NA62 experiment at the CERN SPS aims to measure the branching ratio of the very rare kaon decay $K^+ \to \pi^+\nu\bar{\nu}$. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. Along with the trigger data sent to the L0 trigger processor, readout data is collected to be sent to L1 software trigger level. We present the novel implementation of the readout data collection and forwarding system in the multiple layers of the calorimetric trigger structure. We will also present the performance evaluation of the new system that will be measured in the incoming data taking.

Summary (500 words):

The NA62 experiment aims to measure the very rare kaon decay $K^+ \to \pi^+\nu\bar{\nu}$, collecting O(100) events with a 10% background to make a stringent test of the Standard Model and deepen the knowledge of the CKM matrix. The $K^+ \to \pi^+\nu\bar{\nu}$ decay is highly suppressed, well known from the theoretical standpoint and very sensitive to many New Physics models. The Standard Model branching ratio prediction for $K^+ \to \pi^+\nu\bar{\nu}$ is $(8.4 \pm 1.0) \times 10^{-11}$.

The calorimeter level 0 trigger is used to suppress one of the main backgrounds, the $K^+ \to \pi^+\pi^0$ decay, and to select events with a π^+ in the final state. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. It prepares time-ordered lists of reconstructed clusters together with the arrival timestamp, position, and energy measurements of each cluster. It also provides trigger decisions based on complex combinations of energy and cluster multiplicity. The main parameters of the trigger processor are the high design hit rate (30 MHz) and the required single cluster time resolution (1.5 ns). The calorimeter trigger processor is a parallel system composed of 37 boards, 111 mezzanines and 221 programmable devices housed in three 9U crates.

Until now, only trigger data was available to L0 trigger processor, while readout data was not used at L1 software trigger layer. The implementation of the readout datapath towards L1 has now been deployed, in order to enhance data acquisition efficiency and refine trigger decision between hardware L0 and software L1 trigger layers.

At the early stage in the first hardware layer, the trigger signal arriving from L0 Trigger processor is used to collect timestamps of the triggered data, calculated with proper delay offset. Readout data from CREAM modules are stored in proper buffers (separated from trigger data line), and data timestamps are matched within a programmable window. Selected data is then forwarded and reduced at the higher levels, using the same data path as the trigger data lines with proper traffic priority rules; this expedient allows using completely the same hardware already deployed, except from a mezzanine card at the second hardware layer, implementing dual Gbit ethernet interface that has been added later. Data packets are thus sent to software trigger layers in order to enhance data selection.

The new fast readout system will be put on-line in the experiment with the beginning of 2021 data taking run. Performance measurement will be carried out, in order to check readout and trigger data integrity with increasing beam intensity.

Posters ASIC / 157

DIAMASIC: A multichannel front-end electronics for high-accuracy time measurements for diamond detectors

Authors: Abderrahmane GHIMOUZ[1]; Fatah Ellah Rarbi[2]; Olivier ROSSETTO[2]; Fatah Ellah Rarbi[3]

[1] *Univ. Grenoble Alpes, Grenoble INP, CNRS, LPSC-IN2P3*

[2] *Univ. Grenoble Alpes, CNRS, LPSC-IN2P3, Grenoble INP*

[3] *Centre National de la Recherche Scientifique (FR)*

Corresponding Authors: fatah-ellah.rarbi@cern.ch, ghimouz@lpsc.in2p3.fr, rarbi@lpsc.in2p3.fr

This paper describes the design and testing results of an 8 channels preamplifier-discriminator circuit based on a resistive feedback Transimpedance Amplifier architecture and a Leading-Edge Discriminator stage for fast high-accuracy time measurement systems. The circuit has been designed in a 130 nm CMOS technology. It is intended to be used as a Front-End-Electronics for measuring the Time Of Flight using diamond detectors. The size of the chip is 1.27x1.22mm² and the total power consumption of one channel is 1.5mW with a power supply of 1.2V. Testing results shows a timing jitter of about 80ps for a 10fC input charge pulse.

Summary (500 words):

Recently, Chemical Vapor Deposition (CVD) Diamond detector offers an attractive alternative to silicon detector due to its outstanding performances such as the higher charge mobility (2200cm2/Vs and 1600cm2/Vs for electron and hole respectively), low leakage current (high bandgap of 5.45eV) and radiation hardness capabilities. This type of diamond detectors is used as solid-state ionization chambers: it means that the detector can be modeled as a current source with both a capacitor and a resistor in parallel of each other. The resistor is neglected because it is so high to be considered (several Tera Ohms). The goal of this project is to measure the Time Of Flight (TOF) of particles with a resolution of tens of picosecond using CVD double-side stripped metallized diamond detector. This leads to some challenges in the design of the dedicated Front-End readout Electronics (FEE): large bandwidth and low noise. The proposed circuit is an 8 channels preamplifier-discriminator circuit based on a resistive feedback Transimpedance Amplifier (TIA) architecture and a Leading-Edge Discriminator stage. The TIA is sized using the gm over id methodology which is suitable for low power applications. In our case, the timing resolution of the system is estimated as the quadratic sum of three main parameters: The Time-To-Digital Converter (TDC) resolution that is related to its topology, the time walk of the discriminator stage which appears when signals with same rise time but different amplitude are detected, and the timing jitter of the front-end stage. It was already shown that the time walk can be corrected using post-processing techniques as the time over threshold method or the constant fraction discrimination method. The timing jitter of the front-end stage depends on both the bandwidth and the noise of the

amplifier stage. It is deemed to be the most critical parameter which needs to be reduced in order to guarantee the best timing resolution. Thus, during this study, the timing jitter error is considered as the criteria of time resolution. For this, a more accurate model of the circuit is proposed adding the interconnection inductances of bonding wires between the detector and the FEE. We developed as well a new mathematical model of the timing jitter capable of obtaining the optimum values of the input impedance and the bandwidth. The model is implemented in MATLAB Simulink and compared to electrical simulations and testing results to demonstrates the accuracy of the new design approach and the timing jitter estimation equation. Using the proposed methodology, we could achieve a measured timing resolution of about 80ps with an input charge pulse of 10fC and a total power consumption of only 1.5mW for a single channel.

Optoelectronics and Links / 158

40 Gbps optical transceiver for particle physics experiments

Authors: Xing Huang[1]; Binwei Deng[2]; C.-P. Chao[3]; S.-W Chen[4]; Datao Gong[5]; Suen Hou[6]; Guangming Huang[7]; C.-Y Li[4]; Chonghan Liu[5]; Tiankuan Liu[5]; Hanhan Sun[8]; Quan Sun[9]; Jingbo Ye[5]; Li Zhang[8]; Wei Zhang[8]

[1] *Southern Methodist University (SMU)*

[2] *Hubei Polytechnic University*

[3] *APAC Opto Electronics Inc*

[4] *APAC Opto Electronics Inc.*

[5] *Southern Methodist University*

[6] *Academia Sinica*

[7] *Central China Normal University*

[8] *Southern Methodist University & Central China Normal University*

[9] *Fermi National Accelerator Laboratory*

Corresponding Author: xingh@mail.smu.edu

QTRx is an optical transceiver for particle physics experiments. The transmitters, each at 10 Gbps, are based on QLDD and 1x4 VCSEL array. The receivers, with data rates between 2.56 Gbps and 10 Gbps, are based on QTIA and 1x4 photodiode array, GaAs or InGaAs. QTRx is 20 mm × 10 mm × 5 mm and couples to an MT fiber connector. Preliminary tests indicate that QTRx meets design data rates with a power of 124 mW per Tx channel at 10 Gbps and 72 mW per Rx channel at 2.56 Gbps. More tests, including irradiation, will be carried out.

Summary (500 words):

QTRx is a 4-Tx, and 4-Rx optical transceiver developed for particle physics experiments. The Tx channels, each at 10 Gbps, are based on QLDD (quad laser diode driver), an ASIC resulting from previous developments of cpVLAD [1], and a 1x4 VCSEL array. The Rx channels are based on QTIA (quad transimpedance and limiting amplifier) and a 1x4 photodiode (PD) array of either GaAs or InGaAs. QTIA is optimized for operations at 2.56 and 10 Gbps per channel. Each channel of QLDD has a charge pump to address the possible increase of VCSEL forward voltage in radiation. QTIA is at the R&D stage with different PD biasing structures in each channel to study options for mitigating radiation-induced degradation in PDs. Details about QTIA are reported separately. Each Tx or Rx channel can be disabled via I2C block to save power. Both dies of QLDD and QTIA are 2 mm × 2 mm, fabricated in a 65 nm CMOS technology.

QTRx is 20 mm (L) × 10 mm (W) × 5 mm (H) and couples to an MT fiber connector. The electrical interface is a 40-pin connector for the moment and may be changed in the future. All components of QTRx are on one side of the PCB, leaving the other side to be coupled to cooling plates if needed.

The preliminary tests indicate that QTRx meets design data rates. The Tx optical eye has an RMS jitter of 4 ps. The rise and fall times are around 35 ps. The preliminary sensitivity of the receiver -17 dBm of the input optical power operating at 2.56 Gbps. The electric power consumption is 124 mW per Tx channel at 10 Gbps and 72 mW per Rx at 2.56 Gbps. A full set of evaluations, including performance in radiation, are planned for the coming months. We will present the results we have at the workshop.

Reference:

[1] Huang, X., D. Gong, D. Guo, S. Hou, G. Huang, S. Kulis, C. Liu et al. "A novel quad-channel 10 Gbps CMOS VCSEL array driver with integrated charge pumps." Journal of Instrumentation 15, no. 12 (2020): T12004.

Posters Trigger / 160

Progress report on the online processing upgrade at the NA62 experiment

Authors: Alessandro Lonardo[1]; Andrea Biagioni[2]; Andrea Ciardiello[3]; Dario Soldi[4]; Francesca Lo Cicero[5]; Francesco Simula[6]; Gianluca Lamanna[7]; Luca Pontisso[1]; Matteo Turisini[1]; Mauro Raggi[8]; Ottorino Frezza[1]; Paolo Cretaro[9]; Paolo Valente[1]; Piero Vicini[10]; Roberto Ammendola[11]; Roberto Piandani[12]

[1] *Sapienza Universita e INFN, Roma I (IT)*

[2] *INFN*

[3] *Università Sapienza di Roma, Italy*

[4] *Universita e INFN Torino (IT)*

[5] *INFN, Sezione di Roma, Italy*

[6] *Istituto Nazionale di Fisica Nucleare - sezione di Roma 1*

[7] *Universita & INFN Pisa (IT)*

[8] *LNF INFN*

[9] *INFN - National Institute for Nuclear Physics*

[10] *INFN Rome Section*

[11] *INFN e Universita Roma Tor Vergata (IT)*

[12] *University of Chinese Academy of Sciences (CN)*

Corresponding Author: matteo.turisini@cern.ch

In 2021 the NA62 experiment at CERN is restarting data taking with upgraded instrumentation. In this framework we present the commissioning test of the new L0 trigger processor offering enhanced bandwidth, updated interconnection technology and increased logic capabilities with respect to its predecessor. We also present the latest performances of two computing-intense additional components dedicated to the online processing of RICH detector information: a ring reconstruction algorithm on GPU for electron identification and a fast neural network developed with HLS tools on FPGA for ring multiplicity counting. Finally we evaluate the impact of introducing such features in the TDAQ system.

Summary (500 words):

NA62 is a fixed target experiment at CERN aiming for precision measurements of the rarest decay modes of the K+ meson.
The apparatus is 270 meters long and composed by many sub-detector modules dedicated to particles identification and kinematics reconstruction.
The online data selection is managed by a two-levels trigger system: the lowest (L0) is implemented in hardware and constrained by a 1 millisecond latency,
the other is software operated on a dedicated PC farm.
Among the most challenging requirements there is a 10 orders of magnitude background rejection and a peculiar beam structure consisting of ~5 seconds long spill populated by 3×10^12 particles.

The L0 trigger processor adopted so far (L0TP) was implemented on a Tera-sic DE4 board equipped with eight 1GbE links; it proved substantially robust but meanwhile technology has advanced.
The system has now been ported onto a more recent platform, a Xilinx VCU118 board featuring 10GbE links.
We present a comparison between the old and the new system (L0TP+) in realistic conditions in lab and in beam tests.

The increased resources on L0TP+ allow for better integration with the Run Control of the experiment and addition of new features for online detectors data processing.

One of the inputs of L0TP is the Ring Imaging Cherenkov (RICH) detector data, requiring a maximum 10 MHz throughput processing capability.
No track information is available and the current solution is based just on hit multiplicity and temporal clustering.
Two online systems were developed to refine the logic dedicated to process the RICH data stream.

The first one is a neural network for rings counting implemented on FPGA.
The model consists of a fully connected architecture with less than 150 neurons; it was trained using the Tensorflow framework, using Qkeras for weights quantization.
The FPGA code is generated using High Level Synthesis (HLS) techniques and reaches about 80% test accuracy when deployed on device.
We present bench test results that demonstrate the effectiveness of this approach in satisfying the high demanding timing requirements of NA62-RICH i.e. a throughput of 10 million event classifications per second.
We highlight the innovative aspects of the workflow together with details related to the reduced numerical representation on FPGA.
Thanks to the small footprint on the VCU118 resources the module could be integrated in L0TP+.

A second system was developed for geometrical reconstruction of the rings on a Nvidia GPU board and has been tested on site in 2018 experiment runs.
The key component enabling GPU for online usage is NaNet, an FPGA-based Network Interface Card that exchanges data with the GPU memory without host CPU supervision.
We preliminary assess here the system performance in electron identification during the first months of the 2021 NA62 data taking.

In conclusion the trigger scenario in HEP is evolving thanks to new distributed computing paradigms based on heterogeneous nodes and low latency interconnects.
The L0TP+ of NA62 enriched with parallel and specialized systems is an example of this trend that more and more will take hold in near future.

Radiation Tolerant Components and Systems / 161

Low dose rate irradiation of the RD53A chip with Kr-85 beta source

Author: Aleksandra Dimitrievska[1]

Co-authors: Timon Heim [1]; Maurice Garcia-Sciveres [1]; Simone Pagan Griso [1]

[1] *Lawrence Berkeley National Lab. (US)*

Corresponding Author: aleksandra.dimitrievska@cern.ch

To test the performance of the future pixel readout chip in the harsh High Luminosity LHC (HL-LHC) environment, an irradiation experiment has been setup with gaseous Kr-85 beta source with dose rate of about 7 rad/s. This setup was designed to emulate as closely as possible operation in the HL-LHC conditions of the ATLAS detector inner layer, including temperature, radiation, and continuous electrical operation. The low dose rate irradiation setup has been running since September 5th 2018 at a temperature of -15 degrees Celsius. The first results will be presented with a 500 Mrad total dose received.

Summary (500 words):

The High Luminosity LHC (HL-LHC) will reach a factor of five larger instantaneous luminosity than the current LHC, enabling the ATLAS and CMS experiments to achieve the full physics potential of the LHC beyond 2025. With the luminosity, the radiation levels are also increasing. The current tracking detectors will be completely replaced with a new generation pixel detector. A new readout chip for

the upgraded pixel detector has to meet specifications after 1 Grad total dose received in the HL-LHC conditions. A prototype of the pixel readout integrated circuit has been designed by the RD53 Collaboration in 65nm CMOS technology. To test the performance of the RD53A chip in the harsh HL-LHC environment, an irradiation experiment has been setup with gaseous Kr-85 beta source. The total dose of the Kr-85 source is estimated to about 7 rad/s which roughly corresponds to the expected conditions at the HL-LHC. From a single transistor irradiation experiments it is observed that for the same integrated dose, the radiation damage is worse with low dose rate compared to the high dose rate. Since an accurate scaling from a high dose rate measurements to low dose rate has not beet yet developed, the low dose rate irradiation provides an accurate answer about the survivability of these chips in the real conditions of the detector. The SLIPPER (SLow Irradiation of Phase-II PixEl Readout) setup was designed to emulate as closely as possible operation the HL-LHC inner layer of the ATLAS detector, including temperature, radiation, and continuous electrical operation. The low dose rate irradiation started on September 5th 2018 and it is been running for 2.5 years now. The chip is running all the time at a temperature of -15 degrees Celsius. The first results will be presented with a 500 Mrad total dose received. The effects of irradiation form a high and low dose rate are compared.

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Investigation of Radiation-Induced Effects in a Front-end ASIC designed for Photon Counting Sensor Systems

Authors: Vlad-Mihai Placinta[1]; Lucian Nicolae Cojocariu[2]; Florin Maciuc[2]

[1] *Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH RO)*

[2] *Horia Hulubei National Institute of Physics and Nuclear Enginee*

Corresponding Author: vlad-mihai.placinta@cern.ch

This work outlines the measurements done to evaluate the second SPACIROC generation in ionizing radiation environments, i.e., particle beams: ions, protons, and X-rays. The SPACIROCs are front-end ASICs designed for the readout requirements of photomultiplier technologies like: SiPMs, MaPMTs. Several radiation-induced effects were observed but they proved to be benign application-wise. The threshold LET for SEUs was measured and two cross-sections for different LETs are provided. At extremely high dose rates (~100 rad/s) and TID above 50 krad proton/X-ray induced TID effects were observed, however a room-temperature annealing process was determined to mitigate the harmful TID effects in 24 hours.

Summary (500 words):

The Spatial Photomultiplier Array Counting and Integrating Readout Chips (SPACIROC) are photodetector readout ASICs designed initially for the JEM-EUSO cosmic ray observatory. The second generation SPACIROC was a prototype version designed to evaluate the performance of several internal blocks before adopting the final design. The SPACIROC inherits the analog blocks from the third generation of Multi-Anode Readout Chip (MAROC3) ASICs, which are front-end ASICs proposed as backups for the LHCb-RICH MaPMT sensor readout. An irradiation campaign was organized to investigate the reliability of the SPACIROC2 in a radiation environment which emulates key characteristics of ISS environment or any LHC accelerator experiment. The SEE rates and the TID effects were measured using particle beams from various facilities: ions at LNL (Italy); 200 MeV protons at PSI (Switzerland); 35 MeV protons at Juelich Research Center (Germany); and 8-50 keV X-rays at University of Padova (Italy).
Two species of ions, 16O and 28Si -with LET values of (2.8 ± 0.3) MeVcm2/mg and (8.6 ± 0.8) MeVcm2/mg- were used to test the chips and to measure SEE rates for different beam-inclination angles and with various fluence values, up to (1.5 +/- 0.3) · 107 ions/cm2. Two values of SEU cross-section in configuration registers were measured: (☒”1.6” ☒“*-1.4” ^”+4.18”*) · *10-6 cm2/device for a LET of (8.6 ± 0.8) MeVcm2/mg and (☒”0.5”*☒“-0.34” ^”+0.6”) · 10-5 cm2/device for a LET of (11.2 ± 1.1) MeVcm2/mg. The SEU-threshold value was measured to be between (4.4 ± 0.4) MeV cm2/mg and (8.6 ± 0.8) MeVcm2/mg. No SEL was observed, and the few SEUs were mitigated by a reconfiguration of the device.
Using protons, and at very high and unrealistic dose rates, failures were observed in various build-in blocks, e.g., DACs. Increased leakage currents were observed due to TID, which were highly visible in the digital component of the ASIC. One sample was irradiated with 35 MeV protons in three runs of 50 krad (Si) each (total TID ~150 krad), which corresponds to a total fluence of (6.9 ± 0.33)·1011 protons/cm2.

Three chips were irradiated with 200 MeV protons, each being subject to a TID of ~100 krad, and a fluence of about (2 ± 0.3) · 1012 protons/cm2. It was observed that the build-in DACs start to lose their linearity at a TID threshold between 80 and 100 krad. After 100 krad the DACs suffer complete failure. All previous TID effects were fully recovered through a rapid annealing process at room temperature within 24 hours to a few days, with no evidence of permanent effects or long-term effects even though one sample was irradiated with a cumulative TID of ~250 krad. No configuration SEUs were observed during irradiation with 35 MeV protons beam, though this measurement was for only one chip and smaller fluence, hence less conclusive. One chip was tested with X-Rays and a TID of ~117 krad and this measurement confirmed the TID effects observed in the proton-beam tests, separating these cumulative effects from the SEE class.

Systems, Planning, Installation, Commissioning and Running Experience / **163**

Prototype Design of Timing and Fast Control in the CBM experiment

Author: Vladimir Sidorenko[1]

Co-authors: Steffen Baehr [1]; Walter Mueller [2]; Jürgen Becker [1]

[1] *Karlsruhe Institute of Technology*

[2] *Unknown*

Corresponding Author: vladimir.sidorenko@kit.edu

The Compressed Baryonic Matter (CBM) experiment is designed to handle interaction rates of up to 10 MHz and up to 1 TB/s of raw data generated. With free-streaming data acquisition in the experiment and beam intensity fluctuations, it is expected that occasional data bursts will surpass bandwidth capabilities of the Data Acquisition System (DAQ) system. In order to preserve event data, the bandwidth of DAQ must be throttled in an organized way with minimum information loss. The Timing and Fast Control (TFC) system provides a latency-optimized datapath for throttling commands and distribute a system clock together with a global timestamp.

Summary (500 words):

Timing and Fast Control (TFC) system is being developed for the Compressed Baryonic Matter (CBM) experiment to orchestrate the data acquisition process and prevent the Data Acquisition (DAQ) network from congestion. TFC system has a dual purpose in the experiment: it distributes the experiment-wide system clock along with the 64-bit global timestamp and provides the datapath for DAQ bandwidth throttling. The need for a throttling mechanism arises from the expected beam intensity fluctuations that will occasionally cause data generation beyond processing and buffering capabilities of the DAQ system.
Experimental data in CBM is generated in radiation-hard Front-End Boards (FEB) and transmitted over e-links to GBTx ASICs. These ASICs, in turn, forward the collected data to the Common Readout Interface (CRI) boards over optical GBT links at 4.8 Gb/s rate. Up to 200 CRI boards constitute the entry stage of the First-Level Event Selector (FLES) network, where event reconstruction takes place.
The number of CRI boards in the DAQ system defines the scalability requirement for the TFC system, which must serve up to 200 endpoints. In order to ensure scalability and centralized architecture, TFC network has a hierarchical topology with Master, Submaster and Endpoint nodes defined. The nodes in the TFC network are connected with 4.8 Gb/s bi-directional optical links and the data flow is organized in short messages. Whereas Master and Submaster nodes are based on dedicated FPGA boards, each Endpoint is an FPGA core integrated into CRI firmware.
In the current prototype design of the TFC system, the 40 MHz system clock and the global timestamp are propagated from the Master to Endpoints in a flooding fashion. When received from the “upstream” link, both the clock signal and the timestamp are reused locally by Submasters and forwarded over each “downstream” link. Since the 40 MHz clock is extracted from the higher transport frequency, dedicated logic eliminates phase uncertainty introduced by clock division in each node.
Synchronization and fast control traffic will be sharing the network and have different latency requirements, which drives the need for traffic prioritization. In TFC, this is handled by request-based access to optical links, where request arbitration is done with a priority encoder.

In this paper, a prototype of the TFC system will be presented. Its latency and synchronization properties are studied on the target BNL-712 FPGA platform and a Xilinx Ultrascale+ evaluation board.

Trigger / **164**

FPGA-based real-time data processing for accelerating reconstruction at LHCb

Authors: Federico Lazzari[1]; Andrea Contu[2]; Giovanni Bassi[3]; Giovanni Punzi[4]; Giulia Tuci[4]; Luca Giambastiani[5]; Marco Sticchi[4]; Michael J. Morello[6]; Mirco Dorigo[7]; Riccardo Fantechi[4]; Wander Baldini[8]

[1] *Universita di Siena & INFN Pisa (IT)*

[2] *INFN*

[3] *SNS & INFN Pisa (IT)*

[4] *Universita & INFN Pisa (IT)*

[5] *Universita e INFN, Padova (IT)*

[6] *SNS and INFN-Pisa (IT)*

[7] *INFN Trieste*

[8] *Universita e INFN, Ferrara (IT)*

Corresponding Author: federico.lazzari@cern.ch

In Run-3 beginning in 2022, the LHCb software trigger will start reconstructing events at the LHC average crossing rate of 30 MHz. Within the upgraded DAQ system, LHCb established a testbed for new heterogeneous computing solutions for real-time event reconstruction, in view of future runs at even higher luminosities.

One such solution is a highly-parallelized custom tracking processor ("Artificial Retina"), implemented in state of the art FPGA devices connected by fast serial links.

We describe the status of the development of a life-size demonstrator system for the reconstruction of pixel tracking detectors, that will run on real data during Run-3.

Summary (500 words):

With the slowdown of Moore's law, HEP experiments are looking at heterogeneous computing solutions as a way to face ever-increasing data flows and complexity. LHCb is on the frontier of these developments due to its specific physics needs, calling for the full software reconstruction of events in real-time at the LHC average rate of 30 MHz (40 Tb/s), already in the next physics run starting in 2022. LHCb has already adopted a GPU-based solution for HLT1 for the next run, and is further researching solution for its future Upgrade-II, with a significant increase of luminosity by a factor 5÷10. To this purpose, a coprocessor testbed has been established, to allow parasitical testing of new processing solutions in realistic DAQ conditions during the 2022 run.

One such solution under development is a highly-parallelized custom tracking processor ("Artificial Retina"). The "Artificial Retina" architecture takes advantage of FPGAs parallel computational capabilities, by distributing the processing of each event over an array of FPGA cards, interconnected by a high-bandwidth (~15 Tb/s) optical network. This is expected to allow operation in real-time at the full LHC collision rate, with no need for time-multiplexing or extra buffering thanks to its brief latency (<1 μs).

This level of performance has never been attained before in a complex track-reconstruction task, and achieving it opens the door to early reconstruction of track primitives transparently during detector readout. These data can be used as seeds by the High Level Trigger (HLT1/HLT2) to find tracks and perform trigger decisions with much lower computational effort than possible by starting from the

raw detector data. This can free an important fraction of computing power of the conventional event-processing farm, allowing more powerful and faster reconstruction at higher luminosities than otherwise possible. Implementation of this technology could enhance the physics potential of LHCb already from the following physics run (Run-4), by expanding its trigger capability with the inclusion of long-lived tracks in the HLT1 decision.

In this talk we describe the status of commissioning, and the performance of the first realistic prototype of this system. The prototype is configured to process data from the VELO pixel detector, that is compact enough to be processed by a small system (~40 boards), and yet accounts for a significant fraction (~1/2) of the HLT Level 1 (HLT1) computational load. The 2-dimensional pixel geometry of the VELO requires a demanding cluster-finding task to be performed at the 30 MHz event rate as a preliminary step, before performing track reconstruction proper. This has been addressed by a derivation of the same "Artificial Retina" approach, implemented in firmware within the already-existing readout boards, and will be a default part of the standard LHCb reconstruction already in Run-3. The track pattern-recognition stage is instead implemented in independent commercial boards, equipped with Stratix-10 FPGAs (2.8 MLE) and 16 * 28 Gbps links each, connected in a network topology of 4 cyclically-connected full-mesh nets, each carrying a total ~4 Tb/s flow of point-to-point connections.

Posters Programmable Logic, Design Tools and Methods / 165

Proton Sound Detector for Beam Range Measurement in FLASH Hadron Therapy

Authors: Elia Arturo Vallicelli[1]; Andrea Baschirotto[2]; Marcello De Matteis[None]

[1] *University of Milano Bicocca*

[2] *Univ. Milan Bicocca*

Corresponding Author: e.vallicelli@campus.unimib.it

Proton-Sound-Detectors (ProSDs) sense (at <1 ms latency) the thermoacoustic signal generated by the fast energy deposition at the Bragg peak of proton beams penetrating energy absorbers.
ProSDs are especially promising for experimental monitoring of high pulse rate (FLASH) hadron therapy treatments working in-sync with the beam.
This paper presents a mixed-signal detector capable of sensing and processing high rate (1k beam shots/sec) ionacoustic signals with <1 ms latency. The system was validated by measuring the dose deposition of a 20 MeV proton beam in water, achieving 3.43% precision (±2.75 GyRMS) after 50 ms acquisition (77.56 Gy total dose deposition).

Summary (500 words):

Background and aims
Proton Sound Detectors (ProSDs) sense the proton-induced thermo-acoustic pulse generated by particle beams penetrating a water energy absorber. This signal is directly proportional to the deposited dose.
Compared to nuclear imaging techniques, ProSDs have < 1 ms latency and sub-mm precision, making this technique particularly suitable in real-time monitoring of high dose depositions, as in the case of FLASH hadron therapy.
However, to quickly acquire and process this information, advanced and specific digital signal processing (DSP) stages are required.
For this reason, this paper presents a digital system on FPGA as back end element of the Detector, operating in sync with 1k shots/sec beam and finally providing digital domain proton induced acoustic tracks within 1 ms latency.

Methods
The Detector is composed by a piezoelectric acoustic sensor and low-noise analog front-end (60-80 dB low-noise amplifier, 4.5 MHz -3dB 3rd order low-pass filter and 10-bits 80 MS/sec A/D converter) and a DSP stage on a Xilinx Spartan 6 FPGA. It performs event-driven data acquisition (triggered by the beam shot) and a custom c++ GUI is used for signal processing and visualization. The Detector and the

embedded DSP have been validated with a sub-clinical 20 MeV proton beam with ~106 protons/shot and 1000 shots/sec rate. The Detector sensitivity is 173 mV/Gy (w.r.t. Bragg peak).

Results
Measured acoustic sensor output signal is 276 mV0-peak corresponding to 1.59 Gy dose at the Bragg peak, consistent with 1.6 Gy dose/shot calculated from the beam current and Bragg peak physical size. By repeating the measurement 8000 times, the measured dose precision has been found equal to 388 mGyRMS (24.4%) due to random noise fluctuations. By characterizing the noise performances (62.9 mVRMS, equivalent to 363 mGyRMS, from sensor and electronics themal/flicker noise) it is possible to measure the dose deposition variations due to random beam fluctuations over time, equal to 138 mGyRMS or 8.6% of proton number/shot. The cumulative dose after 50 shots (50 ms acquisition) is 77.56 Gy ± 2.75 GyRMS (3.43%). Finally, the ionoacoustic signal amplitude has been recorded for 1 s. By low-pass filtering, a slow ~7 Hz fluctuation in the ionoacoustic signal amplitude becomes observable. Such slow fluctuation is compatible with the beam fluctuation around the horizontal beam axis visible in the CCD beam spot monitoring system.

Conclusions
Compared to nuclear imaging techniques, Proton Sound Detectors promise sub-mm and sub-ms monitoring of the Bragg peak location, dose deposition and beam characteristics. The low-latency, high precision and low instrument complexity (and cost) make this technique appealing for experimental verification/monitoring of the proton beam range for both medical (hadron therapy) and physics research.

Systems, Planning, Installation, Commissioning and Running Experience / **166**

The Scalable Readout System as a common initiative - a personal review

Author: Michael Lupberger[1]

[1] *University of Bonn (DE)*

Corresponding Author: michael.lupberger@cern.ch

When the RD51 collaboration formed in 2008, the community initiated efforts for a standardised common readout system, the Scalable Readout System (SRS). The APV25 chip, originally designed for the CMS silicon strip detector, was the working horse within the first decade reading out gaseous detectors. Meanwhile, the VMM chip has taken over and further ASICs were (Timepix, SiPMs) or are currently (Timepix3, SAMPA) included. The SRS found many applications, not only in its core field.
I will review the system and collaborative effort from the perspective of a user and developer involved over the last decade.

Summary (500 words):

The RD51 collaboration, formed in 2008, is one of CERN's research and development initiatives. In a community of about 450 members from 89 institutes in 31 countries, the technological development of Micropattern Gaseous Detectors (MPGDs) is advanced. Within the electronics working group, a general readout system for the whole collaboration was initiated and devised by a core team of experts: The Scalable Readout System (SRS).

Over the last decade, the basic SRS with the APV25 ASIC was further developed and other front-end chips were implemented. An ATCA version was derived and besides of many R&D projects, some experiments apply the whole or parts of the system.

Not all initiatives were successful and such a common effort had to overcome many obstacles. Still, the system became a standard in the gaseous detector community and beyond. Meanwhile, more than 100 SRS APV systems were sold via the CERN store. Both the CMS GEM and the ATLAS NSW upgrade performed their R&D with the system. Recently SRS was refurbished for the next decade with the

implementation of the VMM chip. Projects to include SAMPA and Timepix3 are ongoing. There are plans to bring the SRS backend electronics to a recent technological standard.

Taking some messages from the EFCA Detector R&D roadmap process into account, in particular from the Training (TF9) and Electronics and On-detector Processing (TF7) symposia, my contribution will review the system and common effort. The mayor focus will be on the paradigm of the system as standardisation, adaptability and other factors like the influence of large projects, collaboration, compromises to make and less on technicalities of the electronics.

Having started as an inexperienced PhD student to implement the Timepix chip into SRS, then having been involved as a PostDoc in the mayor update of SRS for the upcoming decade with the implementation of the VMM chip as well as being a user of the system, I will look back on my more than ten years of experience with the system and the community. I will address the pros and cons of what stands behind SRS and outline how the system is used in Bonn.

Posters ASIC / 167

A low power clock generator 400-1800 MHz for ADPLL

Author: Pavel Ivanov[1]

Co-authors: Dmitry Normanov [2]; Eduard Atkin [2]

[1] *NRNU MEPhI*

[2] *NRNU MEPHI*

Corresponding Authors: ddnormanov@mephi.ru, pyivanov@mephi.ru

This paper describes a low-power all-digital clock generator (ADCG) designed for reading and processing signals from detectors of large physical experiments. The clock generator operates with a reference clock frequency of 10 MHz to 50 MHz and generates an output signal ranging from 400 MHz to 1800 MHz in 10 MHz steps. The clock generator has been approved in 28nm CMOS technology of TSMC. The power consumption and chip area of the block are 1.5 mW and 80x80 m^2 correspondingly. A wide range of reference and output frequencies makes this block versatile in application.

Summary (500 words):

There is a trend in modern electronics to digitize signals early on. This trend is leading to the development of predominantly analog-to-digital ASICs for physical electronics. The digital part of these ASICs needs phase-locked-loop block (PLL). The most of critical part of PLL is the clock generator (CG) block. CG block must be low-power, area-efficient, work stably when the supply voltage and temperature change in a wide range. CG block described in this article is fully digital (ADCG) and is designed to be used as a universal block for reading and processing signals from detectors of physical electronics. The block diagram of the ADCG block is shown in Figure 1. The ADCG contains the following blocks: a counter, an oscillator controlled by a digital code, a frequency divider and a control unit. The range of reference frequencies at which the ADCG operates varies from 10 to 50 MHz in 10 MHz steps. At the output, the ADCG generates signals in the frequency range from 400 MHz to 1800 MHz in 10 MHz steps. The ADCG principle of operation is based on counting the number of clock pulses at the output of the oscillator in a given time window and comparing it with the calculated theoretical value. The control module compares the calculated and actual counter values and generates an oscillator frequency control code. The oscillator block is a ring generator on NAND elements. It contains two segments - coarse and fine frequency parts. Coarse frequency adjustment is based on the activation or deactivation of a certain number of NAND gates in the generator loop. Fine tuning is shown in Figure 2 by switching the inputs of the NAND gate and is based on the difference in the signal propagation delay for different inputs of the NAND gate, which is very small. This approach allows to regulate the frequency of the oscillator with a very small time step and ensure high accuracy and stability of the generated frequency. The ADCG block has been tested in TSMC 28 nm technology using CAD Cadence. The power consumption and chip area of the block are 1.5 mW and 80 x 80 μm2 correspondingly. The measured block jitter is 20 ps. The ADCG is planned to be used as a part of a phase-locked loop for a data acquisition microcircuit for a time-projection camera of a multipurpose detector (MPD, Dubna).

Systems, Planning, Installation, Commissioning and Running Experience / 169

Installation, integration and first operating experiences of the ALICE ITS Upgraded Readout System

Author: Ola Slettevoll Groettvik[1]

[1] *CERN*

Corresponding Author: ola.slettevoll.grottvik@cern.ch

The ALICE Inner Tracking System has gone through a significant upgrade for the upcoming third running period of the CERN LHC. The new detector consists of seven layers of high-granularity pixel sensors, while 192 custom FPGA-based readout units control the sensors and transmit the data upstream for analysis. This contribution describes the current system status and the expertise gained by moving from commissioning to the installation and throughout the data-taking preparation period, focusing on the intricate integration with other system components. Furthermore, we outline strategies applied to identify and handle various error conditions of the readout system.

Summary (500 words):

The new ALICE Inner Tracking System (ITS) is using a total of 24120 ALPIDE monolithic active pixel sensors arranged as staves in a seven-layer cylinder configuration. The upgraded system design specifications allow data taking of a minimum of 100 kHz Pb-Pb and 400 kHz pp events, but the final design can achieve even higher interaction rates. The sensors chips are fully controlled by 192 readout units (RU), one per stave. The RU's main component is a Xilinx UltraScale FPGA that is responsible for the four primary operations:

1. Configuration of the sensors.
2. Distribution and control of triggers from the Central Trigger Processor (CTP) to the sensors.
3. Aggregating and formatting the data sent from the sensors electrically and forwarding it upstream to the ALICE Common Readout Unit (CRU) on optical links.
4. The monitoring and control of the sensors' voltage and current supply, controlling the Power Boards.

The ALICE ITS detector and its readout electronics were installed in the ALICE cavern in early 2021. In this contribution, we will present the status of the ALICE ITS detector readout electronics. Furthermore, we will describe the first experiences made going from commissioning to the installation in the ALICE cavern. This transition period is demanding since many issues can be revealed and addressed. Especially when integrating the readout system with other components, like the CTP, the CRU, and the various software for detector control and data distribution, issues and obstacles can be exposed and addressed. The integration process is further complicated by the continuing development of both firmware and software. We will report some of the lessons learned while integrating all the components of the system.
During the installation and preparation for data taking, the focus has been to optimize the system and reduce the number of potential data-taking inefficiencies that can arise during a run. We expect that the readout electronics will need to handle several types of anomalous conditions brought about by external factors. For instance, issues with cooling, powering, or single-event effects might provoke transient functional errors that can cause problems with correctly sampling data from the sensor links. During a run, the ultimate goal is that data reading efficiency is maximized. This is the reason why significant efforts have been directed into analyzing the possible error conditions of the system that might inhibit our objective. We will present some of the methods applied to cope with prospective issues.

Posters Power, Grounding and Shielding / 170

High precision scalable power converter for accelerator magnets

Authors: Krister Leonart Haugen[1]; Konstantinos Papastergiou[2]; Panagiotis Asimakopoulos[2]; Dimosthenis Peftitsis[3]

[1] *Norwegian University of Science and Technology (NTNU) (NO)*

[2] *CERN*

[3] *NTNU*

Corresponding Author: krister.leonart.haugen@cern.ch

The lower conduction power losses and the positive temperature coefficient that favours parallel connections, make Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs) to be an excellent replacement of existing Silicon insulated gate bipolar transistors (IGBTs) technology. These characteristics combined with high switching frequency operation, enables the design of high-accuracy DC-DC converters with minimised filtering requirements. This paper compares two designs for a converter with high-accuracy current (0.9ppm) supplying a 0.05H electromagnetic load; one design with the topology and filter for a typical IGBT-based full-bridge and a second one with a SiC MOSFET based topology without filter.

Summary (500 words):

A primary objective of the powering in particle accelerator is the precision and reproducibility of the experiments. Scalable converters enable sub-ppm current precision with minimal filtering requirements by using multiple modules in interleaved operation [1]. In order to reach the 1ppm level which is required for some applications active filters are often used [2]. However, they require relatively large reactors and their control is not trivial. With the introduction of SiC MOSFETs as a commercial alternative for switch-mode converters, it is now feasible to utilise this semiconductor technology in the world of high-particle physics as well. This paper demonstrates a case study for a 0.05H electromagnet with high accuracy requirement of 0.9ppm and investigates the performance improvements to the design and operation of such converters when using SiC MOSFETs compared to IGBTs. The benefits of the SiC MOSFET are two-fold. Firstly, the reduced conduction on-state losses and positive on-state temperature coefficient and secondly, the reduced switching losses, enabling higher switching frequencies. And with the technology emerging with lower current ratings than the IGBTs, parallel connection is necessary to take advantage of the advantages that the SiC can offer.

The reduced on-state losses of SiC MOSFETs enables high-efficiency operation. Besides, their positive temperature coefficient facilitates a robust and more reliable parallel connection, as the positive temperature coefficient leads to natural balance of the current. Introducing a number of parallel connected DC-DC converter enables the use of interleaving to achieve a lower current ripple.

The current ripple form a single converter can be approximated by Eq. 1, where the ripple is inversely proportional to the switching frequency of the DC-DC converter. By using SiC MOSFETs it becomes possible to increase the switching frequency from 5kHz that is currently used, up to 60kHz and beyond. This gives an increase in accuracy by an order of magnitude or more. In addition, higher switching frequency results in a higher frequency on the ripple, reducing the size of any filters if they are still required. Thus, the anticipated cost and losses of filters are reduced. It is also possible to consider 3-level modulation (unipolar switching), reducing the ripple even further.

Introducing parallel connected devices leads to an increased investment cost for the devices, but it can reduce the device losses, cooling requirements, filter requirements and filter losses. In addition to having the benefit of being a more scalable topology to cover a large range of loads with minimal overcapacity, redundancy, and introducing more segmentation for the storage in the case of pulsed loads with storage requirements for the DC-DC converter. By taking a complete view and considering lifetime costs, SiC MOSFETs seem to be very suitable technology for this application [3]. The final paper will present the design and operation of a topology to satisfy sub-ppm accuracy without filters and will show the advantages and disadvantages of such a design compared to a conventional converter with IGBTs and active filters.

Posters Trigger / 171

Upgrade of the CMD-3 trigger system.

Authors: Leonid Epshteyn[1]; Anton Gorkovenko[1]

[1] *Budker Institute of Nuclear Physics*

Corresponding Author: l.b.epshteyn@inp.nsk.su

In 2017, the luminosity at the VEPP-2000 collider at the Budker Institute of Nuclear Physics SB RAS, Novosibirsk, has increased. In this regard, it was decided to upgrade the trigger system of the CMD-3 detector. For this, the development of a device called the “Final Decision Block” was started. In this paper, we consider the designing and debugging process of the created block, as well as its implementation in the Data Acquisition System of the CMD-3 detector. The test results are presented both at the test bench and directly as part of the Data Acquisition System on the detector.

Summary (500 words):

he VEPP-2000 is an electron-positron collider located at Budker Institute of Nuclear Physics SB RAS. The collider is designed to provide luminosity up to 10^32 cm^(-2)s^(-1) at the maximum center of-mass energy sqrt(s) = 2 GeV. The Cryogenic Magnetic Detector (CMD-3) is installed in the interaction regions of the collider VEPP-2000. The CMD-3 is an electrophysical installation designed for accurate measurements of charged particles and photons.
The Data Acquisition system (DAQ) is one of the most important parts of the CMD-3 detector. Its task is to collect and record data from the detector, synchronize the operation of all units, and monitor the parameters of the detector subsystems. Thus, the CMD-3 DAQ automates the process of conducting the experiment and processes the received data. It consists of about 6500 measuring channels, the signals from which are processed by several types of electronic modules.
The CMD-3 DAQ includes blocks of the front-end electronics, the L-1 trigger, the Module for synCHronization of System (MChS), the General Interface Board for Data Delivery (GIBDD), and the Event Builder.
The L-1 trigger system consists of interface blocks (IFLT, ADAM) and solver blocks (ClusterFinder (CF) and Trackfinder (TF)). The IFLT and ADAM units prepare data from the front-end electronics and send them to the TF and CF, respectively. Operation of triggering electronics is based on the pipeline algorithm of data processing. Based on the received data, the solver blocks form logical arguments and, comparing them with masks, issue a decision on the registration of the current event. At the moment, there are two trigger signals: Charged Trigger (Trackfinder) and Neutral Trigger (ClusterFinder).
When designing the trigger system of the CMD-3 detector, it was planned that the start of the event digitization cycle would be carried out by a device called the Final Decision Block (FDB). The following signals should be proceeded as inputs: Charged trigger and signs of tracks, Neutral trigger and signs of clusters, which are formed in TF and CF respectively. Based on the arguments received, the FDB was obliged to make a final decision on the registration of the current event and, in the case of a positive decision, to generate the L-1 trigger signal.
In 2017, the VEPP-2000 collider luminosity was increased, thus it was decided to upgrade the trigger system of the CMD-3 detector. Upgrade will be carried out in two stages. The first stage is creation of the FDB with a Mixed trigger, which will allow the selection of events on the basis of joint data from the Charged and Neutral triggers. The second stage is creation of the second version of the block, which will combine the Charged, Neutral and Mixed trigger.
In this paper, we present the designed block and tests carried out with it, as well as its integration in the Data Acquisition System of the CMD-3 detector. The test results are presented both at the test bench and directly as a part of the Data Acquisition System of the detector.

Posters Systems, Planning, Installation, Commissioning and Running Experience / 172

New Generation RCE system for the Rd53 Pixel Front End chip readout

Author: Zijun Xu[1]

Co-authors: Dong Su [1]; Andrew Young [1]; Matthias Wittgen [1]; Larry Lou Jr Ruckman [1]

[1] *SLAC National Accelerator Laboratory (US)*

Corresponding Author: zijun.xu@cern.ch

The RCE (Reconfigurable Cluster Element) platform is a general-purpose system-on-chip data acquisition system, which is broadly deployed in various experiments, including ATLAS. A new generation of bench-top RCE system, based on Xilinx UltraScale+ MPSoC, is developed to support the Rd53a/b module and system testing with high performance. The RCE system also serves as the primary platform for validating the data transmission design of the ATLAS ITk pixel system with the same or equivalent components as the eventual ITk pixel system.

Summary (500 words):

The RCE (Reconfigurable Cluster Element) platform is a general-purpose system-on-chip data acquisition system, varying from a compact standalone bench-top form to ATCA compliant system. It is broadly deployed by several experiments, such as ATLAS, HPS, ProtoDUNE and LSST. Especially, the RCE was used as the platform for quality assurance and control system during the construction of the ATLAS inner-most pixel layer, IBL(Insertable B-layer).

In this work, we present the new generation bench-top RCE system, based on Xilinx UltraScale+ MPSoC Evaluation board ZCU102. A custom FMC adaptor card successfully runs Rd53a and ITkPixV1(Rd53b), which is used by ATLAS and CMS phase 2 pixel upgrades, at full speed. With industrial ICs, this card delivers ultra-low jitter (< 4ps random-jitter) with pre-emphasis for the Cmd at 160 Mb/s which cannot be run from an FPGA MGT directly. Rx data equalizing is also provided in the FMC card. These features are essential for the lossy transmission chain. Following the design of the FMC card, an ATCA blade and RTM is produced to read out a large number of Rd53 chips. This ATCA blade emulates the lpGBT functionalities with a large FPGA to aggregate the frontend 1.28Gb/s data links to 10Gb/s optical links for backend readout. Well-designed firmware and software are essential for a high-performance readout and calibration system. Raw data de-compressing by FPGA for Rd53b can improve chip calibration performance by a factor of 5. The ARM NEON SIMD(Single instruction multiple data) libraries can boost data processing speed by a factor of 3. Moreover, a look-up-table S-curve fitting engine reduces the fitting time by a factor of 10 for threshold scan. All the performance improvements allow the RCE system to take full advantage of the high output bandwidth (5.12Gbps) of the Rd53.

The RCE system also serves as the primary platform for validating the data transmission design of the ATLAS ITk pixel system, which is one of the most challenging tasks of the ATLAS Phase-2 upgrade. Up- and downlink communication from DAQ to the ITk periphery is foreseen to be largely optical and expected to be realized with lpGBT and VTRx+ ASICs. Radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first stage of transmission within ITk volume, up to 6m in length, with a combination of flex and twinax electrical links to carry signals to larger radii for optical conversion. A balance between data transmission bandwidth, stability, and material usage is required. A demonstration system is composed of an ATLAS ITkPixV1 chip, passive electrical links and interface PCBs with -20dB@640MHz signal loss, connecting to the opto-conversion stage that consists of a custom signal equalizer chip, GBCRv2, and lpGBT/VTRx+ for data aggregation and optical conversion. This whole data transmission chain is readout with RCE DAQ via optical link. This system stably runs at the design frontend data speed of 1.28 Gb/s, with measured BER<1e-12. The ITk pixel system data transmission design is validated with equivalent components as the eventual system.

Posters ASIC / 173

A Four-Channels Front End Electronics for ATLAS Muon-Drift-Tubes Detectors in 65nm CMOS Technology

Author: Adeel Syed Ali Shah[1]

Co-authors: Marcello De Matteis [1]; Robert Richter [2]; Hubert Kroha [3]; Markus Fras [3]; Andrea Baschirotto [1]

[1] *UNIMIB*

[2] *Max Planck Inst, Munich*

[3] *Munich, Max Planck Inst.*

Corresponding Author: s.shah4@campus.unimib.it

Front-End-Electronics are utilized by ATLAS muon chamber (MDT) to detect charge and give information regarding charge arrival time and amount of charge being detected. Read-Out-Electronics along with being robust, should operate faster, be area and power efficient. This paper presents improved version of AFE, ASD designed in 130nm technology, that is actually used for MDT chambers of ATLAS Experiment. AFE is designed in 65nm CMOS Process, with single Mode of operation and minimal architecture by eliminating two stages without effecting performance. Along with scaling down technology this AFE consumes 16mW per channel, which is 46% efficient than the previous design.

Summary (500 words):

Background and aims:
Front-End Electronics performs charge-to-voltage conversion by Preamplifier. This voltage pulse is further amplified and converted into Bipolar shape which carries information regarding Charge arrival time and amount of Charge been detected. To differentiate incoming small charges from noise Threshold level of 3-5 rms noise value is applied at discriminator Input. Each channel includes Analog part and Digital part. To control certain functional parameters, Shift Registers are used which can be programmed with Digital word at reset time through Serial Interface.
This paper presents a power and area efficient Front-End Electronics design for Muon Drift Tube which has minimum SNR of 14.5 dB and fast-peaking time of 11ns at Preamplifier output. It further, utilizes a new design of Shift Registers to re-read Data written through Serial I/O Data Interface.

Methods:
Key parameter in designing Preamplifier is to minimize noise performance by setting very high Transconductance (gmM1), 25mA/V, value of input Mosfets. This, however, increase current consumption, trade-off between noise and power, which is compensated by minimizing number of stages in overall design, hence saving overall power consumption. For fast peaking time, Op-Amp of Preamplifier is designed with High-Bandwidth of 2.4GHz along with good stability margin. For Bipolar Shaping of Signal, two stage shaper is utilized rather than three stages as used previously. Also, pre-discriminator stage is eliminated without effecting performance, thus further simplifying architecture and making it area, power efficient. With lower supply voltage, to keep maximum linear sensitivity at output of shaper, two stage differential amplifiers are utilized. Keeping circuit Architecture minimum and power-efficient, it operates in single mode of operation, Time-Over-Threshold, in which incoming signal is compared with threshold voltage set by programmable DAC's. Output of discriminator stage is sent to SLVS PADS cell, converted to external low-level signals for faster transfer rate.
To confirm that correct data is written into Registers, another block is implemented which reads registers Data using PISO interface. Programable Dead-Time circuit is added to suppress multiple threshold crossing in MDT Signal-Tail.

Results:
This design has sensitivity of 1.1mV/fC at output of Preamplifier and 8mV/fC at output of Analog signal processing Chain. Input noise density of CSP is 1.1 nV/√Hz. Peaking time of Preamplifier is 11ns and 14.4ns at end of Analog Chain. Bipolar signal reaches baseline about 400ns. Minimum SNR at output of preamplifier is 14.5 dB which increases up to 44dB for maximum charge input-pulse. Performance is investigated with respect to Process/Voltage/Temperature (PVT) variations to check robustness of circuit. It consumes power of 16mW per channel

Conclusions:
4-channels Front-End-Electronics for Muon-Drift-Tube has been presented. Design is carried-out in TSMC-65nm Technology. This work has targeted power and area efficient design along with achieving performance specifications of state-of-the-art AFE, ASD, already used in ATLAS detectors

Reference:
S. Abovyan, V. Danielyan, M. Fras, O. Kortner, H. Kroha, R. Richter, Y. Zhao, A. Baschirotto, M. De Matteis, F. Resta, "The new octal amplifier-shaper-discriminator chip for the ATLAS MDT chambers at HL-LHC", Nuclear Instruments and Methods in Physics Research A936, August 2019 – pp. 374-375

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DAMIC-M electronics and acquisition system

Author: Romain GAIOR[1]

Co-author: rocio vilar [2]

[1] *LPNHE*

[2] *ifca*

Corresponding Author: romain.gaior@lpnhe.in2p3.fr

We present the status of the DAMIC-M (Dark Matter In CCD at Modane) electronics and acquisition system. This first version controls a skipper CCD and measure the pixel charge with a single electron resolution. It was designed to allow optimization with respect to clocking and readout parameters to achieve the best tradeoff between noise and readout speed. We present the implementation of the full system composed of a mother board, a front end ASIC, the sequencer and ADC boards.

Summary (500 words):

The DAMIC-M experiment aims at the direct detection of dark matter particle with skipper CCDs [1] as target and sensor. Thanks to multiple non destructive charge measurements (NDCM) skipper CCDs allow to improve the pixel charge resolution from several electron to a fraction of electron (depending on the number of NDCM). The control and readout electronics have to ensure noise negligible compared to the CCD readout amplifier one (~15nV/sqrt(Hz)) and operate at maximum speed to keep the CCD dark current as low as possible.
The V1 of the DAMIC-M electronics comprises:
- A mother with an FPGA Altera ArriaV and a complete firmware to sequence the CCD and control the board and elements below.
- a front-end ASIC that will be placed at a few centimeters to amplify the CCD video signal with the option to perform an analog correlated double sampling.
- a dedicated board to produce the CCD clocks and biases. This board integrates CABAC [2] chips with the capability of clock rise and fall time configuration.
- An ADC board, for which 3 solutions are implemented and tested with either 20bit 1.6MS/s AD4020 with LVDS interface, a 20 bit 1.8MS/s with isolated digital interface or an 18bits 15MS/s LTC2387-18.
We present the implementation of this first system, the results of test and the plan for the future version.

[1] Tieffenberg et al. Single-electron and single-photon sensitivity with a silicon Skipper CCD, arXiv:1706.00028
[2] H. Lebbolo et al. CABAC : A CCD Clocking and Biasing Chip for LSST Camera. 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference, and Room-Temperature Semiconductor X-Ray and Gamma-Ray Detectors workshop, Oct 2013, Seoul, South Korea

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Radiation hard TwinAx for ATLAS ITk pixel electrical data transmission

Authors: Andrew Young[1]; Martin Kocian[1]; Dong Su[1]; Zijun Xu[1]; John Kenneth Anders[2]; Meghranjana Chatterjee[2]; Laura Franconi[2]; Isidre Mateu[2]; Roman Mueller[2]; Michele Weber[2]; Jessica Metcalfe[3]; Lea Halser[2]

[1] *SLAC National Accelerator Laboratory (US)*

[2] *Universitaet Bern (CH)*

[3] *Argonne National Laboratory (US)*

Corresponding Author: andrew.young@cern.ch

Abstract

The high radiation dose and the cold environment at the HL-LHC pixel detector regions presents serious challenges for the survival of optical components. Radiation hard twinax cables are developed for the ATLAS ITk pixel data transmission within the pixel detector volume for up to 6m before transitioning to optical links at larger radius where radiation dose is reduced to acceptable level for optical components. We will present the design, qualification and industrialization process of the ATLAS ITk pixel electrical links using such twinax cables.

Summary (500 words):

The need for radiation hard electrical links operating in the cold volume of the ATLAS upgrade tracker led to the original custom TwinAx R&D in 2008. Most commercial twinax cables use PTFE as dielectric medium, but it is unfortunately radiation soft. The systematic evaluation of the transmission loss and radiation hardness of components led to the key conclusion that Low Density Polyethylene (LDPE) is the optimal choice of dielectric medium, balancing data transmission quality and radiation hardness. The original TwinAx prototype from Temp-Flex (now a subsidiary of Molex) from 2009 with AWG30 Cu-clad Al signal wires and LDPE dielectric achieved 6.2Gb/s over 6m once applied pre-emphasis and 8b/10b DC-balance. With the RD53 pixel readout chip for HL-LHC settled to1.28 Gb/s data links, a more compact version of the TwinAx with AWG34 Cu signal wires became the nominal baseline for both the command links and data links in the ATLAS ITk pixel system. Although the command links are operating at only 160 Mb/s, it also carries the clock to be recovered by the front end chip so that it also requires Gb/s transmission quality.

In this presentation, we will describe the ATLAS ITk pixel TwinAx design philosophy with a drain wire to reduce shield material and manage termination heating. The thin jack further ensures the dimensions are minimized so that the high multiplicity of links can still fit into the very constrained service volumes. The design insertion loss is up to ~14 dB after irradiation for a maximum length of 6m. The S-parameter measurements before and after irradiation, as well as performance and mechanical integrity checks at low temperature will be presented. To comply with CERN/EU fire retardancy requirements, a series of fire propagation, smoke and acidity certification tests are also performed.

The ITk pixel TwinAx are organized into various types of E-link bundles depending on the detector region. The outer end of the bundles connecting to Optoboards are terminated with a rigid-flex for up to 8 command + 24 data links per Optoboard. The inner ends are terminated to the on detector Patch Panel 0 (PP0) with Samtec FireFly connectors with up to 12 links for the Outer pixel subsystem, or directly soldered to a densely packed PP0 with up to 100 TwinAxes in the Inner pixel system. We will present the termination PCB designs, TwinAx ribbonization and bundle termination process bundle electrical test results. We will also describe the Inner system PP0 design and bundle packing tests.

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Precision timing ASIC for LGAD sensors based on a Constant Fraction Discriminator – FCFD0

Authors: Artur Apresyan[1]; Thomas Zimmerman[1]

[1] *Fermi National Accelerator Lab. (US)*

Corresponding Authors: tzimmer@fnal.gov, artur.apresyan@cern.ch

Silicon detectors with excellent time resolution will play a critical role in future collider experiments, providing a new tool in event reconstruction. The Low Gain Avalanche Detectors (LGAD) have been demonstrated to provide the required time resolution and radiation tolerance. We will present the

FCFD0 ASIC developed to read out LGAD signals. The FCFD0 utilizes Constant Fraction Discriminator (CFD) algorithm to time-stamp the time-of-arrival, which has several advantages compared to Leading Edge discriminator, and promises to be more reliable in operation. Results from the first prototype chip produced in TSMC 65 nm node, will be presented.

Summary (500 words):

INTRODUCTION
The proposed future colliders call for O(10) ps time resolution in order to disentangle the expected extreme number of simultaneous interactions per bunch crossing and improve particle identification capabilities. The LGAD sensors are a leading candidate for such applications, and will be used in upgrades of the CMS and ATLAS experiments. We will present the design and measurements of the novel approach to time-stamping LGAD signals based on Constant Fraction Discriminator (CFD) algorithm, as implemented in the Fermilab CFD v0 chip (FCFD0).

OVERVIEW OF THE DESIGN
The FCFD0 uses several new techniques to achieve low power, area, jitter, time walk, and drift. This enables a simple and robust timing measurement (~30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required.
The FCFD0 forms both an attenuated and a delayed version of the amplified input pulse. The input stage is an integrator with a feedback capacitor and a parallel feedback resistor to provide "slow" continuous reset. The attenuated signal is derived very efficiently by splitting the integration capacitance into two series capacitors and buffering the midpoint node. The delayed signal is formed by a programmable RC delay on the integrator output, followed by a buffer. These two buffered signals then directly feed a fast differential amplifier. The single-ended output of the differential amplifier feeds a very simple output comparator that compares it to an internal DC threshold voltage.
The biasing of the integrator and differential amplifier chain is critical to achieving the best performance and eliminating the need for any trimming. The integrator capacitor midpoint must have a DC bias established, and the differential amplifier has a significant random input offset. A servo loop is used to establish the differential amplifier output voltage by sensing and filtering it and comparing it to an on-chip DC level setting. The capacitor midpoint is then driven appropriately in order to establish the desired DC output level of the differential amplifier.
In a classical CFD, the output comparator would have its threshold set to the quiescent value of the differential amplifier output. However, large signals have more comparator overdrive than small signals, and thus smaller delays. To compensate for this effect, the differential amplifier output is biased at a critical level away from the comparator threshold.

MEASUREMENTS
Evaluating the performance of the FCFD0 is a challenge in itself. To facilitate easy measurement of the critical parameters of the chip, an on-chip charge injection circuit was included at the input. It is carefully designed to produce charge pulses of widely differing amplitude but of identical shape and timing. A time-to-voltage converter at the output was designed to allow easy measurement and characterization of the time walk and jitter. Early measurements show these parameters are consistent with obtaining 30 ps timing precision.

CONCLUSION
We designed and manufactured the FCFD0 chip in TSMC 65 nm technology. Detailed results of the ongoing chip testing will be presented.

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The JUNO experiment and its readout electronics system

Authors: Pierre-Alexandre Petitjean[None]; Pierre-Alexandre Petitjean[1]

Co-authors: marta colomer [2]; Yifan Yang [3]; Barbara Clerbaux [3]

[1] *Université Libre de Bruxelles*

[2] *km3net*

[3] *Universite Libre de Bruxelles (BE)*

Corresponding Authors: pierre-alexandre.petitjean@ulb.be, bclerbau@ulb.ac.be, yifan.yang@cern.ch, mcolomermolla@km3net.de

The main goal of the Jiangmen Underground Neutrino Observatory (JUNO) under construction in China is to determine the neutrino mass hierarchy. The detector consists of 20 ktons of liquid scintillator instrumented by 17612 20-inch photomultiplier tubes, and 25600 3-inch small PMTs, with photocathode coverage of 77%. The electronics system is separated into two main parts. The front-end system, sitting under water, performs analog signal processing. The backend electronics system, sitting outside water, consists of the DAQ and the trigger. The design of the electronics system as well as the current production status will be reported in the presentation.

Summary (500 words):

The Jiangmen Underground Neutrino Observatory (JUNO) is a neutrino medium baseline experiment in construction in China. This experiment will look for neutrino mass ordering (NMO) and neutrinos from a wide variety of natural sources. The JUNO detector consists of 20 ktons of liquid scintillator contained in a 35 m diameter acrylic sphere, instrumented by 17612 20-inch photomultiplier tubes (PMTs), and 25600 3-inch small PMTs, accounting for a total photocathode coverage of about 77%. The required energy resolution to measure the NMO at a 3-4 sigma in about 6 years of data taking is of 3% at energy of 1 MeV.

JUNO's physics goals place stringent requirements on the electronics: an excellent photon's arrival time measurement for good vertex reconstruction, large dynamic range, and negligible dead time. The following specifications have been defined: to provide a full waveform digitization with a high speed, and a high resolution on the full dynamic range. The main risk concerns the reliability of the underwater electronics, which will not be accessible after the installation. The reliability requirement is to have less than 1% PMT and underwater electronics failure over 6 years.

The JUNO electronics system is separated into two main parts: underwater and outside water, which are connected through 100-meter Ethernet cables and power cables. The first contains the PMTs, the second hosts the backend electronic cards (BECs) and consists of the DAQ and the trigger. This scheme was adopted to get very precise PMT signal measurement required by JUNO's physics goals, but it poses strong requirements on electronics reliability.

First, the analog signals from the PMTs are processed and digitized by frontend electronics located underwater and protected by stainless-steel boxes. For large PMTs, three of them are connected to one Global Control Units (GCUs) which power the PMT and digitize the digitize the signal. This set-up is chosen to optimize the ratio between power consumption and reliability. Then, the digitized signal is processed by FPGA. The digital signal and the trigger information are forwarded to the dry electronics through 100 m Ethernet cables chosen over optical fibers for their price and reliability.

At this point, the signal reaches the back-end electronics, where the BECs collect and equalize the incoming trigger request signals, which are handled by FPGA mezzanine card. Each BEC receives 48 Ethernet cables from the 48 underwater boxes and distributes the clock signal to the GCU's. The signals from the various BECs are sent to 21 RMU (Reorganize & Multiplex Unit) cards and then send to the central trigger unit.

The electronics for small PMT is a bit different. On the underwater side, they are grouped by 128 over an underwater junction box where all the front-end electronics belongs. The readout and digitization of the 128 channels will be operated by single electronics board called ABC board. The small PMT share the design of large PMT for back-end electronics.

The talk will describe the full electronics system which has been developed for JUNO and will give an update on the production state.

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Test poster

Author: Alex Kluge[1]

[1] *CERN*

Corresponding Author: alexander.kluge@cern.ch

Test poster description

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Introduction

Author: Alex Kluge[1]

[1] *CERN*

Corresponding Author: alexander.kluge@cern.ch

Summary (500 words):

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Closing

Author: Alex Kluge[1]

[1] *CERN*

Corresponding Author: alexander.kluge@cern.ch

Summary (500 words):