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Towards the next generation of CERN radiation monitoring front end ASICs

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The front-end electronics of Ionization chamber for radiation protection demands challenging sensitivity requirements in the femtoampere range and a wide dynamic range. This work details the development trajectory that culminated in a single chip solution with current measurement capability spanning nine decades. The various Application Specific Integrated Circuits designed in the Radiation Protection team at CERN are explained. The challenges faced and the methodology adopted in designing ASICs for ultra-low current measurement is detailed. The latest version of the ASIC designed in 130nm technology can measure currents from -6 fA to -20 μA with an accuracy of 7%.

Summary (500 words)

ARCON and RAMSES are the two pillars that cemented the radiation protection and monitoring sphere of CERN. With the in-house developed next-generation radiation monitors- CROME, the legacy systems are getting replaced. This SoC-based SIL2 compliant modernized front end of the Ionization chamber is state-of-the-art technology. However, to mitigate the risks of obsolescence that might hinder the development in the future and to reduce the industrialization complexity process, an in-house development of ASICs for radiation monitoring was taken up. In this program, five series of ASICs were developed.

The first two families of ASICs named UTOPIA were designed in 350 nm technology. UTOPIA 1 identified the main sources of leakage in a typical current to frequency (CFC) based current measurement architecture in the 350 nm technology. UTOPIA 2 increased the measurement span to 9 decades and can measure current from -1 fA to -5 μA.

As the fab which provided the 350 nm technology started limiting the support for new designs, and with the need to have improved performance in pulsed radiation fields, newer technology nodes were evaluated for designing a future version of the ASIC. As the technologies scale down, the leakage currents increase which was hindering the use of advanced nodes for ultra-low current measurements. A technology demonstrator chip in GLOBAL FOUNDRIES 22nm technology established techniques of using thick gate transistors in the critical path to minimize leakage thus enabling the use of such technology nodes for low current measurements.

By following a similar approach, another ASIC in TSMC 130 nm was designed which compared different current measurement topologies and successfully demonstrated a measurement range from -1 fA to -1 μA. Among the three architectures compared –it was found that the direct slope measurement method was a good choice for fast low current measurement in the femtoampere range and charge balancing method for current from picoampere to microampere range.

The newest version of the ASIC designed also in 130 nm technology incorporated the two current measurement topologies and could attain an ultra-wide dynamic range from -6 fA to -20 μA. An increased feedback capacitor of the CFC along with a dedicated channel for generating high charges for measurement in the microampere range helped in increasing the dynamic range. The increase in the time of measurement resulted from higher feedback capacitor was compensated by the fast results from the direct slope method channel. Thus, a high-speed wide-band ultra-low current measurement system was realized. The ASIC meets the stringent requirements acting as a versatile front end for the Ionization chambers for future radiation monitors at CERN.

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