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A radiation tolerant 12 bits, 160 MS/s data conversion and transmission ASIC for the CMS electromagnetic calorimeter

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The readout electronics for the CMS Electromagnetic Calorimeter is undergoing a re-design in order to cope with the LHC ugrade. In particular, a fourfold increase in the sampling frequency (from 40 to 160 MS/s) is required. Therefore a new readout ASIC has been developed.
The ASIC, named LiTE-DTU, is designed in a CMOS 65 nm technology. The LiTE-DTU embeds two 12 bits, 160 MS/s ADCs, a time window based sample selection, lossless data compression and 1.28 Gb/s serialization. An on-chip PLL provides the 1.28 GHz clock required by the ADCs and the serializers from the 160 MHz clock.

Summary (500 words)

The High Luminosity LHC (HL-LHC) will require a significant upgrade of the readout electronics for the CMS Electromagnetic Calorimeter (ECAL).
While the detectors will be unchanged (PbWO4 crystals and APD photosensors), new Very Front-End (VFE) and Front-End (FE) cards with their associated ASICs are in advanced state of development.
The new VFE card will be equipped with a fast transimpedance amplifier (named CATIA), capable to follow the input signal shape and therefore more efficient in disentangle pile-up events with respect to the legacy charge sensitive amplifier. It will also have better capability in recognize signals from directs hits in the APD detectors from scintillation signals.
To take full advantage from the new preamplifier, its output signal needs to be sampled at 160 MS/s (i.e. four times the current sampling rate) with a 13 bits resolution. Therefore, a high-speed, high-resolution ADC is required. With these specifications, each readout channel will produce 2.08 Gb/s, in turn requiring a fast data transmission circuitry.
A new ASIC, named LiTE-DTU, was developed to this purpose. The ASIC has been designed in a commercial CMOS 65 nm technology and tested. The LiTE-DTU is designed to work connected on one side to the CATIA amplifier and on the other side to the LpGBT optical transceiver. It embeds two 12 bits, 160 MS/s A/D converters, a time window based sample selection, a lossless data compression and 1.28 Gb/s serializer. An on-chip PLL provides the 1.28 GHz clock required by the ADCs and the serializers from the 160 MHz master clock. The ADC IP block was designed by an external company while the PLL is adapted from the LpGBT low jitter PLL/CDR IP block.
Extensive tests have shown that the ADC is capable to reach the required ENOB of 10.2 bits with an external clock, while with the internal PLL clock the ENOB is limited to 9.7 bits with an input frequency of 30 MHz. The issue has been identified as deterministic jitter due to the coupling between the power supply and the frequency divider in the PLL and will be corrected in the final version. Data selection and compression logic has been successfully tested, as well as the PLL (apart from the extra jitter contribution).
The ASIC was designed to be radiation tolerant to a dose up to 20 kGy and resistant to single event upset. Functional test of the LiTE-DTU and its main building blocks (ADC and PLL) have been performed both before and after irradiation. SEU tests with protons and ions have also been performed. Overall

results are very good, albeit a few issues have to be addressed in order to fully comply with the specifications. Test results of the LiTE-DTU coupled with CATIA shows no increase in noise and excellent performance in terms of time and amplitude resolution.

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