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# First Measurement on TimeSPOT1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End

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This work presents the first measurements on the Time SPOT1ASIC. As the second prototype developed for the TimeSPOT project, the ASIC features a 32×32 channels hybrid-pixel matrix. Targeted to 4D-Tracking applications in High Energy Physics experiments, the system aims to achieve a timing resolution of 30 ps or better at a maximum event rate of 3 MHz/channel with a Data Driven interface. Power consumption can be programmed to range between 1.2 W/$cm^2$ and 2.6 W/$cm^2$. The presented results include operation and performance characterization.

## Summary (500 words)

Current plans for particle colliders upgrades aim to increase the statistics on rare events by increasing the beam instantaneous luminosity (up to 7×10 35cm−2s−1). Under this condition the number of pileup events is expected to increase to a value as large as 200, demanding new tracking techniques such as 4D-Tracking to maintain an adequate tracking efficiency and ghost-event rate. 4D-Tracking operates by exploiting both the time and positional information of the particle-detector interaction point. Therefore the development of a system capable of a local high-precision time measurement is critical to sustain the advancement in the field.The TimeSPOT project, by INFN, aims to develop a demonstration 4D-Tracking Detector with a spatial resolution of 55µm and a timing resolution of 30 ps or better. The system will be equipped with sensitive layers of Hybrid-Pixel detectors based on both 3D-Sensors. In this communication we will present the first measurements on the TimeSPOT1 Front-End ASIC, a prototype chip developed in a commercial 28 nm CMOS technology. This chip is the successor of TimeSPOT0,which was comprised of independent test blocks of the components of a FE chain. Compared to the first chip, TimeSPOT1 integrates a 32×32 channels matrix as well as all required logic and drivers for IO operations. The ASIC is testable both stand-alone or coupled with the target sensors via Bump-Bonding. Every Front-End Channel is equipped with a low-jitter (<30 ps) input Charge Sensitive Amplifier (CSA), a discrete time Discriminator and Vernier based Time to Digital Converter (TDC) with an LSB of 10 ps.The CSA features a novel AC-coupled Inverter based core Amplifier with leakage current compensation. The Analog Front-End has digitally configurable power consumption which can be varied between 2.3µW and 32.9µW per channel. The TDC can produce both Time of Arrival and Time over Threshold with an LSB of 10 ps and 1 ns respectively. This TDC power consumption varies with hit-rate per channel, it is estimated to be 20µW when on idle; it consumes 25µW, 45µW and 69µW at 100 KHz, 500 KHz and 1 MHz respectively. Both the 32×32 channels matrix, its service circuitry and power and data paths are integrated in the area that matches the one of the full sensor-matrix. In this way it is possible to build a free from dead-space pixel sensor by correctly routing the input signals to match the sensor grid with the electronics one. The periphery of the chip contains the data-read out paths, LVDS IO drivers and a PLL for clock recovery. Data is derandomized and transmitted to the 8 output driver using an end-of-column readout tree. The system is able to transmit a maximum of 10.24 Gb/s with an estimated power consumption of 100 mW. The system is Data Driven and can be synchronized with an external signal for global time reference.The ASIC has been assembled with its PCB and is now under test. The test comprises the ASIC characterization in different power regimes. Valuable parameters to be extracted from measurement are timing resolution, channels uniformity, peak-datarate and power consumption.

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