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The ETROC1: The first full chain precision timing prototype for CMS MTD Endcap Timing Layer (ETL) upgrade

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The Endcap Timing Readout Chip (ETROC) is being developed for the CMS MTD Endcap Timing Layer (ETL) for the HL-LHC, to process LGAD signals with time resolution down to 30ps per track. The ETROC1 is the first full chain precision timing prototype, including preamplifier and discriminator, as well as a new low power TDC design that performs time-of-arrival (TOA) and time-over-threshold (TOT) measurements. It also includes a 4x4 pixel array with precision clock distribution network that is scalable to the final full size 16x16 array. The performance of ETROC1 with bench test and beam test results are presented.

Summary (500 words)

The development of the ETROC ASIC is divided into three prototyping phases (in 65nm CMOS technology). ETROC0 consists of a single channel analog front-end with preamplifier and discriminator only, ETROC1 is 4x4 array with full chain precision timing signal processing including a new TDC stage for TOA/TOT measurements, while ETROC2 is the first full size and full functionality prototype chip (16x16). The ETROC0 chips have been demonstrated in beam with time resolution of around 33 ps from the pre-amplifier waveform analysis and around 42 ps from the discriminator pulses analysis. A subset of ETROC0 chips have also been tested to a total ionizing dose (TID) of 100 MRad using X-ray machine at CERN and no performance degradation observed. The ETROC0 design is successful and is directly used without modification for ETROC1. The ETROC1 has 5x5 pixel arrays with a 4x4 pixel array H-tree style clock distribution network that is scalable to the final full size of 16x16. The ETROC1 is the first full chain precision timing prototype, aiming to study and demonstrate the performance of the full signal processing chain, with the goal to achieve 40 to 50 ps time resolution per hit with LGAD (˜30ps per track with two detector layer hits). One of the challenges of the ETROC design is that the TDC is required to consume less than 200 μW for each pixel at the nominal hit occupancy of 1%. To meet the low-power requirement, we use a single delay line for both the Time of Arrival (TOA) and the Time over Threshold (TOT) measurements without delay control. This TDC is based on a simple delay-line approach originally developed in FPGA implementation. A double-strobe self-calibration scheme is used to compensate for process variation, temperature, and power supply voltage. The overall performances of the TDC have been evaluated and meet the CMS ETL upgrade requirements. The TOA has a bin size of 17.8 ps within its effective dynamic range of 11.6 ns. The TOT has a bin size of 35.4 ps within its measured dynamic range of 9.8 ns. The effective measurement precisions of the TDC are 5.6 ps and 9.9 ps for the TOA and 10.4 ps and 16.7 ps for the TOT with and without the nonlinearity correction, respectively. The bare ETROC1 chips have been tested extensively using charge injection, and the measured performance agrees well with the simulation, including the power consumptions. The bump bonded ETROC1 chips (with LGAD sensors) have been also extensively tested using charge injection, laser and test beam. The timing performance of the full signal processing chain as well as the 4x4 pixel array clock distribution network has been studied. This talk will briefly describe the ETROC1 design including the new TDC and clock tree distribution network, and then focus on the bench test and beam test results of the bump bonded ETROC1 chips, and how the knowledge gained from bump bonded ETROC1 testing are applied to guide the on-going full size ETROC2 design.

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