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Performance simulations and characterization of RD53 pixel chips for ATLAS and CMS HL-LHC upgrades

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The RD53B pixel readout chip has been submitted for fabrication, meeting specifications of the ATLAS and the CMS experiments for HL-LHC upgrades. Performance characterization of a readout chip in terms of link data rate, average readout latency and efficiency of hit data is essential to evaluate operation of pixel sensors at an extreme interaction rate. At the same time it is complex due to its dependence on various environmental conditions and operational settings. In this work, readout performance parameters and their simulation results for various detector positions of the ATLAS and the CMS experiments are presented.

Summary (500 words)

The Large Hadron Collider (LHC) at CERN is being upgraded to deliver increased luminosity of 7.5 \times 10^{24} cm^{-2}s^{-1}, a factor seven higher than its operation during 2018. Sub detectors of the ATLAS and the CMS experiments are being upgraded to cope with new operational conditions and physics requirement at an unprecedented interaction rate. Silicon based tracker systems of the ATLAS experiment and the CMS experiment will be equipped with new pixel sensors having pitches of 50 µm x 50 µm and 100 µm x 25 µm for phase II upgrade. The RD53 collaboration has designed and submitted readout chips testing and evaluating performance of sensors and their redout electronics. The collaboration has submitted two specific versions of RD53B chips following specifications of each experiment. Both versions of the RD53B chip for the ATLAS (ITK-V1) and the CMS (CROC-V1) differ in terms of required chip size and analogue front ends based on specifications driven by respective experiment. These chips are identical in terms of control, configuration, processing, and readout link interface of the hit data. In this work performance of readout architecture of the RD53B chip is characterized for data rate on readout link under range of operational conditions of the ATLAS and the CMS experiment. Characterization and performance evaluation is performed utilizing Universal Verification Methodology (UVM) based simulation and verification framework developed by the RD53 collaboration. Submitted version of the RD53B chip is extensively simulated processing detector Monte Carlo (MC) hit data of different positions. Effect of operational environment in terms of hit rate and role of operational parameters related to trigger and readout link settings are evaluated to estimate bandwidth utilization of front-end links and average readout latency. Option to minimize number of front-end links is investigated by simulating and reading out data from four chips via a shared single front-end link. In this work, average readout latency and bandwidth utilization of the shared single front-end link is characterized for various trigger settings. The RD53B chip is equipped with memory buffering hit data while waiting for a trigger which validates buffered data to be readout, named as latency buffer. Saturation of the latency buffer may lead to loss of hit data. This work further includes occupancy studies of latency buffer verifying that implemented size of memory is sufficient handling extreme hit rates without being over saturated. Hit efficiency in terms of lost hits vs total generated hits during a simulation is recorded and compared against specifications. These results are expected to guide in establishing performance benchmarks (data rate, readout latency, hit efficiency) for evaluations of sensors and pixel modules under various environmental conditions (hit rate) and range of operational settings (trigger rate, latency, link speed).

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