Precision timing ASIC for LGAD sensors based on a Constant Fraction Discriminator – FCFD0

A. Apresyan[1], T. Zimmerman[1]
[1]*Fermi National Accelerator Laboratory, Batavia, IL 60510, USA*

***Abstract* — Silicon detectors with time resolution around 30 ps will play a critical role in future collider experiments, providing a new tool in event reconstruction. The Low Gain Avalanche Detectors (LGAD) have been demonstrated to provide the required time resolution and radiation tolerance. We will present the FCFD0 ASIC developed to read out LGAD signals. The FCFD0 utilizes Constant Fraction Discriminator (CFD) algorithm to time-stamp the time-of-arrival, which has several advantages compared to Leading Edge discriminator, and promises to be more reliable in operation. Results from the first prototype chip produced in TSMC 65 nm node, will be presented.**

I. Introduction

The proposed future colliders call for O(10) ps time resolution in order to disentangle the expected extreme number of simultaneous interactions per bunch crossing and improve particle identification capabilities. The LGAD sensors are a leading candidate for such applications, and will be used in upgrades of the CMS and ATLAS experiments. We will present the design and measurements of the novel approach to time-stamping LGAD signals based on Constant Fraction Discriminator (CFD) algorithm, as implemented in the Fermilab CFD v0 chip (FCFD0).

II. Overview of the design

The FCFD0 uses several new techniques to achieve low power, area, jitter, time walk, and drift. This enables a simple and robust timing measurement (~30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required.

The FCFD0 forms both an attenuated and a delayed version of the amplified input pulse. The input stage is an integrator with a feedback capacitor and a parallel feedback resistor to provide "slow" continuous reset. The attenuated signal is derived very efficiently by splitting the integration capacitance into two series capacitors and buffering the midpoint node. The delayed signal is formed by a programmable RC delay on the integrator output, followed by a buffer. These two buffered signals then directly feed a fast differential amplifier. The single-ended output of the differential amplifier feeds a very simple output comparator that compares it to an internal DC threshold voltage.

The biasing of the integrator and differential amplifier chain is critical to achieving the best performance and eliminating the need for any trimming. The integrator capacitor midpoint must have a DC bias established, and the differential amplifier has a significant random input offset. A servo loop is used to establish the differential amplifier output voltage by sensing and filtering it and comparing it to an on-chip DC level setting. The capacitor midpoint is then driven appropriately in order to establish the desired DC output level of the differential amplifier.

In a classical CFD, the output comparator would have its threshold set to the quiescent value of the differential amplifier output. However, large signals have more comparator overdrive than small signals, and thus smaller delays. To compensate for this effect, the differential amplifier output is biased at a critical level away from the comparator threshold.

III. Measurements

Evaluating the performance of the FCFD0 is a challenge in itself. To facilitate easy measurement of the critical parameters of the chip, an on-chip charge injection circuit was included at the input. It is carefully designed to produce charge pulses of widely differing amplitude but of identical shape and timing. A time-to-voltage converter at the output was designed to allow easy measurement and characterization of the time walk and jitter. Early measurements show these parameters are consistent with obtaining 30 ps timing precision.

IV. Conclusion

We designed and manufactured the FCFD0 chip in TSMC 65 nm technology. Detailed results of the ongoing chip testing will be presented.