Precision timing ASIC for LGAD sensors based on a Constant Fraction Discriminator – FCFD0

Design and test results of a first concept chip

Tom Zimmerman

Fermilab

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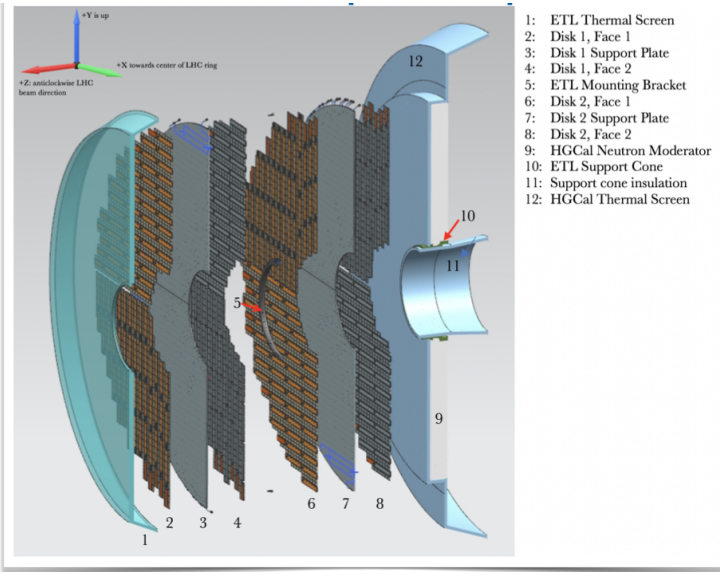
Future trackers will be 4D (x, y, z, *t*)

- The 4D-trackers will play a key role at the future machines
  - Background reduction, track reconstruction, triggering – all will need precision timing information, in addition to precise position information
  - All these pose unique challenges (and opportunities) to detector and electronics design, and event reconstruction
- CMS and ATLAS are building 1st generation of these 4D-tracking detectors
  - Next generation detectors will be more sophisticated and replace tracker
  - Active R&D now on technologies to achieve the required detector performance

Measurement	Technical requirement
Tracking for e^+e^-	Granularity: 25x50 μm^2 pixels
	5 µm single hit resolution
	Per track resolution of 10 ps
Tracking for 100 TeV pp	Generally the same as e^+e^-
	Radiation tolerant up to $8x10^{17}$ n/cm^2
	Per track resolution of 5 ps

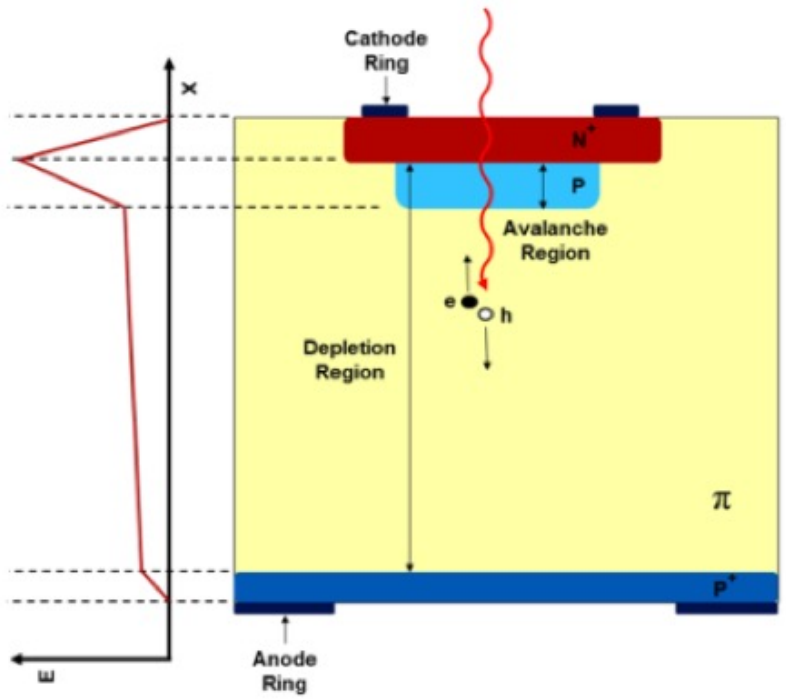
Technical requirements for future trackers:
from DOE's HEP BRN

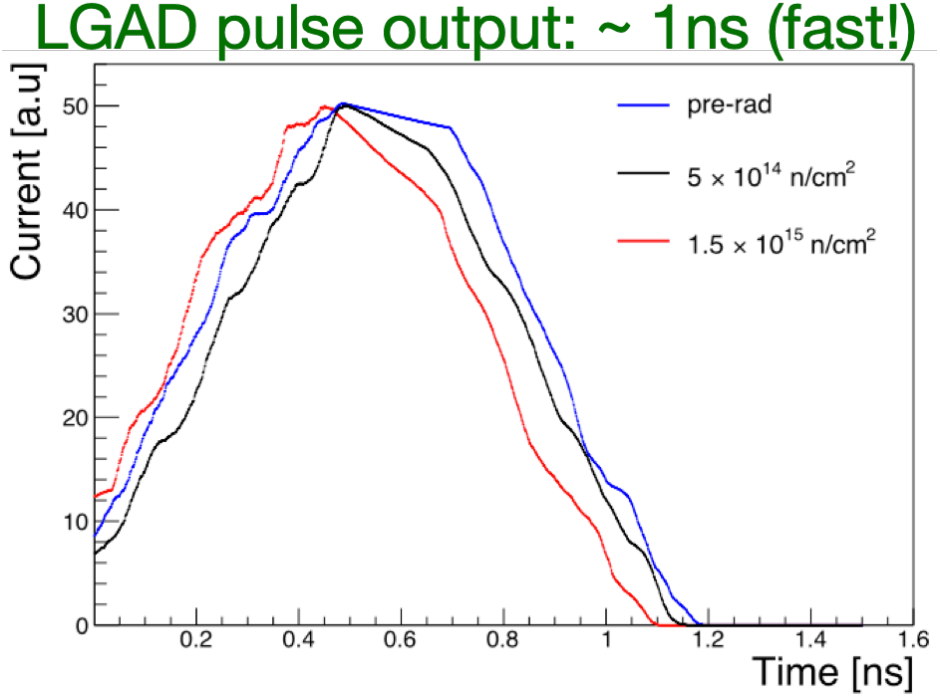


CMS endcap timing detector

Low Gain Avalanche Detector (LGADs)

- Technology for HL-LHC timing detector: ~30 ps
  - Silicon detectors with internal gain
- Thin doped-layer to create large E-field → avalanche
- Improved signal-to-noise ratio → good timing





The work presented here is part of a general Fast Timing R and D effort for electronics.

FCFD0 (Fermilab Constant Fraction Discriminator) is a first demonstrator chip

R and D Goals:

- Develop a robust *fast-timing discriminator* for fast detectors
- Time resolution of 30 pS or better
- Appropriate for use in IC pixels
- Easy to use: *one measurement per hit, no corrections required*
- Stable: *no repeated calibrations and threshold adjustments*
- Very low dead-time after a hit (~ 25 ns)

The big challenges

Our approach:

- Adapt the Constant Fraction Discriminator (CFD) principle for a pixel – when a CFD is paired with a TDC, *one time measurement* gives the final answer. System is ready again for another measurement soon after.
- We modify the classical CFD approach to eliminate the need for pixel-by-pixel trimming or compensation
- The 1st design is tailored to serve an existing need: LGADs for HL-LHC
- General principle should be useful for other applications (beyond LGADs)

As far as we know, this is the first IC pixel design for fast timing based on a CFD.

***Additional challenge*: how to bench-test this device with precision to know its performance!**

↓

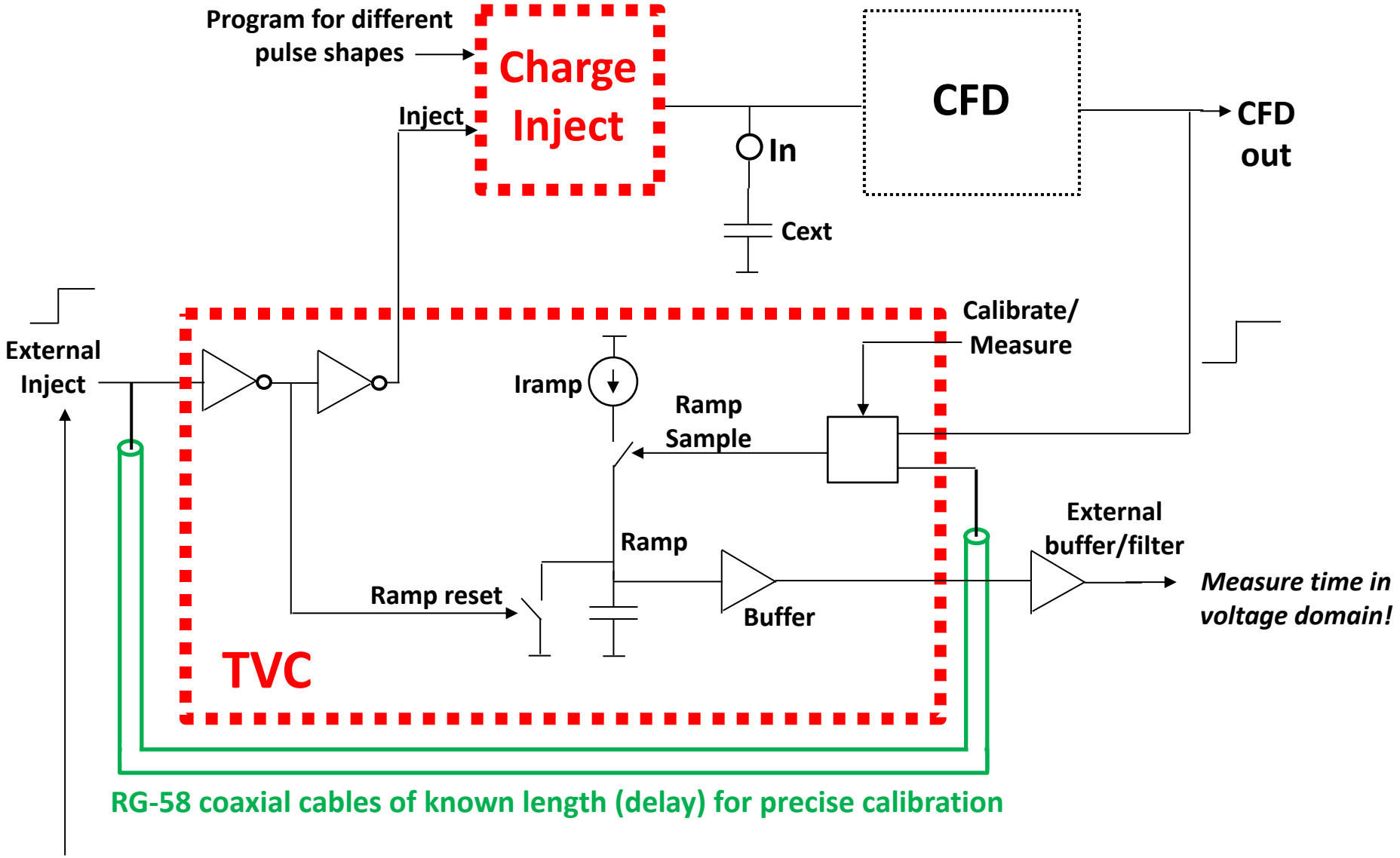
Additional goals:

- **Design an on-chip charge injection circuit that can deliver a wide range of charge pulses**
- **Implement an on-chip time-to-voltage converter with precision of ~ few pS to enable easy measurement of discriminator output delay and jitter.**
- **Establish methods to accurately measure all relevant parameters of these test circuits to ~1% level (so that we know the shape and amplitude of injected pulses), and a method to measure the discriminator input capacitance (so we can accurately mimic the detector capacitance).**
- **Use only readily available basic test equipment (pulse generator, oscilloscope, etc.)**

Success will result in:

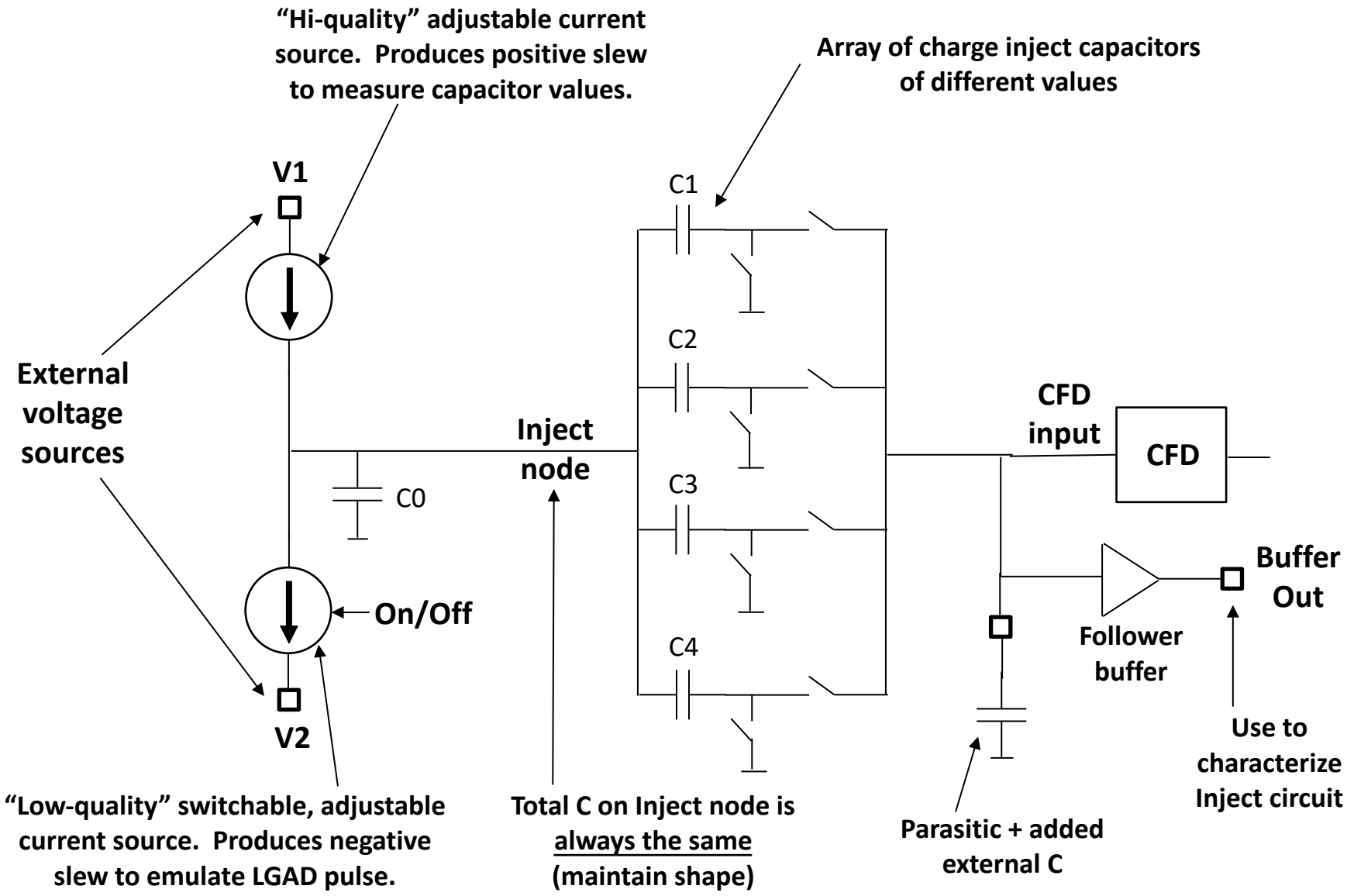
A high-performance timing discriminator that is well characterized on a basic test bench!

Incorporate two test circuits into each pixel: Charge Inject and TVC (time to voltage)



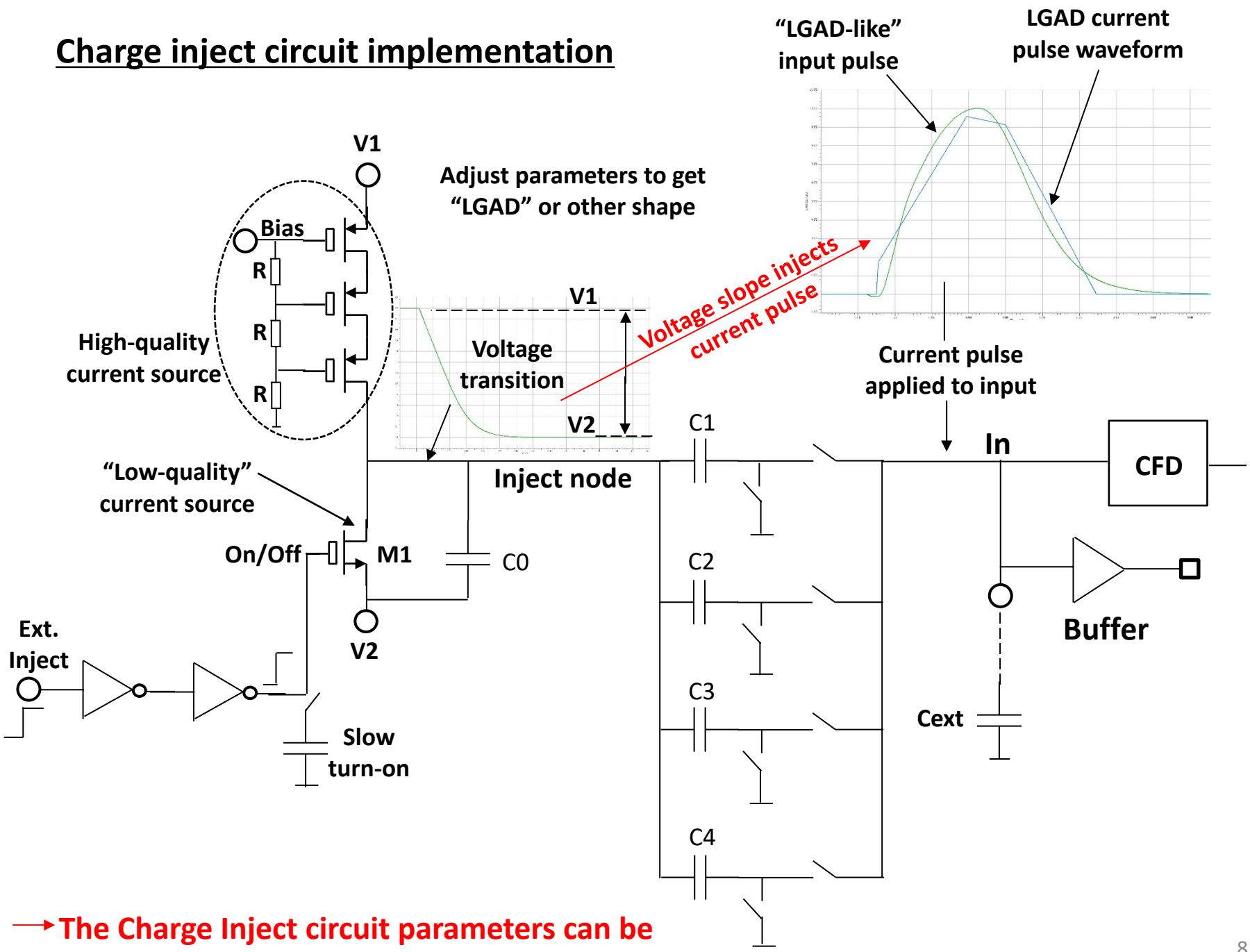
One external pulse activates both circuits:
TVC (ramp) is started, and known charge is injected to the discriminator.

Charge Inject circuit concept



The Charge Inject circuit is carefully designed to enable *accurate calibration*, and therefore, *well-known and adjustable input pulse shape and amplitude*.

Charge inject circuit implementation



→ The Charge Inject circuit parameters can be adjusted to provide an "LGAD-like" input pulse.

Develop a method to characterize the Charge Inject circuit on the bench

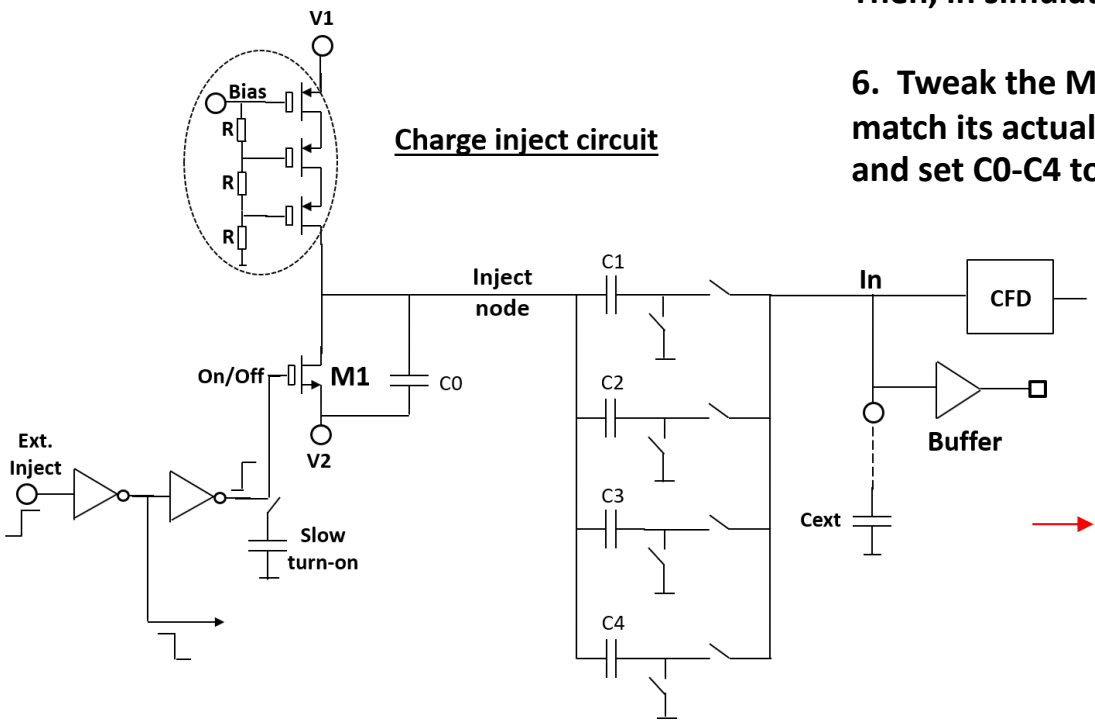
1. Measure gain of buffer
2. Measure characteristic of M1

By arranging voltage slew on the Inject Node, one can then measure:

3. Total capacitance on Inject node (C0+C1+C2+C3+C4+parasitic)
4. Value of each inject capacitor (C1-C4)
5. Total C on In node (Cext + parasitic)

Then, in simulation:

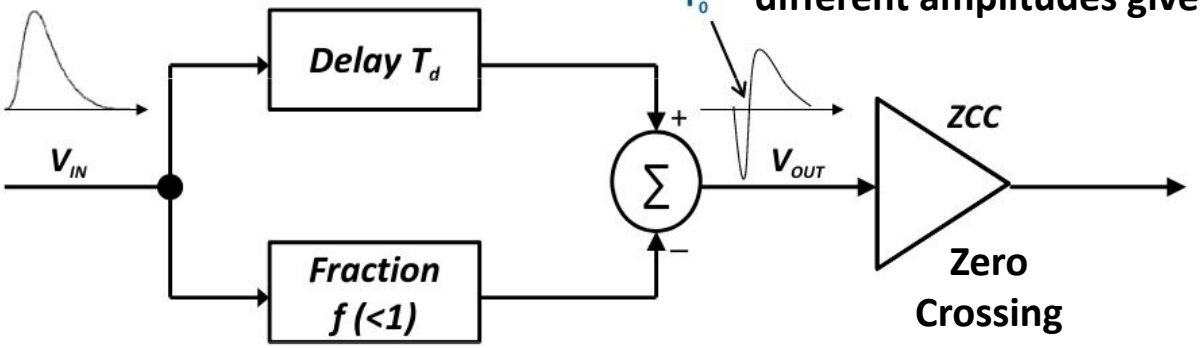
6. Tweak the M1 model to closely match its actual measured behavior and set C0-C4 to their measured values.



→ When parameters are carefully measured, we can use simulation to show the on-chip inject pulse shape/amplitude quite accurately!

CFD design

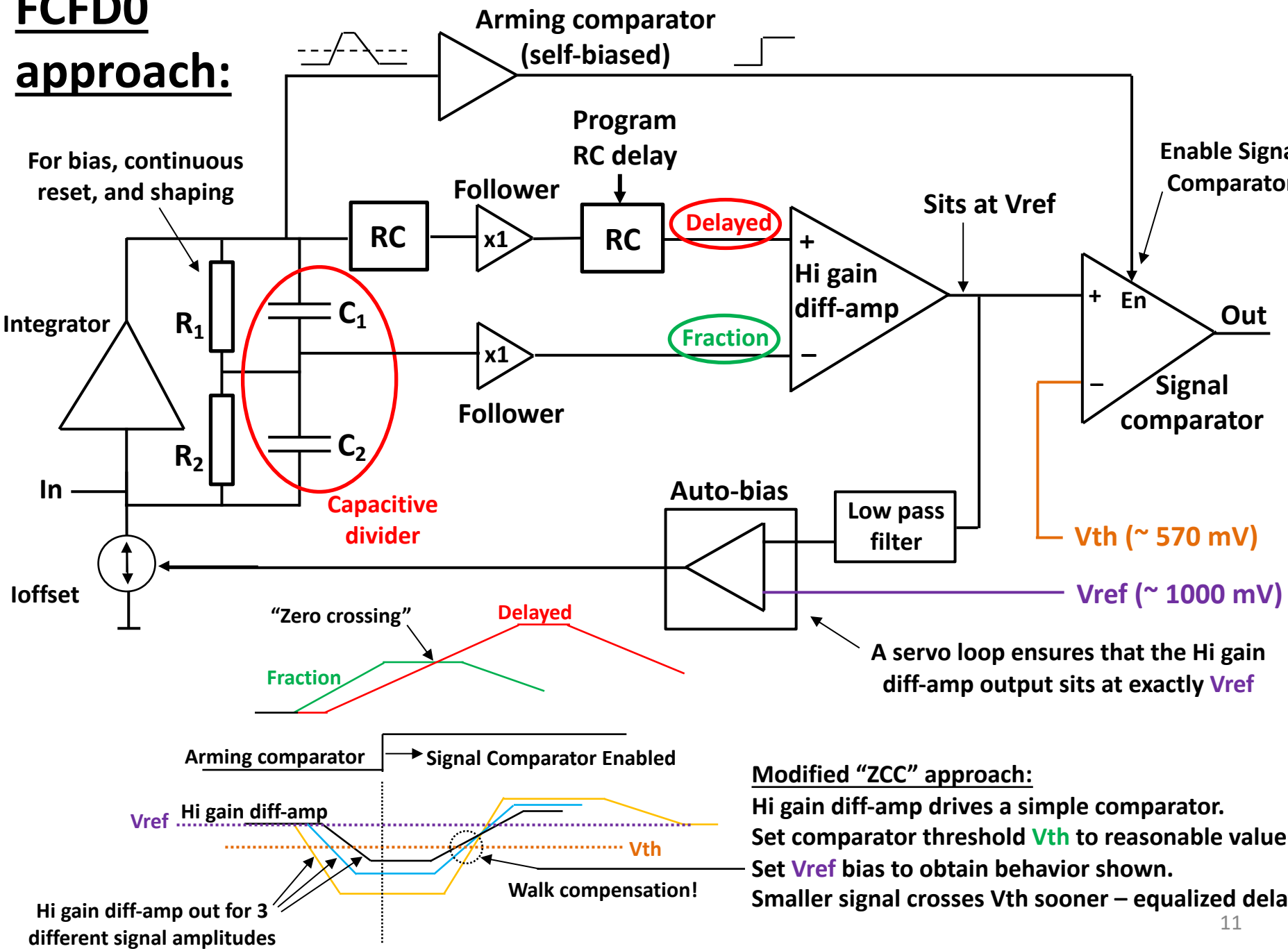
Classical CFD:



CFD-in-a-pixel design challenges:

- **How to amplify a small detector charge and drive the Delay/Fraction circuits?**
- **How to obtain the Fraction signal with low power in a small area ?**
- **How to do a programmable Delay? (optimal delay depends on pulse shape)**
- **How to do a Zero Crossing Comparator without having to trim the offsets?**
- **What about ZCC time-walk? (a classical CFD still needs some form of walk compensation since different signal slopes at the comparator input give the same crossing time but *different real-world comparator delay*)**

FCFD0 approach:

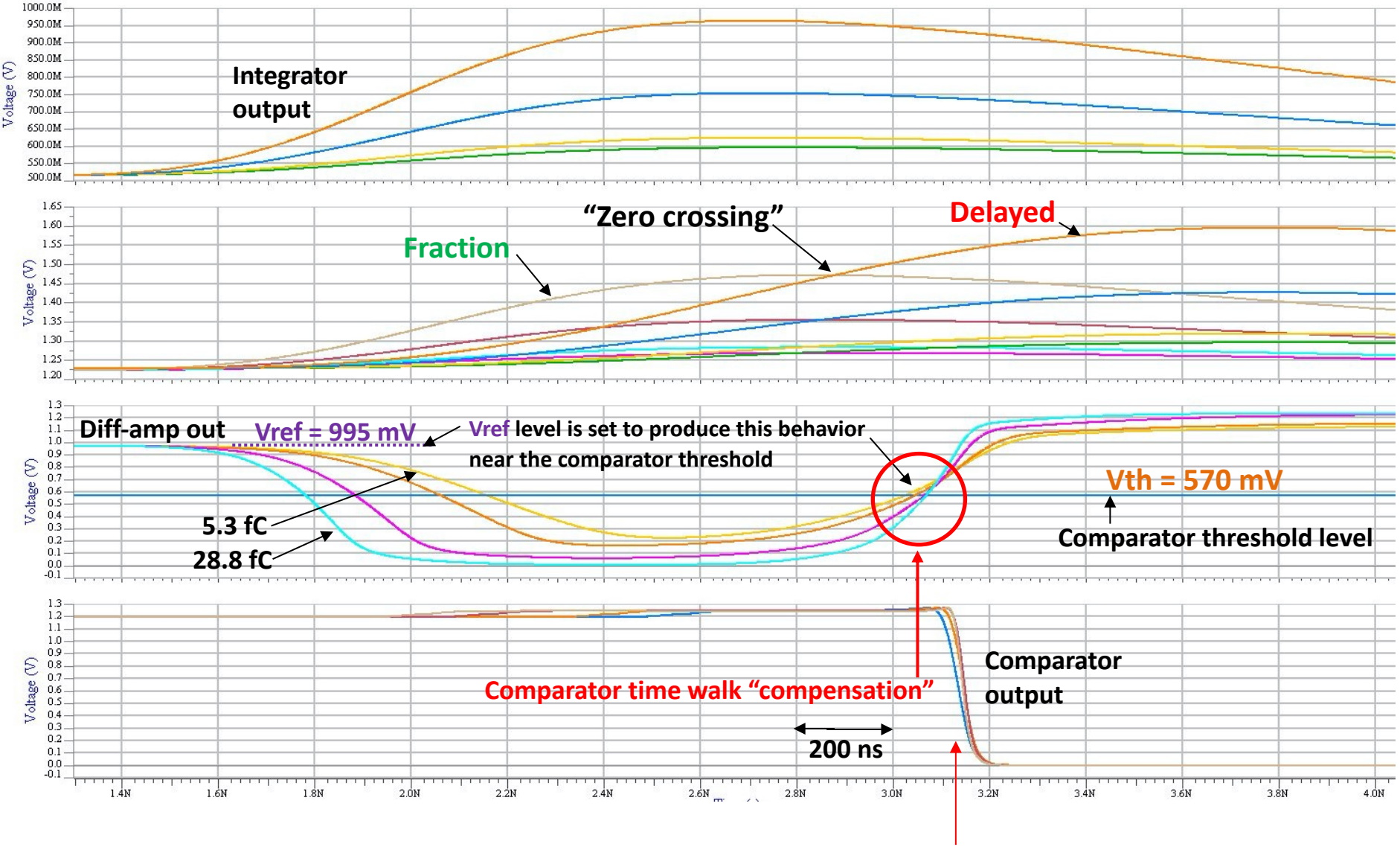


Modified "ZCC" approach:

Hi gain diff-amp drives a simple comparator.
Set comparator threshold Vth to reasonable value.
Set Vref bias to obtain behavior shown.
Smaller signal crosses Vth sooner – equalized delay!

Simulation: Apply LGAD-like charge pulse to FCFD0 input.

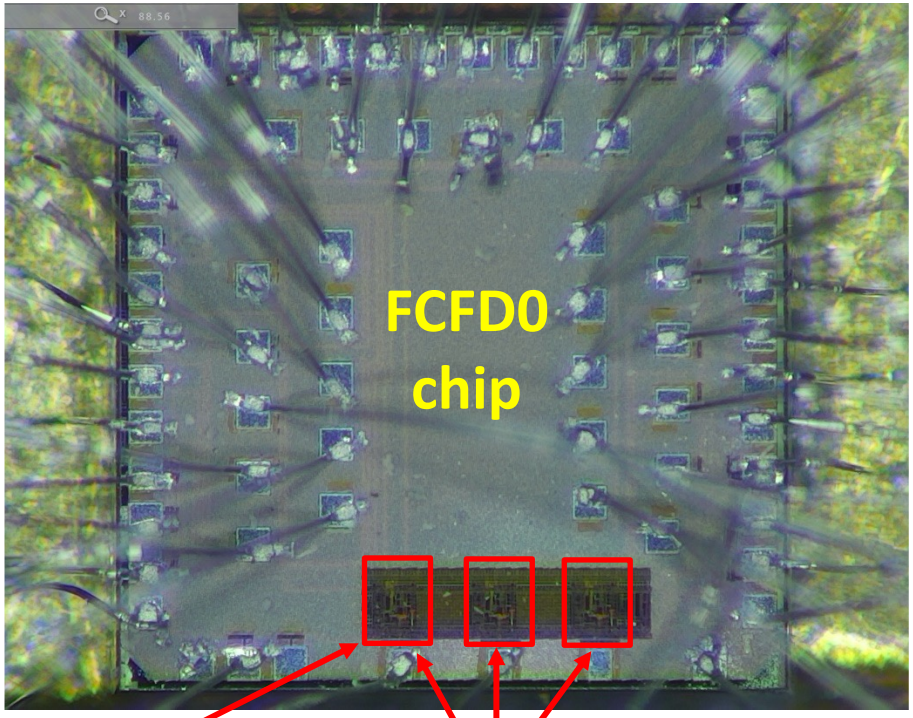
Inject 4 different amplitudes: Qin = 5.3 fC, 7.0 fC, 15.3 fC, 28.8 fC



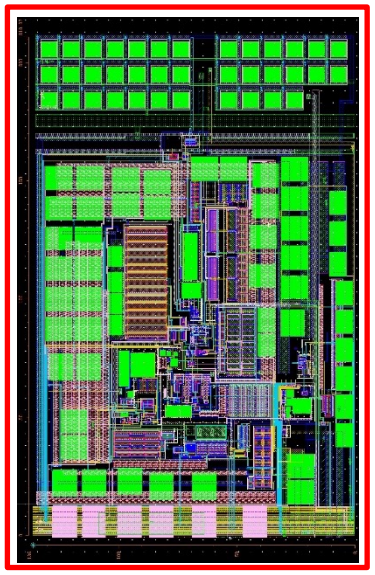
Comparator output has same delay for a range of input amplitudes

Measurement Results

(Charge Inject input only, not yet tested with an LGAD)



TSMC 65 nm pixel layout



First, how to set the optimal delay?

LGAD-shape internally injected pulse
Cin = 3.40 pF
Input charge = 7.0 fC

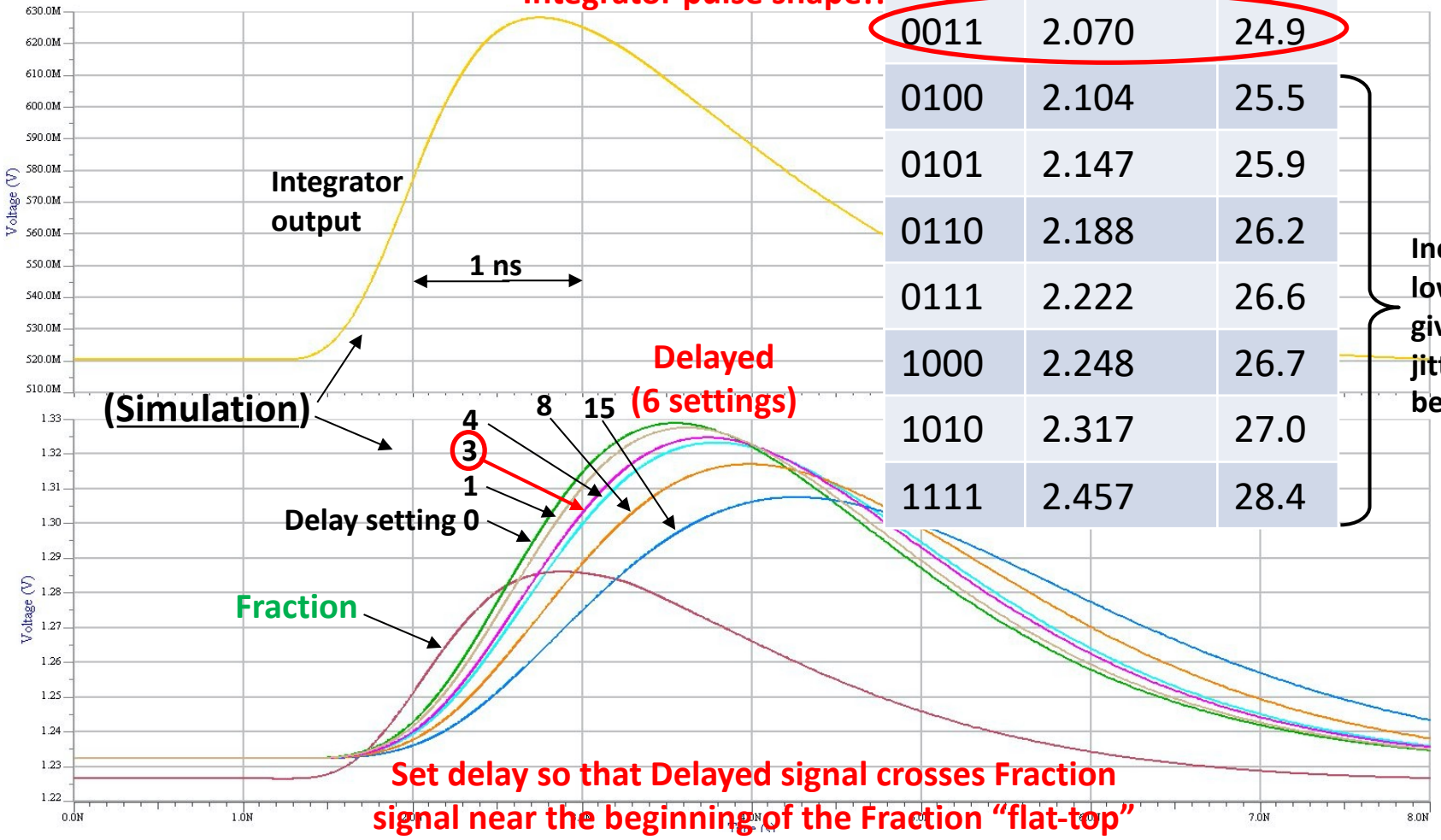
The best Delay setting will depend on the Integrator pulse shape!!

Delay setting	Measured Output delay (ns)	Jitter (ps)
0000	1.908	26.9
0001	1.975	25.0
0010	2.019	24.8
0011	2.070	24.9
0100	2.104	25.5
0101	2.147	25.9
0110	2.188	26.2
0111	2.222	26.6
1000	2.248	26.7
1010	2.317	27.0
1111	2.457	28.4

Measured jitter

Not enough delay – not crossing "flat-top"

Increasingly lower slope gives higher jitter, no benefit



LGAD-shape injected pulse: measured delay dispersion and jitter vs. input charge

Cin = 3.40 pF (LGAD capacitance)

"Low power"

Input transistor current = 520 uA

Delay setting = 0011

Qin (fC)	Delay dispersion (pS)	Jitter (pS)
2.4	+129	73
3.2	-17	49.1
5.6	0	32.3
7.0	+3	25.3
9.4	+2	19.0
10.2	(0)	18.0
12.6	-3	15.1
13.1	-6	13.9
20.1	-9	9.6
25.7	-6	8.0

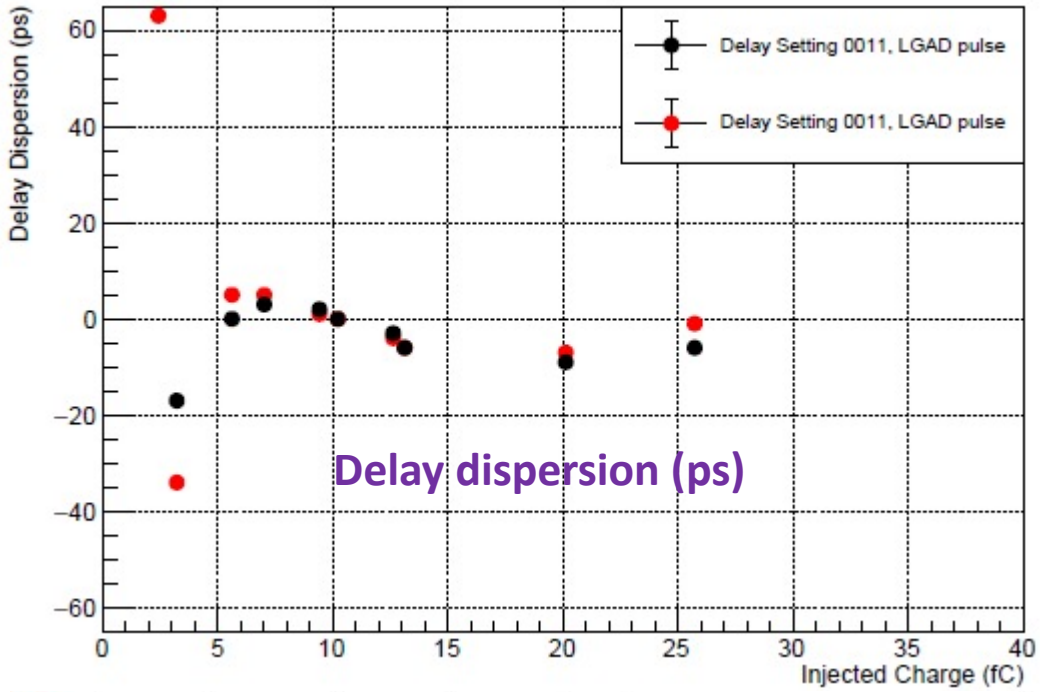
"High power"

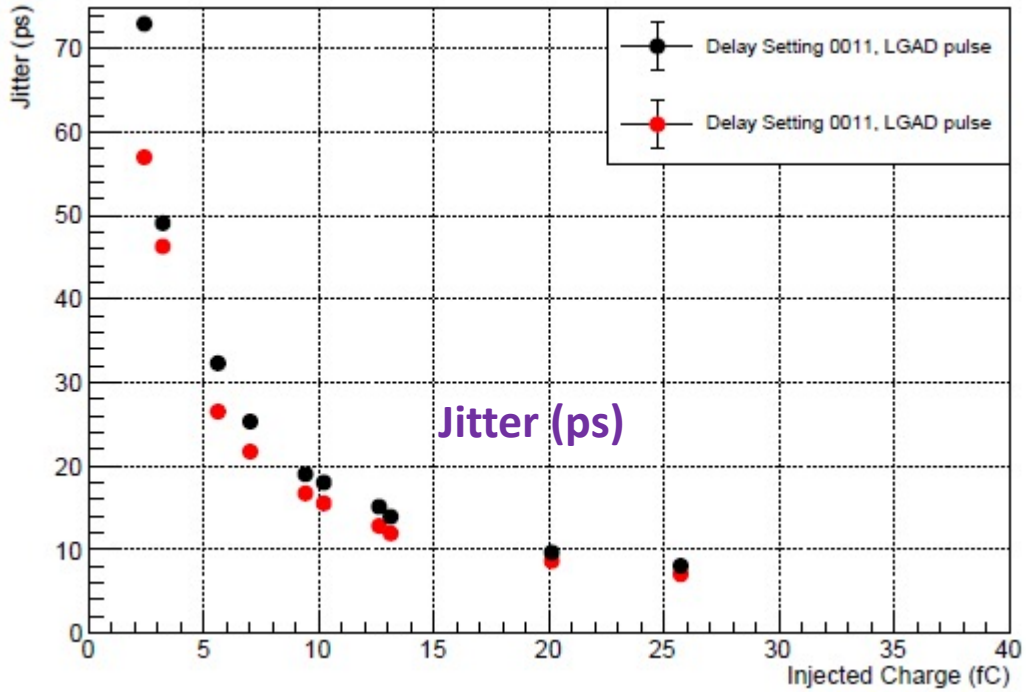
Input transistor current = 820 uA

Delay setting = 0011

Qin (fC)	Delay dispersion (pS)	Jitter (pS)
2.4	+63	57
3.2	-34	46.3
5.6	+5	26.5
7.0	+5	21.7
9.4	+1	16.7
10.2	(0)	15.5
12.6	-4	12.8
13.1	-6	11.9
20.1	-7	8.6
25.7	-1	7.0

Delay dispersion ~15 ns pk-pk. Jitter reduced with higher power.





Input transistor current = 520 uA

Input transistor current = 820 uA

“Fast” input pulse (FWHM ~ 0.3 ns instead of ~ 0.6 ns for LGAD pulse)

Input transistor current = 520 uA
Delay setting = 0010

Qin (fC)	Delay dispersion (pS)	Jitter (pS)
2.4	+119	63
3.2	-5	42.3
5.6	+9	27.1
7.0	+9	22.0
9.4	+2	16.9
10.2	(0)	15.5
12.6	-6	12.8
13.1	-9	12.4
16.3	-13	10.4
25.8	-13	7.0

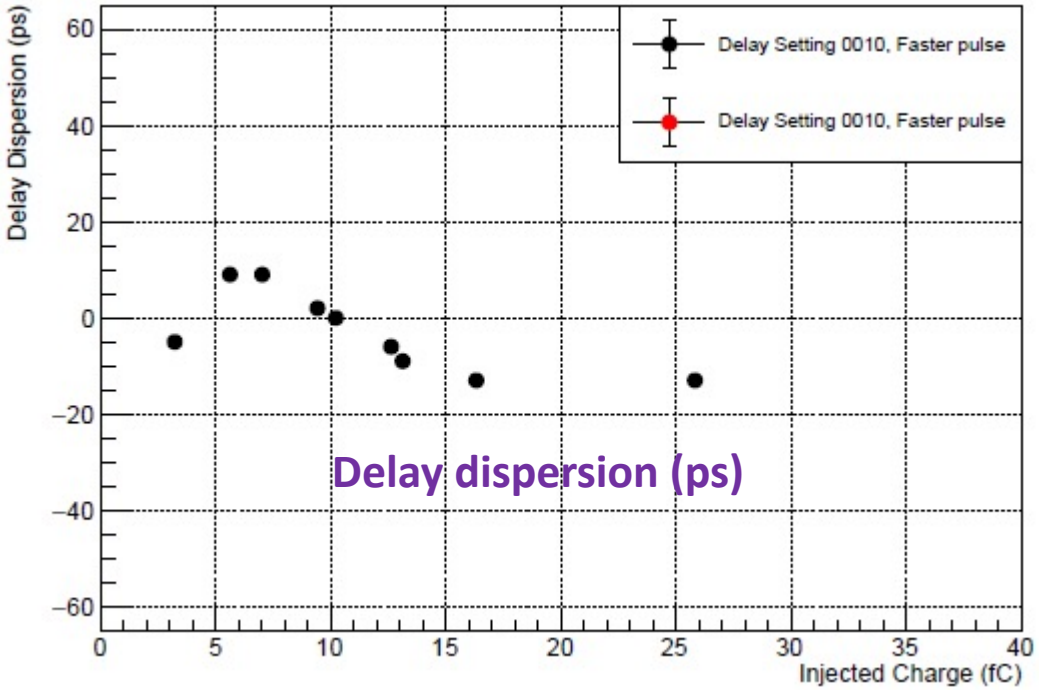
← **~13% lower jitter**

Input transistor current = 820 uA
Delay setting = 0010

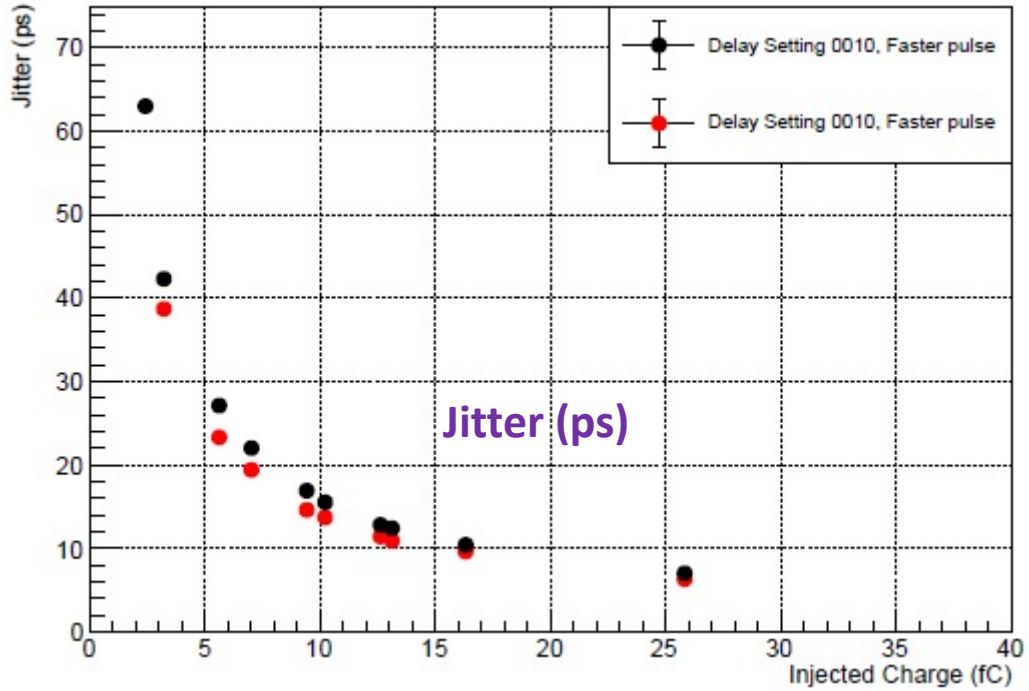
Qin (fC)	Jitter (pS)
2.4	
3.2	38.7
5.6	23.3
7.0	19.4
9.4	14.6
10.2	13.7
12.6	11.4
13.1	10.9
16.3	9.6
25.8	6.3

Jitter measured for a “fast” pulse will be lower than for realistic detector pulse shape!

“Fast” pulse



Input transistor current = 520 uA



Input transistor current = 520 uA

Input transistor current = 820 uA

Deadtime measurement

Measure Delta T (change from nominal measured time) of a 7 fC signal pulse when another pulse of amplitude Q is injected a given time before the signal:

Q arrives 20 ns before signal

Q (fC)	Delta T (ps)
0	0
7	-6
14	-19
21	-24
28	-41
35	-46

Q arrives 25 ns before signal

Q (fC)	Delta T (ps)
0	0
7	-3
14	-3
21	-8
28	-8
35	-10

If a pulse is injected 11 ns before the signal, the signal measurement is not made.
If a pulse is injected 30 ns or more before the signal, it has *no significant effect*.

CFD is ready to make another measurement in 25 ns!

Effect of input capacitance on delay dispersion, jitter

"LGAD-shape" injected pulse: reduce Cin from 3.400 pF to 2.850 pF

Input transistor current = 520 uA

Delay setting = 0011

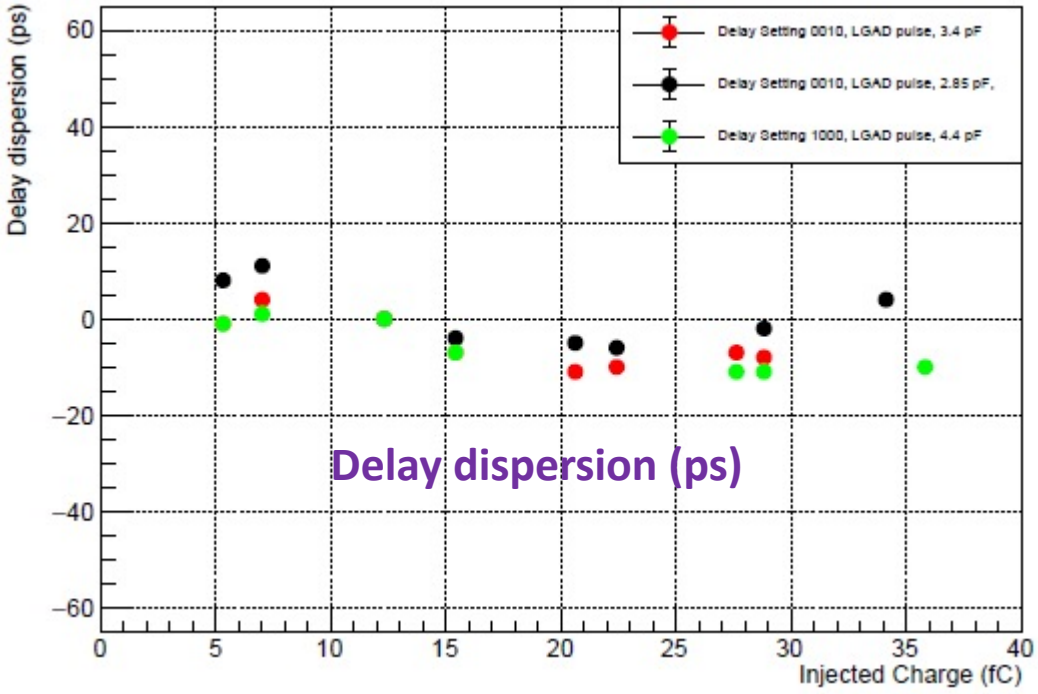
Qin (fC)	Delay dispersion (pS)	Jitter (pS)
5.3	+8	29.4
7.0	+11	22.0
12.3	(0)	13.1
15.4	-4	11.0
20.6	-5	
22.4	-6	7.9
28.8	-2	6.4
34.1	+4	

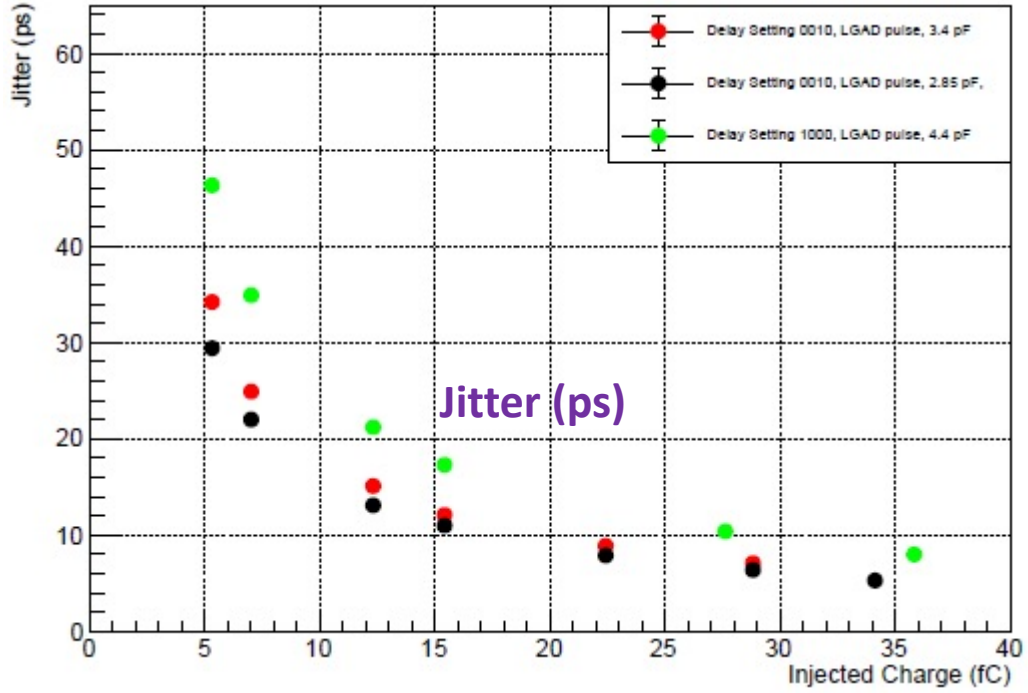
"LGAD-shape" injected pulse: increase Cin from 3.400 pF to 4.400 pF

Input transistor current = 520 uA

Delay setting = 1000 ← **Larger Delay setting to optimize for slower pulse**

Qin (fC)	Delay dispersion (pS)	Jitter (pS)
5.3	-1	46.3
7.0	+1	34.9
12.3	(0)	21.2
15.4	-7	17.3
27.6	-11	10.4
28.8	-11	
35.8	-10	8.0





LGAD-like pulse

Input transistor current = 520 uA

Cin = 2.85 pF, Delay setting 0010

Cin = 3.40 pF, Delay setting 0010

Cin = 4.40 pF, Delay setting 1000

Summary and next steps

- Timing is an enabling technology for future experiments
  - Future tracking detectors will be required to have significant timing precision, 10-30 ps per hit
- Good performance for the first generation of FCFD chip produced in TSMC 65nm technology node
  - Precise measurements and calibrations of the chip on a bench, stable operations, low dead time
  - Consistent with simulations: ~30 ps at 5fC, and < 10 ps at 30 fC, with LGAD-like pulses
- Test beam and beta-source measurements with connected LGAD sensors will follow in Fall/Winter 2021