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HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter

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For the CMS HGCAL, the final version of the 72-channel front-end ASIC (HGCROC3) was submitted in December 2020. HGCROC3 includes low-noise/high-gain preamplifier/shapers, and a 10-bit 40 MHz SAR-ADC, which provides the charge measurement over the linear range of the preamplifier. In the saturation range a discriminator and TDC provide the charge information from TOT (200ns dynamic range, 50ps binning). A fast discriminator and TDC provide timing information to 25ps accuracy. The chip embeds all necessary ancillary services: bandgap circuit, PLL, threshold DACs. We present the experimental results on the latest and final version HGCROC3 received in April 2021.

Summary (500 words)

The HGCROC3 is the final ASIC designed to readout the future High Granularity Calorimeter (HGCAL) of CMS, which will consist of hexagonal silicon sensors for a large part. The HGCAL is designed by the CMS collaboration to replace the existing endcap calorimeters for the High Luminosity phase of the LHC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. The HGCROC chip measures and digitizes the charge deposited in the silicon sensors pads, provides a high precision measurement of the time of arrival (ToA), and transmits the digitized data to the back-end electronics. It also computes, every bunch crossing, digital sums of neighbouring channels which are compressed and then transmitted to the concentrator ASICs through 1.28 Gbps serial links in order to build trigger primitives. The requirements for the front-end electronics are extremely challenging, including dynamic range over 16 bit equivalent (0-10 pC), noise bellow 2500 electrons, high-precision timing information (25 ps) in order to mitigate the pileup effect under high luminosity conditions and low power consumption (below 15 mW/channel). The front-end electronics will face a harsh radiation environment which will reach 200 Mrad at the end of life and 1x10ˆ16 neq/cm^2. Beyond the analog performance, the chip embeds a large part of digital processing to manage the Trigger and the Data paths: a 2-stage memory buffering is implemented with DRAMs to accommodate the 12.5 ms L1 trigger latency and the readout buffering (respectively 512 and 32 deep memories). The radiation hardening against SEE is done by triplicating all the control logic and the ASIC parameters: each clock cycle, state machines and counters are refreshed with a majority voter. For the data path, a SECDED Hamming algorithm is applied before the L1 buffering. The ASIC outputs its data through six 1.28 Gbps serial links: four dedicated for the trigger path and the rest for the DAQ path. It has 72 channels and the analog chain is composed of: low noise and high gain preamplifier, shaper and a 10-bit 40 MHz SAR-ADC provide the charge measurement over the linear range of the preamplifier. In the saturation range of the preamplifier, a discriminator and a TDC provide the charge information from a Time-Over-Threshold over 200 ns dynamic range using 50 ps binning. A fast discriminator and another TDC provide timing information to 25 ps accuracy. The final HGCROC3 ASIC was submitted (130 nm node) in December 2020 and the first lab tests will start in May 2021. The talk will focus on the description of the main changes compared to the previous ASIC iteration, the problem seen and how they have been mitigated in the design. In addition to that, the talk will report on the first performance results in terms of noise, charge and timing, as well as the digital processing with the triplicated logic inside the ASIC.

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