First experimental results with the version TOFHIR2X of the front-end ASIC of the MTD/BTL detector in the CMS experiment

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TOFHIR2 is the front-end ASIC for the barrel timing layer (BTL) of the MIP timing detector for the CMS upgrade for HL-LHC, aiming at 30-60 ps resolution throughout HL-LHC lifetime. The BTL consists of LYSO:Ce crystals coupled to SiPMs which will suffer radiation damage. Relative to the first version of the front-end ASIC (TOFHIR2A), TOFHIR2X implements improved circuitry for mitigation of the SiPM dark count noise (DCR) as well as a new current mode discriminator. We present an overview of the TOFHIR2 requirements and design, simulation results and the first measurements with TOFHIR2X silicon samples associated to LYSO/SiPM prototype sensors.

Summary (500 words)

The MIP Timing Detector (MTD) will provide timing of charged particles with high precision allowing to extend to the time domain the association of charged particles to the ˜200 concurrent proton collision vertices occurring at each bunch crossing in the High-Luminosity LHC (HL-LHC).

The MTD will consist of barrel and endcap timing layers, BTL and ETL respectively. The BTL is a thin standalone detector based on scintillation LYSO:Ce crystal bars read-out on both ends by silicon photomultipliers (SiPMs). The full BTL detector has about 330 thousand SiPM channels.

Dedicated ASIC electronics will be used to readout the SiPM arrays. The readout solution uses the new TOFHIR2 (Time-of-Flight at High Rate) chip. The main requirements for the BTL electronics are: (1) to measure the timing of minimum ionizing particles (MIP) with a precision of 30 (65) ps at the beginning (end) of HL- LHC; (2) to provide a measurement of the signal amplitude with <5% precision for time-walk corrections. Additionally, the chip has to cope with a MIP input rate of 2.5 M hit/s corresponding to the expected maximum channel occupancy of 7% and to have an output bandwidth of 640 Mb/s. The chip should have a static power consumption lower than 15 mW per channel.

The ASIC has 32 channels, each channel containing one pre-amplifier, two post-amplifiers for timing and energy measurements, three leading edge discriminators, two time-to-amplitude converters (TAC) and one charge-to-amplitude converter (QAC) sharing one 40MHz 10-bit SAR ADC and local control logic. The input pre-amplifier provides a low impedance input to the sensor's current signal. The input current is replicated into three branches for timing, energy discrimination and charge integration.

Pulse filtering is included in the post-amplifiers to mitigate the deterioration of time resolution due to the large dark count rate (DCR) induced by radiation (up to 55 GHz) and due to pile-up of LYSO pulse tails. The filter creates an inverted and delayed replica of the input current that is added to the original signal. The processing is done in current mode which allows for large bandwidth in a simple implementation. The delay line is implemented as a set of RC nets with programmable taps.

The first full version of TOFHIR2 (32 channels and complete functionality) has been tested. The performance of TOFHIR2A match well the simulation expectations. The service blocks, digital readout, front-end amplifiers, DCR noise cancellation, TDCs and QDCs were validated. Successful TID and SEU radiation tests have been performed.

The second version, TOFHIR2X, has an improved version of the front-end amplifiers and DCR cancelation module, as well as fast current discriminators, instead of voltage discriminators, matching directly the current output of the pulse filters. Simulation results show that a time resolution of ˜23 ps (˜65 ps) at the beginning (end) of HL- LHC can be achieved (figure 1).

TOFHIR2X ASIC prototype will be received for testing by the end of May. At the conference first measurements with TOFHIR2X silicon samples associated to prototype LYSO/SiPM sensors will be presented.

Primary authors: ALBUQUERQUE, Edgar (PETsys Electronics); BUGALHO, Ricardo (PETsys Electron-

ics); FERRAMACHO, Luis (PETSys Electronics SA); FIRLEJ, Miroslaw (AGH University of Science and Technology (PL)); FIUTOWSKI, Tomasz Andrzej (AGH University of Science and Technology (PL)); FRANCISCO, Rui; GAL-LINARO, Michele (LIP Lisbon); IDZIK, Marek (AGH University of Science and Technology (PL)); MORON, Jakub (AGH University of Science and Technology (PL)); NIKNEJAD, Tahereh Sadat (LIP Laboratorio de Instrumentacao e Fisica Experimental de Part); OLIVEIRA, Luis (DEE, CTS-UNINOVA FCT-UNL, Caparica); RASTEIRO DA SILVA, Jose Carlos (LIP Laboratorio de Instrumentacao e Fisica Experimental de Part); VARELA, Joao (LIP Laboratorio de Instrumentacao e Fisica Experimental de Part); SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL)); SILVEIRA, Miguel (LIP Lisbon); SILVA, Rui (LIP)

Presenter: NIKNEJAD, Tahereh Sadat (LIP Laboratorio de Instrumentacao e Fisica Experimental de Part)

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