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FAST2: a new family of front-end ASICs to read out thin Ultra-Fast Silicon detectors achieving picosecond time resolution.

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We present the first results obtained with the FAST2 family of ASICs. The FAST2 ASIC family, designed in the 110 nm CMOS technology, has been optimized for the read-out of Ultra-Fast Silicon Detectors, aiming to achieve a combined total time resolution of less than 40 ps. In the FAST2 family, the ASIC (FAST2_A) presents 16 channels and has only the amplification stage with a timing jitter lower than 16 ps experimentally, and power dissipation of 1 mW/ch.

Summary (500 words)

FAST2: a new family of front-end ASICs to read out thin Ultra-Fast Silicon detectors achieving picosecond time resolution.

In this contribution, we present the first results obtained with the FAST2 family of ASICs. The FAST2 ASIC family, designed in the 110 nm CMOS technology, has been optimized for the read-out of Ultra-Fast Silicon Detectors, aiming to achieve a combined total time resolution of less than 40 ps. The FAST2 family comprises 3 different ASICs: two of them (FAST2_EVO1, FAST2_EVO2) have 20 channels, and use the amplifier-comparator architecture, while the third ASIC (FAST2_A) has 16 channels and has only the amplification stage. In this contribution, we present the first results of the FAST2_A ASIC.

The FAST2 prototypes have been designed in 110 nm CMOS technology with a power consumption of about 1 mW/channel.

The experimental results presented here have been obtained by coupling the FAST2_A ASIC with a UFSD and using several techniques to evaluate the combined performances.

The setup includes a Large Scanning-TCT with a 1060 nm wavelength laser diode and a tunable laser width between 350 −4000 ps. The laser intensity is tuned in such a way to generates the light needed to produce a MIP. Experimentally, several output signals are acquired to analyze the timing jitter and rising time over the input charge. The UFSD under test has a capacitance of 3.4 pF, and a generated charge range from 5 to 30 fC depending on the bias voltage operation range (120 to 240 V). At these operation conditions, the front-end architecture produces a time jitter lower than 30 ps for input charges higher than 8 fC, as shown in the experimental results. The ASIC prototype achieves a jitter lower than 15 ps with an input charge of a MIP equal to 17 fC. The Near-end and Far-end crosstalk caused due to the mutual capacitance and inductance among 16 electronics channels come out as a time derivative of the transmitter channels. The crosstalk components are attenuated more than 23 dB at 50 ☒ of load.

The experimental results discussed in the conference presentation will include results obtained with a beta telescope, where 2 MeV electrons from the Sr90 beta source are used to evaluate the performances. These results include the corrections due to time walk and the uncertainties introduced by the MIP non-uniform energy deposition, called Landau noise σlandau.

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