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A Sub-Picosecond Digitally-Controlled Phase Delay

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The use of precision timing measurements will be a major tool at the HL-LHC, where it will be used to suppress pile-up and to search for long-lived particles. To control a reference clock with sub-picosecond accuracy, we have fabricated in the TSMC 65nm process a digitally controlled phase shifter. It is composed of a chain of 66 cells, each with a digitally controlled planar wave guide with either a short or long delay. With this a reference clock's phase can be controlled to a precision of 200 fs with dynamic range of 13 ps.

Summary (500 words)

The digitally-controlled phase shifter (DCPS) is an integrated direct digital-to-phase converter with the purpose of enabling accurate and predictable phase adjustment in real time with high efficiency, while occupying a minimal physical footprint.

The operating principle of the DCPS is shown in the attached figure and is best explained by considering the physical characteristics of a TEM wave propagating in a transmission line. In an ideal loss-less transmission line, the TEM mode features a linear dispersion relationship which is equivalent to a constant, frequency-independent time delay.

In order to adjust the propagation speed in the transmission line we break the line into small delay cells. Each cell has a coplanar waveguide structure, with two pairs of parallel ground lines. By switching the return current between the two lines, each unit delay of the line can adjust the equivalent inductance and hence the propagation speed and each delay cell operates in two distinct modes: In the "low-delay"mode the L switches are on and the inner lines carry the return path minimizing the unit inductance of the cell. In the "high-delay" mode the L switches are deactivated. As a result the return path flows through the outer lines, maximizing the inductance.

In order to maintain a true-delay line with minimal dispersion, we simultaneously adjust the unit capacitance in each cell to maintain a stable $\sqrt{\mathrm{L}/\mathrm{C}}$ ratio. For this purpose, we introduce a shunt capacitor in parallel with the signal line. In the low-delay mode, where the inductor is small, the capacitor switch is off, resulting in the inherent capacitance of the structure. In the high-delay mode, the capacitor is added to balance the higher inductance.

The DCPS had been tested with 0.5 to 10 GHz RF signals and with a 160 MHz digital clock. It has shown excellent linearity in the delay, seen in the attached figure, and 4 dB signal attenuation up to 7 GHz, in good agreement with the device simulation.

In our presentation we will describe the design of the delay cell, the results we have obtained with the first version, our plans to extend the dynamic range of the device and the steps we are following to make it radiation tolerant

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