Test results of RD53B chips
for ATLAS and CMS Phase-2 Pixel Upgrades

Dominik Koukola on behalf of the RD53 collaboration

TWEPP-2021

Online event, 20 – 24 September 2021

RD53 collaboration

- **Joint effort between ATLAS and CMS with 24 collaborating institutes**

- **Established in 2013 to develop readout chips for the HL-LHC pixel detectors**

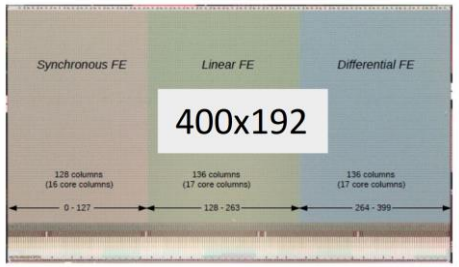
- **Collaboration is in charge of**
  - Characterization of **65 nm CMOS technology** in radiation environment
  - Design of rad-hard IP library
  - Design and characterization of **half-size pixel chip demonstrator (RD53A)**
  - Design of pre-production (**RD53B**) and production (**RD53C**) pixel readout chips

RD53 requirements	
Chip size	2x2 cm^2
Pixel size	50x50 μm^2
Hit rate	3 GHz/cm^2
Trigger rate	1 MHz
Trigger latency	12.5 µs
Min. threshold	600 e-
Radiation tolerance	0.5 Grad
Power consumption	< 1W/cm^2

RD53B chips

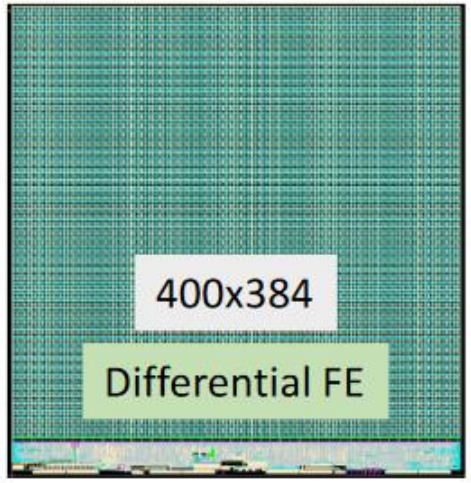
- **RD53B chips are full-size pre-production chips**
- **ATLAS and CMS chips are two instances of the same design**
  - Main difference is size and Analog Front-End (FE)

- **RD53B-ATLAS has been extensively tested since summer last year**
- **RD53B-CMS wafers received beginning of September, expect first results next week or two**



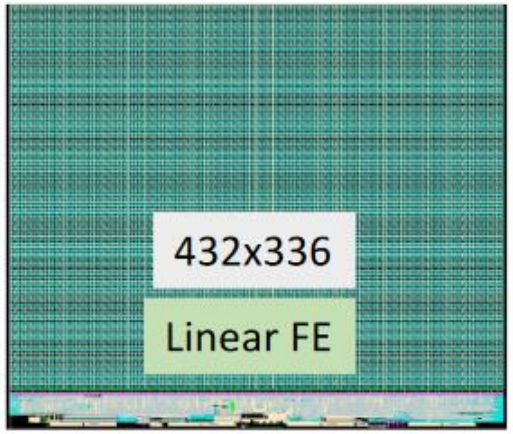
RD53A

- Submitted in Aug 2017



RD53B-ATLAS (ITkPixV1)

- Submitted in March 2020

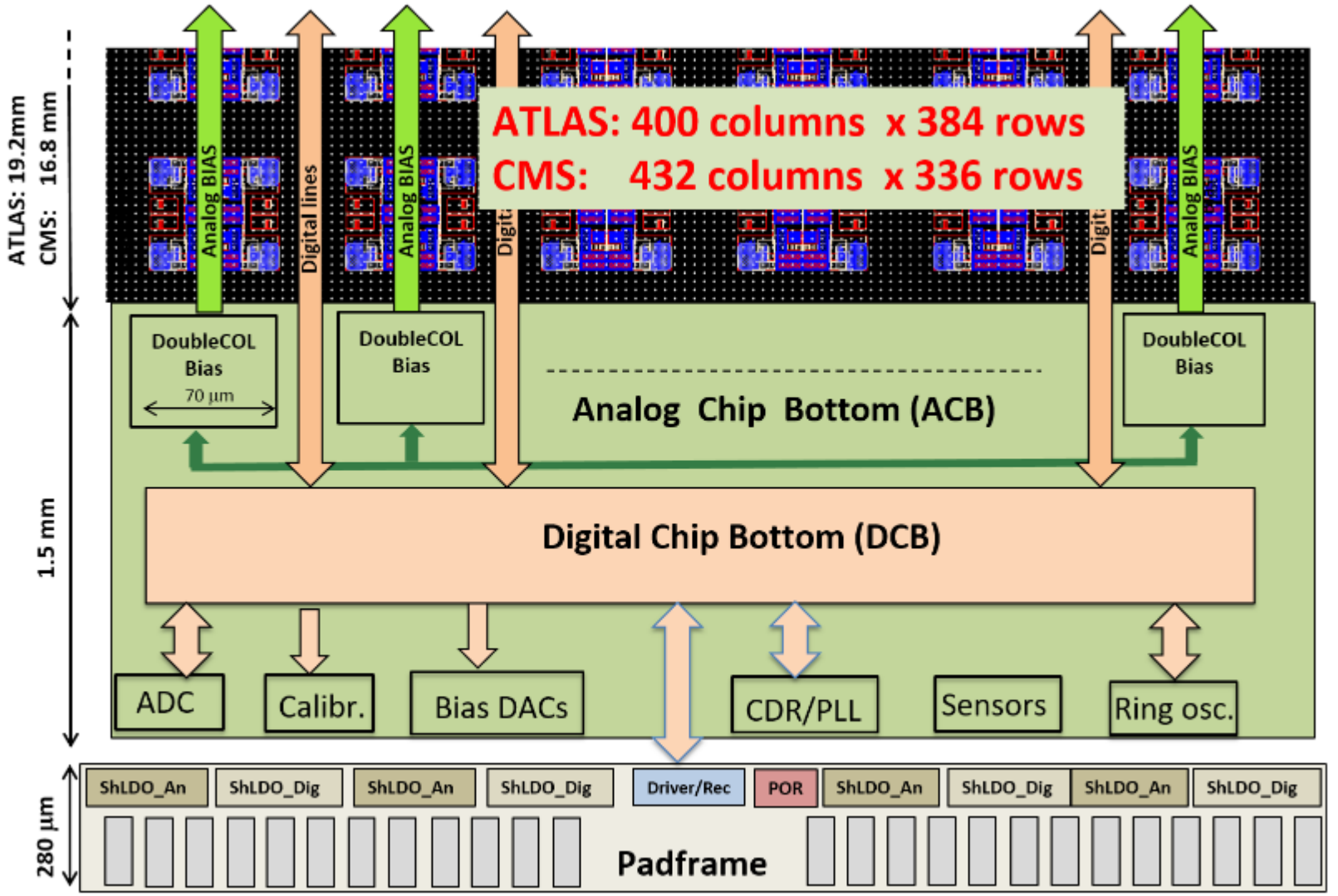


RD53B-CMS (CROCv1)

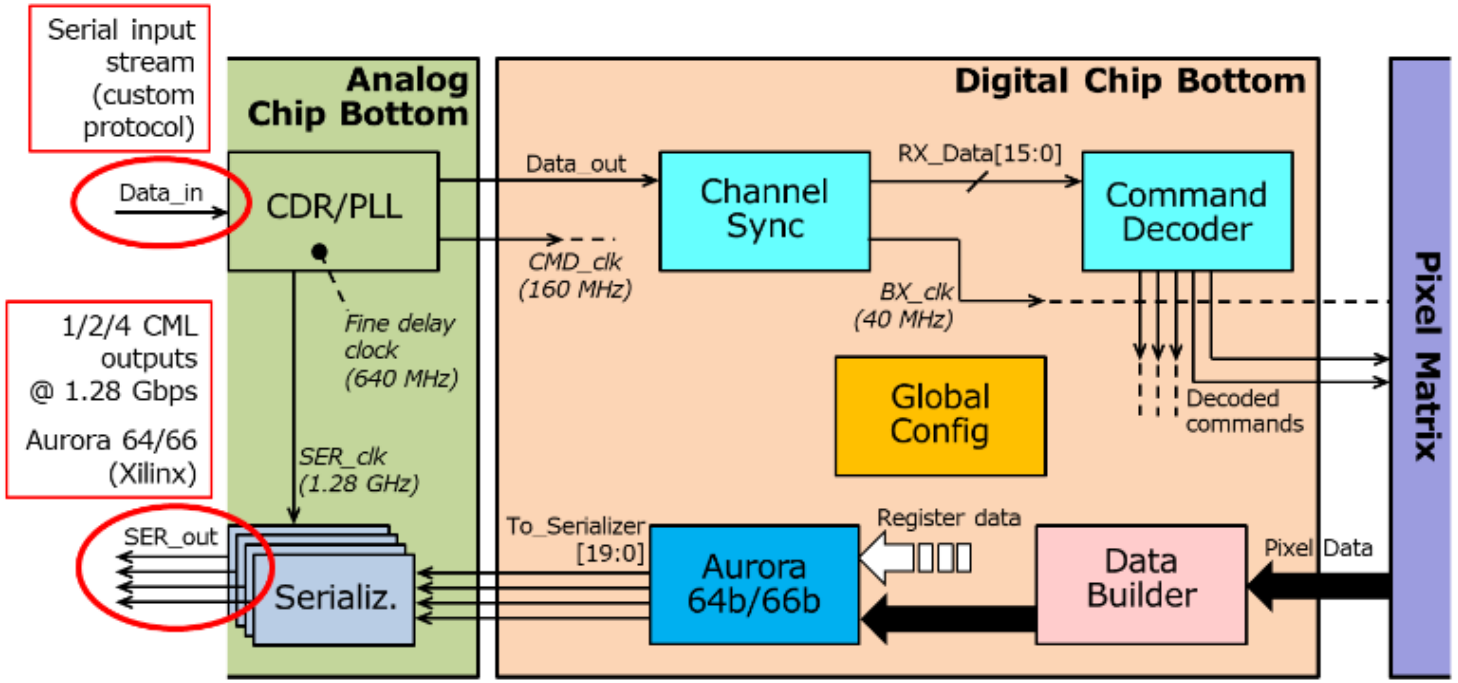
- Submitted in June 2021

RD53C-ATLAS: Q1 2022
RD53C-CMS: Q2-3 2022

RD53B functional diagram



Data flow architecture



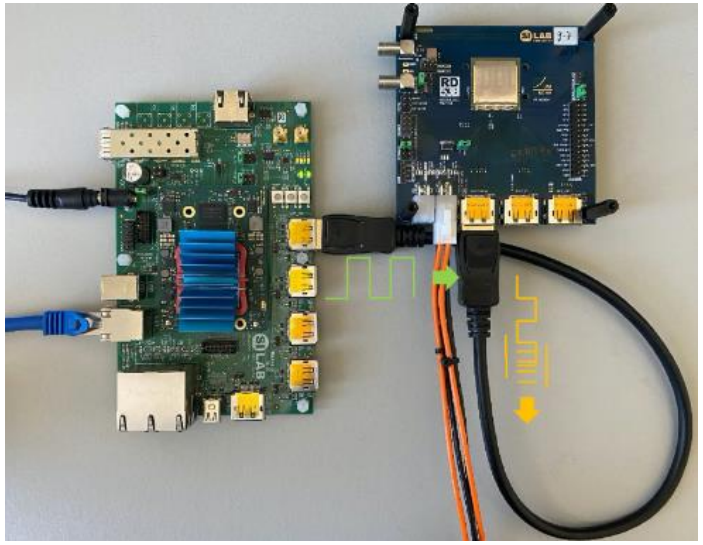
- Hits are stored as ToT (Time over threshold) associated to a timestamp
- Each pixel has 8x 4 bit ToT memories
- Token-based read out of hits along core columns
- Data processing, buffering, formatting event building before final readout

- **Command, control and timing are provided by single 160 Mbit/s differential link**
- **Readout via serial links (1-4) @ 1.28 Gbit/s using Aurora 64b/66b encoding**

More in the next talk by Attiq Ur Rehman
Performance simulations and characterization of RD53 pixel chips for ATLAS and CMS HL-LHC upgrades
https://indico.cern.ch/event/1019078/contributions/4443947/

RD53B (ATLAS) chip testing

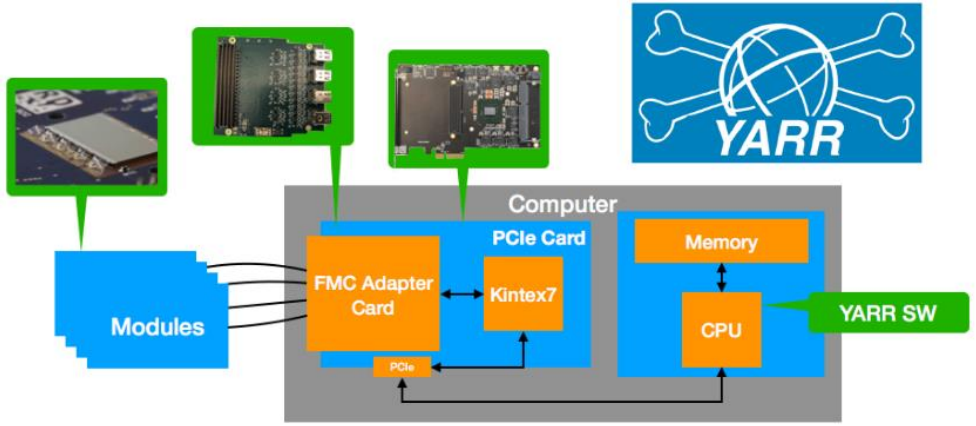
BDAQ53



https://gitlab.cern.ch/silab/bdaq53

- Custom board with commercial FPGA plug-in
- Ethernet communication to PC
- Python based SW
- Lightweight readout system specifically targeting chip testing and characterization

YARR

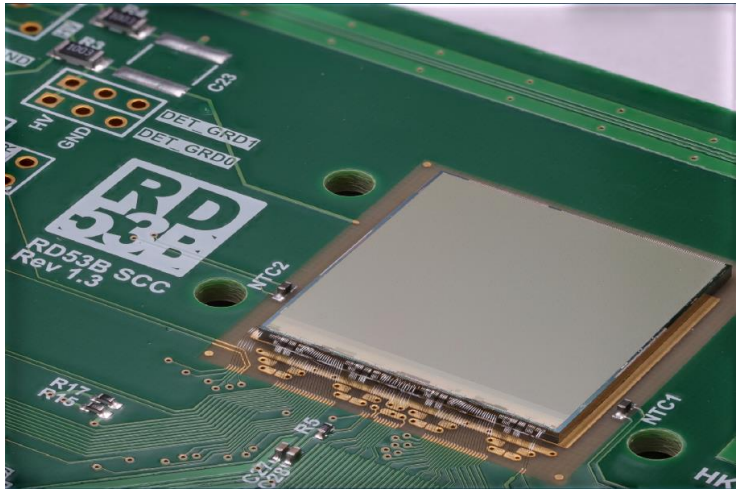


https://gitlab.cern.ch/YARR/YARR

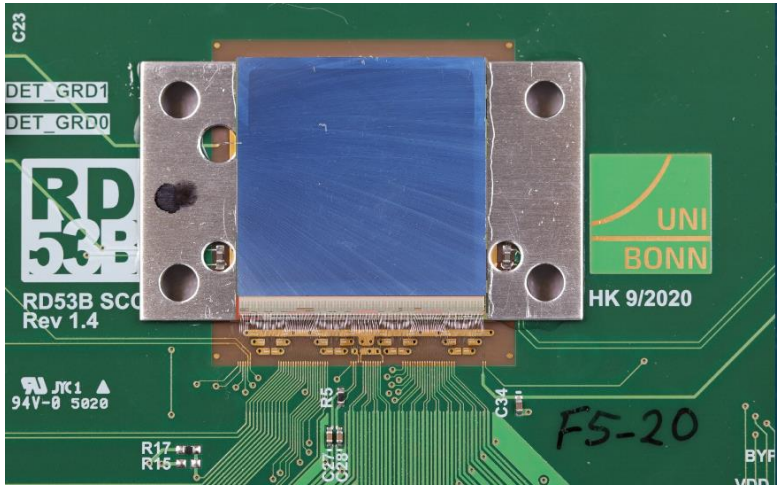
- Commercial PCIe FPGA board with custom FMC adapter card
- PCIe communication to PC
- C++ based SW
- Hardware agnostic SW aimed to grow from chip testing to detector operation

RD53B single chip cards and modules

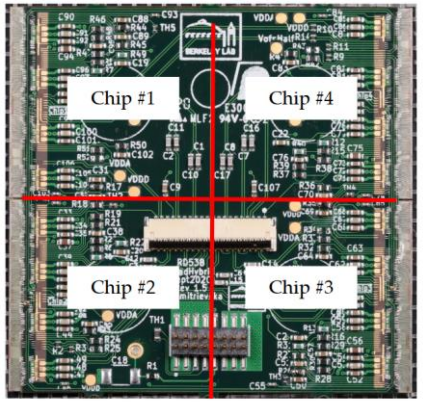
Bare ItkPixV1 on single chip card (SCC)



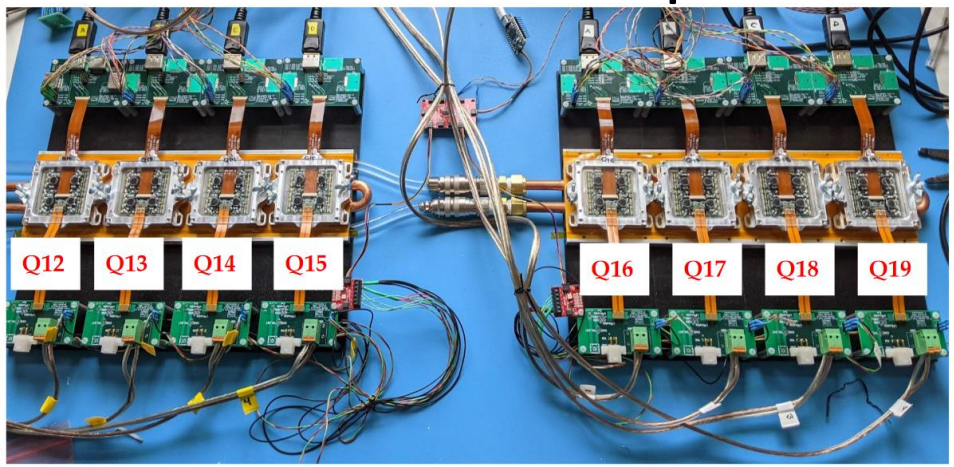
ItkPixV1 with 3D sensors on top



Digital quad module

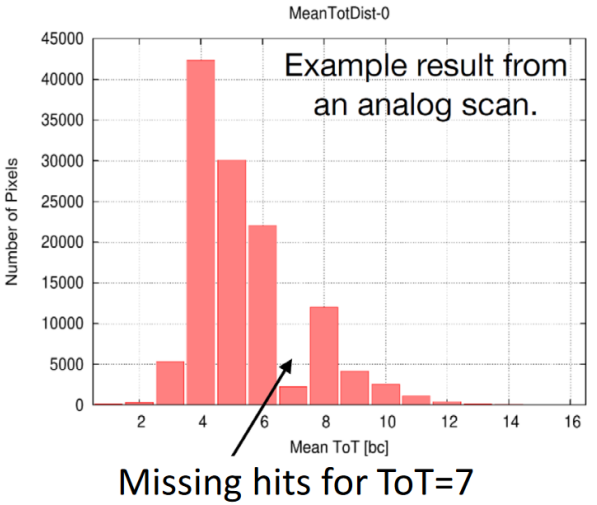


Readout chain of 8 ItkPixV1.1 quad modules



High current due to Multi-bit ToT latch

- **Upon power up observed abnormally high digital current (2-3A instead of 200mA)**
  - Bug found in custom 4-bit latch used for the first time due to area congestion
  - High current consumption when inputs differ from stored values in latched state
  - Also causes hit loss for some ToT values



- **Most blocks and functionalities could be tested with this version**
  - System testing of serial power chains were not possible

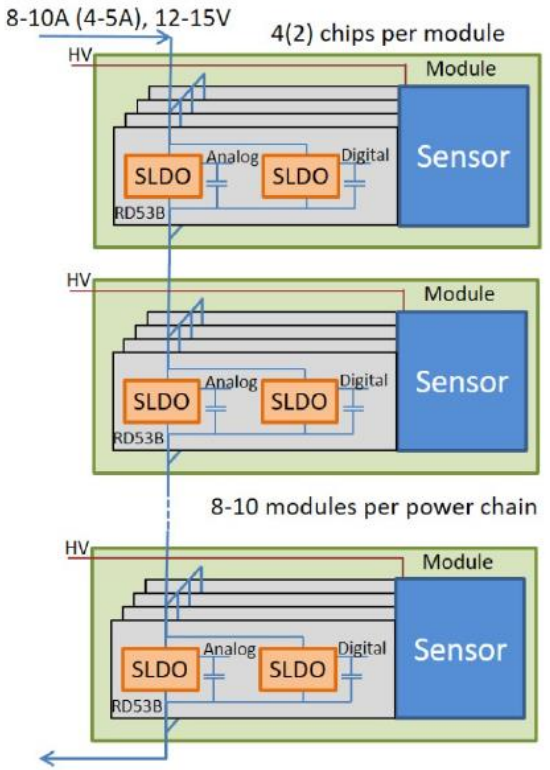
- **Patch in metal layer (ITkPixV1.1)**
  - Fix high digital current and hit-loss by transforming multi-bit latch into single-bit latch
  - Only required changes two metal layers
  - Patched chip is being used for system level tests and ATLAS ITk pre-production

- **Issue has already been fixed in RD53B-CMS chip with new multi-bit latch design**

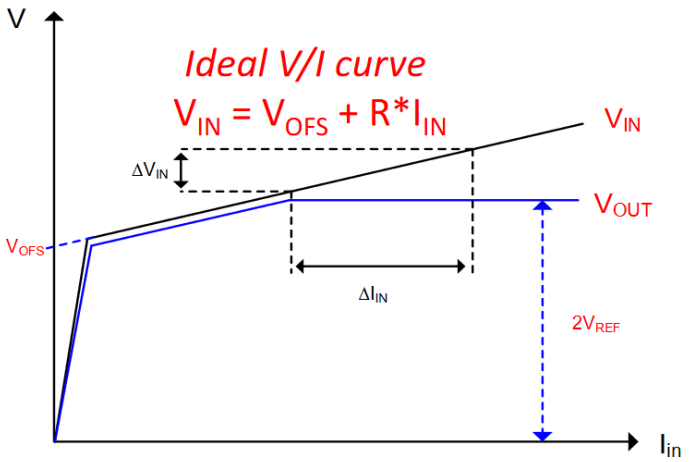
Serial powering

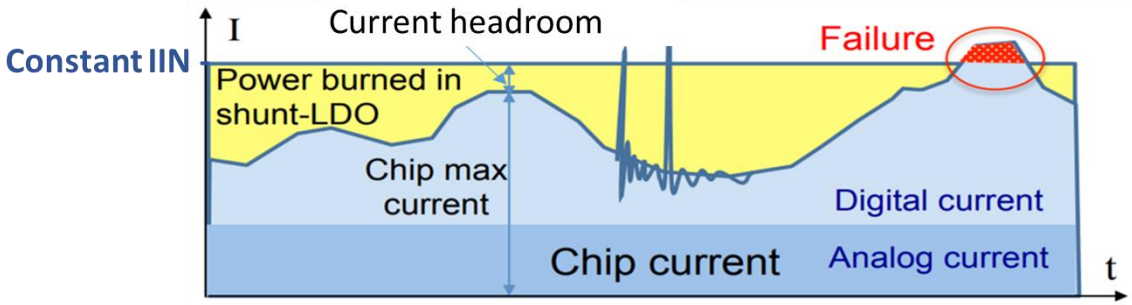
ATLAS and CMS will use the serial powering scheme to power the pixel chips

- **Enables large reduction in mass of services**
- **Based on on-chip Shunt-LDO regulators (1 for analog, 1 for digital domain)**
  - ➢ Combination of linear voltage regulator (for Vout) and shunt regulator (for VIN and shunt current)
- **Constant input current IIN is shared among chips on the same module**
  - ➢ Enough IIN needs to be supplied to satisfy highest load plus some headroom (10-20%) for stable operation



- ❑ V/I curve parameters (Vofs, slope) defined by external resistors
- ❑ Vout is configurable via chip registers



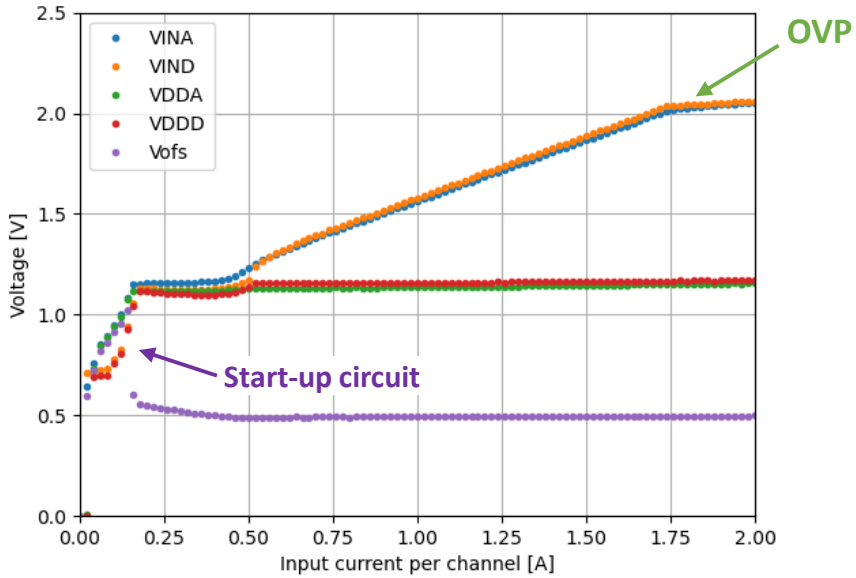


Example current consumption of one readout chip

Shunt-LDO tests

ItkPixV1 and V1.1 tests show that Shunt-LDO works well

ITkPixV1.1 measurement at -10C



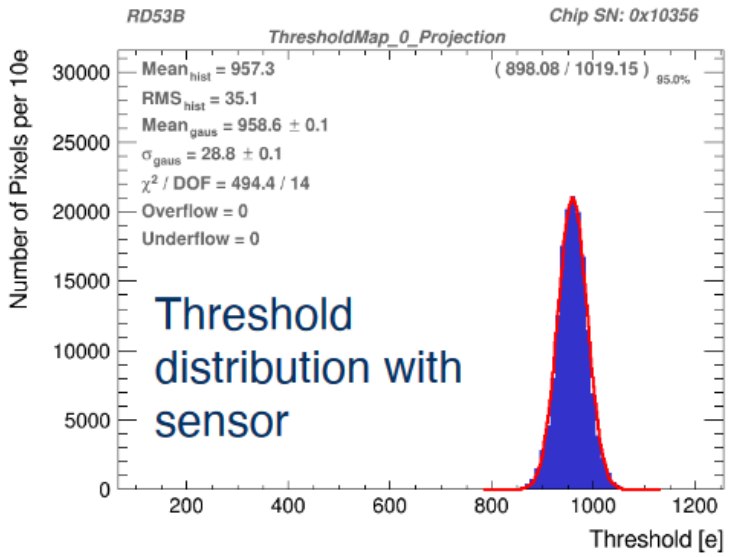
- **Improvements in V/I behavior**
  - Linear fit parameters of VIN close to theoretical values
  - Reduced Vout dependence on VIN
- **Improved start up behavior with added start up circuit**
  - Boosts Vofs, which helps Shunt-LDO start up at low VIN
  - Also validated after 1 Grad and -40 ℃
- **New protection features**
  - **Over-voltage protection (OVP)**: clamps VIN to 2V (internally)
  - **Under-shunt protection (USP)**: Vout decreases in case shunt current goes too low
- **First system tests with pixel modules show promising results (good current sharing)**
  - Minor instabilities detected in one control loop, already fixed in design and can be mitigated by ext. configuration

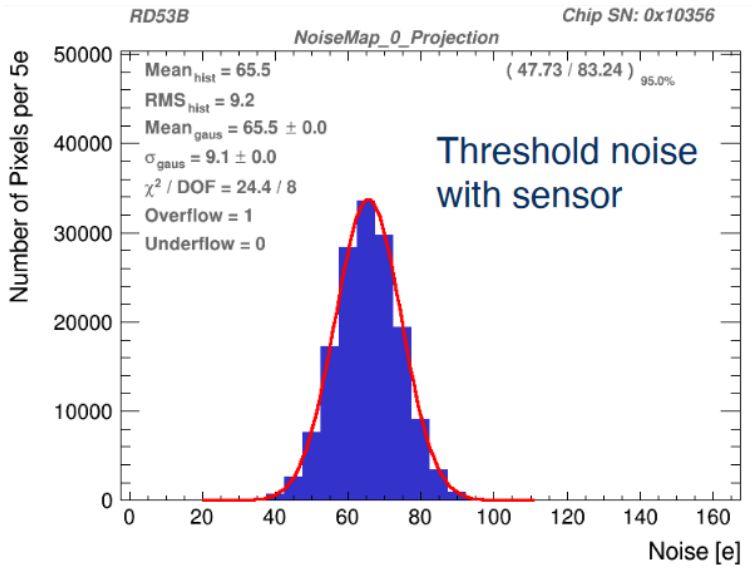
Differential FE

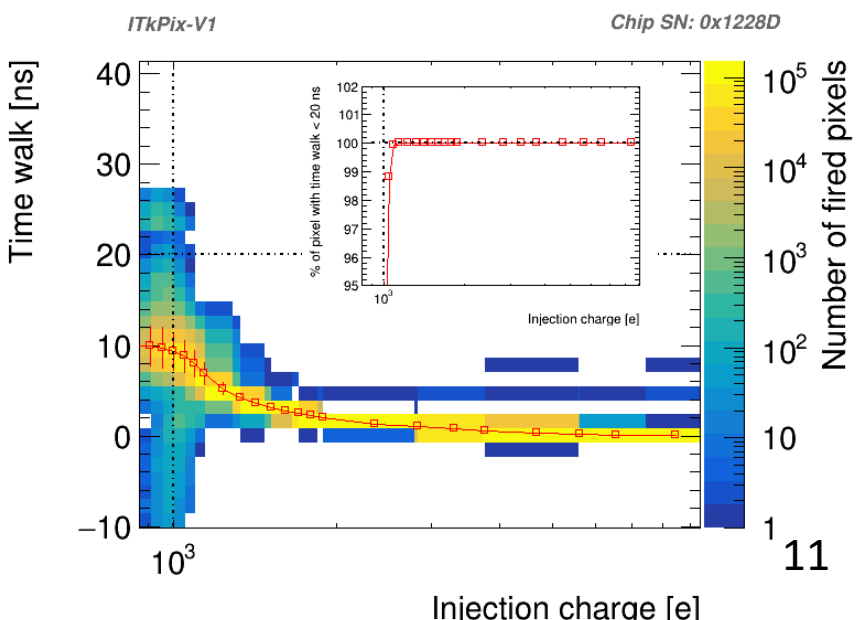
Differential FE has been thoroughly tested and shows very good results both bare and with sensor

- Threshold and noise are homogeneous over pixel matrix
- With tuned threshold to 1000e and with 150 µm Micron sensor:
  - ➢ **Very low tuned threshold dispersion** of ~30e
  - ➢ **Low mean noise** of ~65e
- **Low time walk of below 20 ns on bare chip**

  (20 ns estimated to be needed to stay in 25 ns bunch crossing taking into account clock delays, etc.)



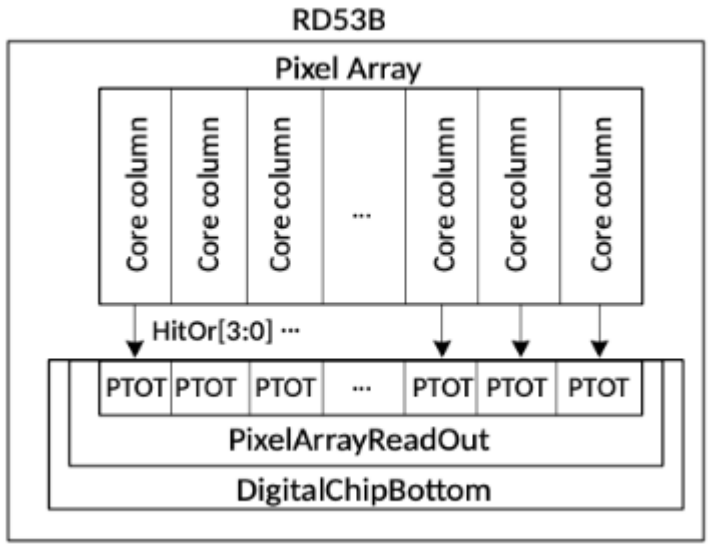


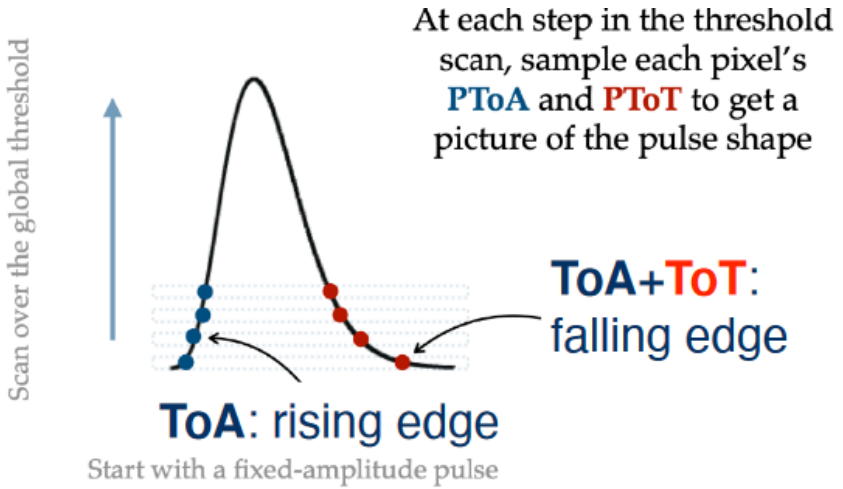


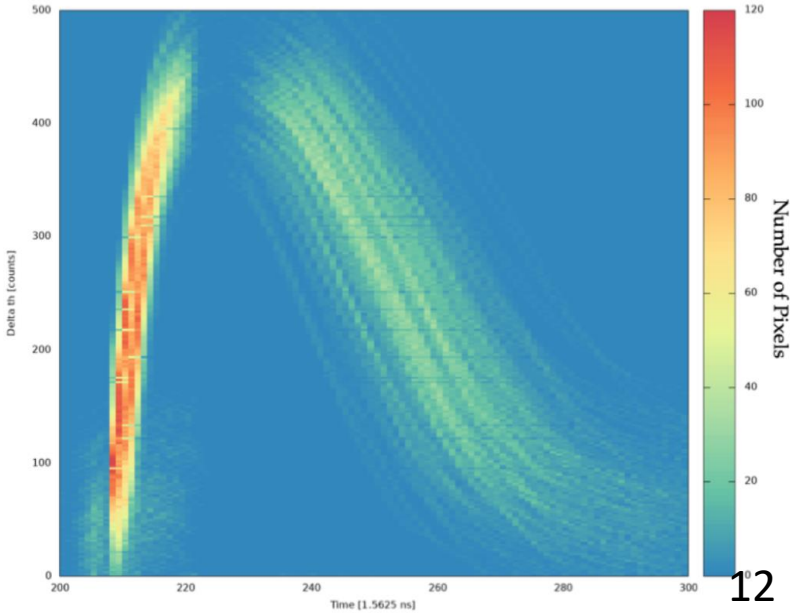
Precision TOT and TOA

New feature to measure precision time-over-threshold (ToT) and time-of-arrival (ToA) using 640 MHz clock

- Each core column has 4 PToT and PToA counters connected to HitOr bus (OR of all pixel discriminators)
- Triggered via normal path, but only column information known
  - Can measure four pixels per core column at a time
- **Can be used for precision measurements of FE like the signal profile and time walk**
  - Also as workaround for bug in pixel ToT memory



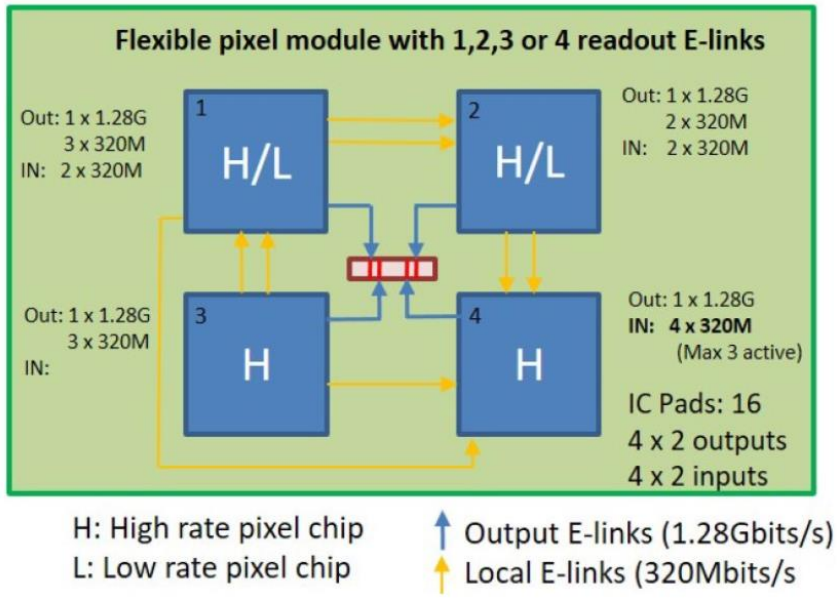




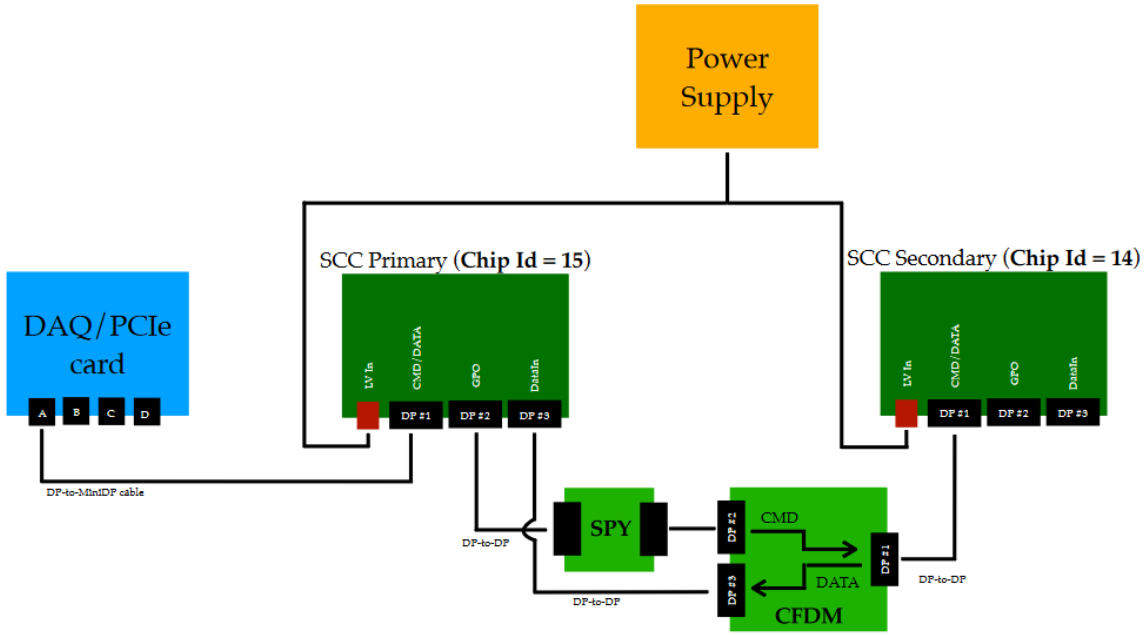
Multi-chip data Merging

- **RD53B supports multi-chip data merging for low-rate outer pixel layers**
  - Data from up to four chips is merged into one output elink
  - Secondary chips send data with 320 Mbit/s to primary chip, which merges data to 1.28 Gbit/s output link
- **Data merging successfully tested with two chips on single chip cards**
- **Tests with modules and four chips are planned**

Data merging scheme on a module



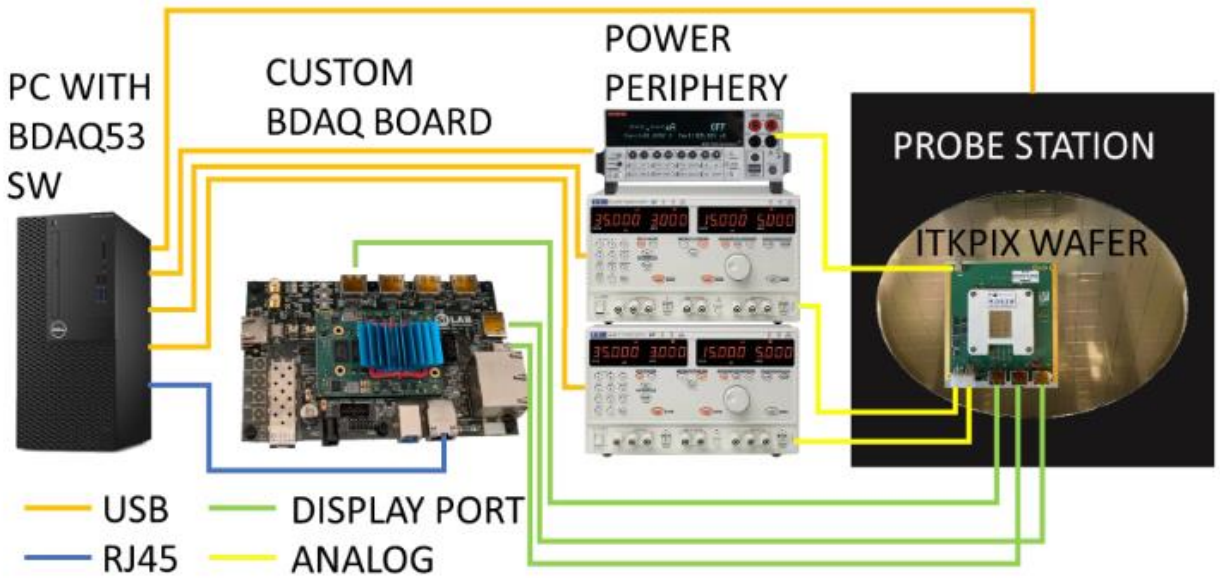
Test setup for data merging of two chips

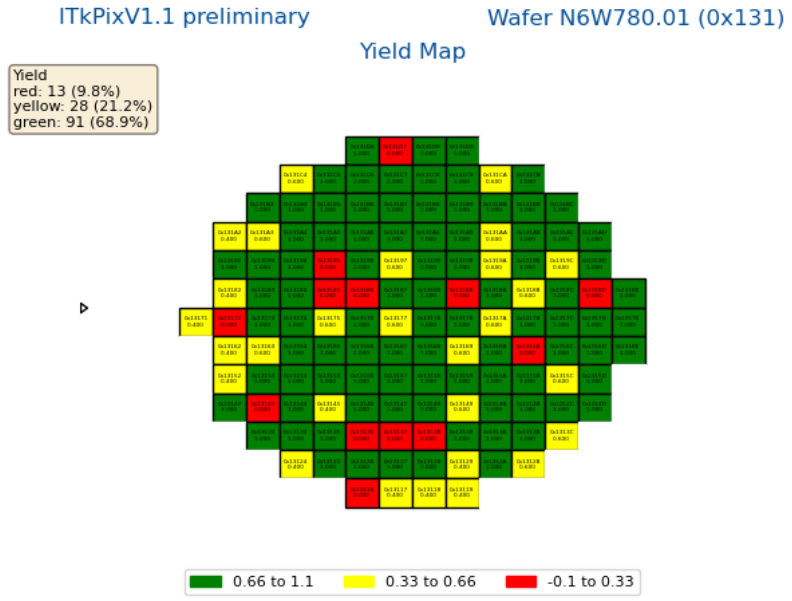


RD53B (ATLAS) Wafer Testing

- **Stable wafer probing procedure with tests covering most of the RD53B functionality** (powering, biasing and monitoring, communication, pixel matrix logic, AFE, ...)

- **15 wafers (~2000 chips) tested so far**
  - ➢ >85 % of chips are generally functional
  - ➢ Final yield will also be driven by system constraints (serial powering)





Radiation hardness and SEU tests

Irradiation campaigns

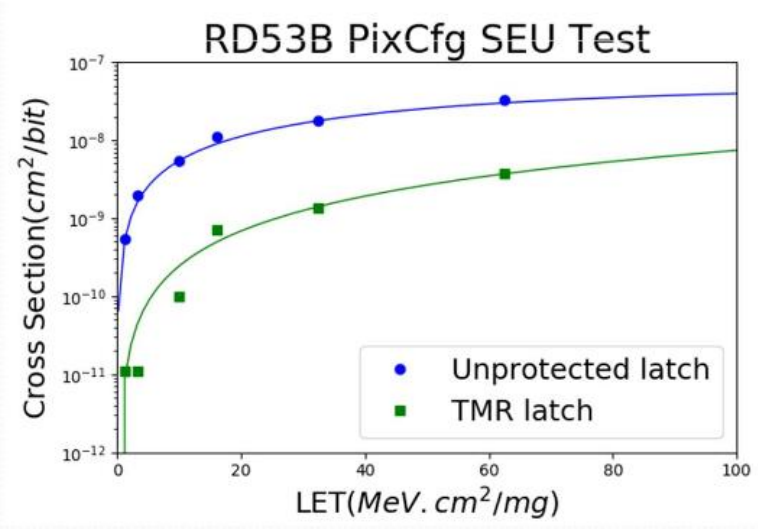
- Several x-ray irradiation campaigns performed
- Measurements suggest the chip is radiation hard **up to 1 Grad** (at -10 ℃ and 4 Mrad/h)
- Linear extrapolation of low-dose rate irradiations indicates **detector operation of up to 1 Grad or more should be possible**
- **Observed** differences in bias DACs correlated with metal thickness above the circuits
  - Suspecting different x-ray absorption due to metal

More in contribution by Maria Marionova
Radiation hardness of the ITkPixV1 and RD53A chips
https://indico.cern.ch/event/1019078/contributions/4443960/

And in contribution by Aleksandra Dimitrievska
Low dose rate irradiation of the RD53A chip with Kr-85 beta source
https://indico.cern.ch/event/1019078/contributions/4444329/

SEU tests

- Different campaigns with heavy ions and protons
- Measurements show improved SEU tolerance due to introduced triplication



More in contribution by Jelena Lalic
Single Event Effects on the RD53B Pixel Chip Digital Logic and On-chip CDR
https://indico.cern.ch/event/1019078/contributions/4444326/

Summary

RD53B pre-production chips for ATLAS and CMS are two instances of the same design

RD53B-ATLAS (ITkPixV1/V1.1)

- Submitted in March 2020
- Found bug in ToT memory causing high current, but didn't prevent to characterize most of the chip
- Developed a patch by changing two mask layers => ITkPixV1.1 which is being used for system tests
- Testing is well advanced and chip is otherwise working fine ~ no show-stoppers
- Several tests, especially on system level (data merging, serial powering, ..) are planned

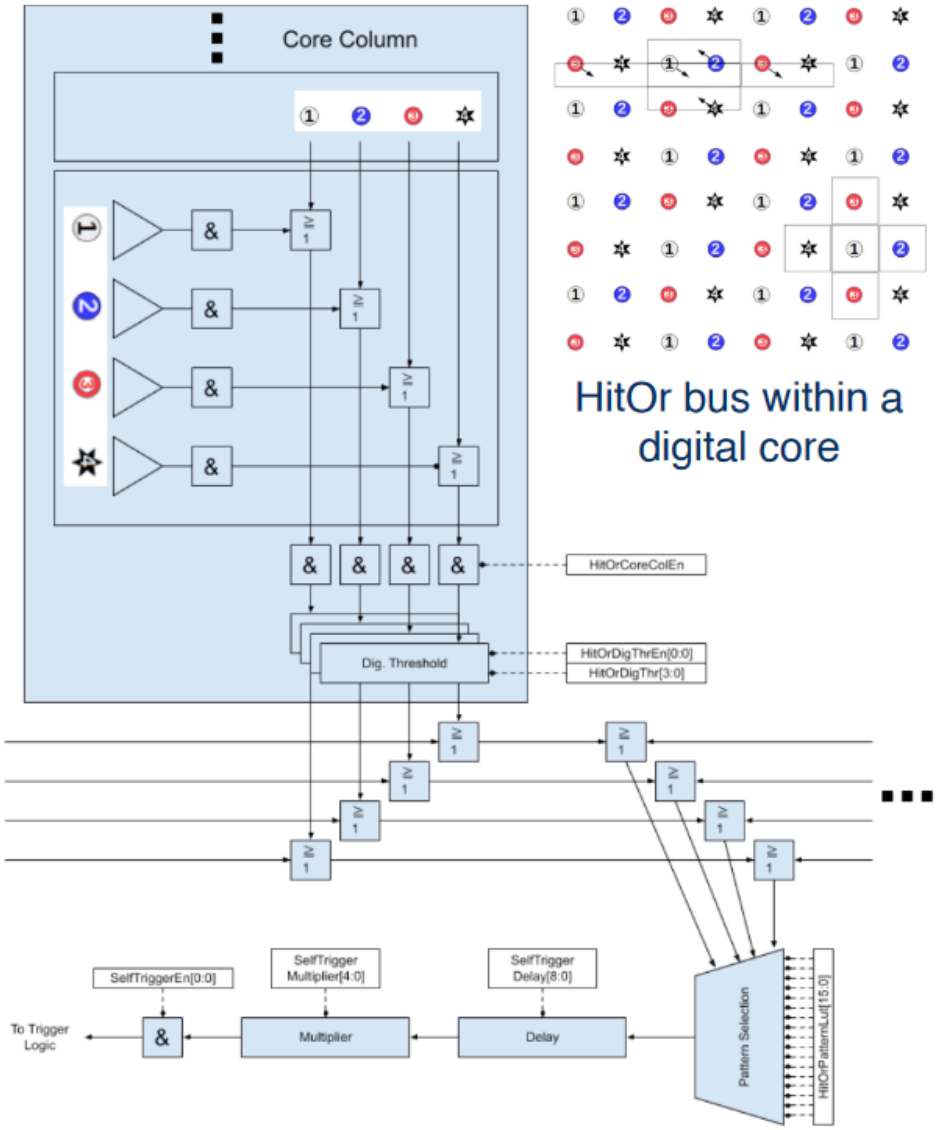
RD53B-CMS (CROCv1)

- Includes fixes of known bugs and improvements plus some additional features
- Wafers received beginning of September and testing expected to start end of next week

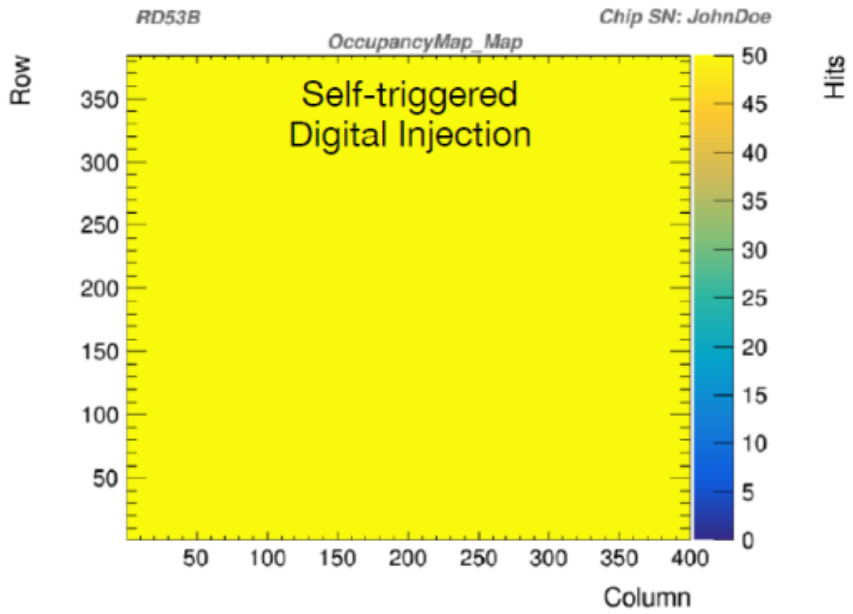
Final production chips to be submitted in first half of 2022

Backup

Self-Triggering

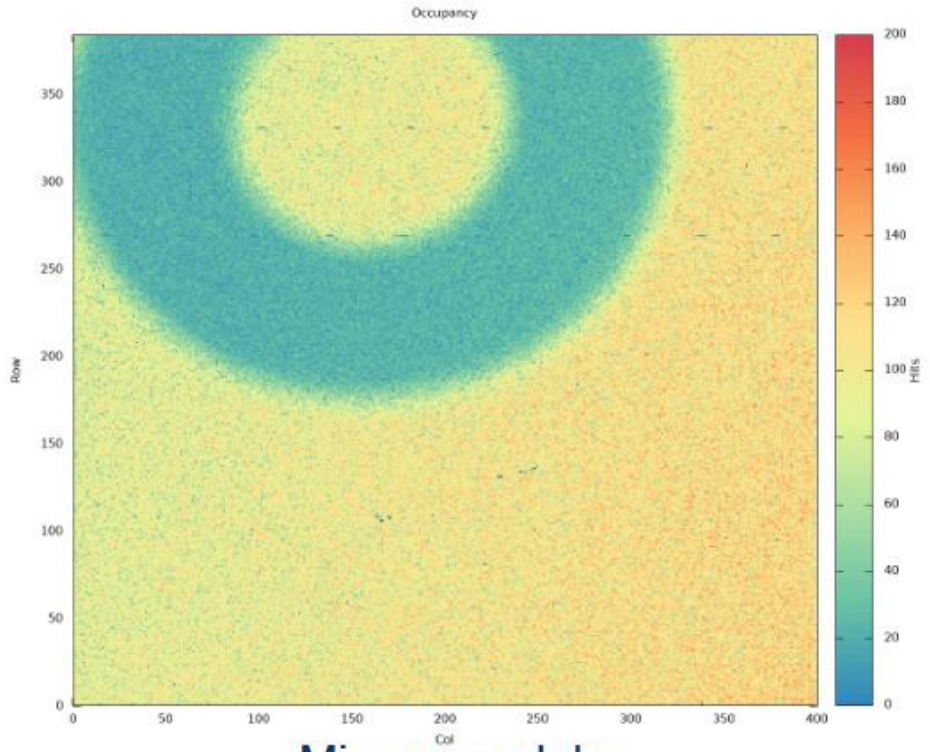


- Auto trigger function based on Hit-OR network
- Four Hit-OR nets serially chaining all pixels in each core column
- At the end of core column, the four are combined to build global Hit-OR with programmable patterns

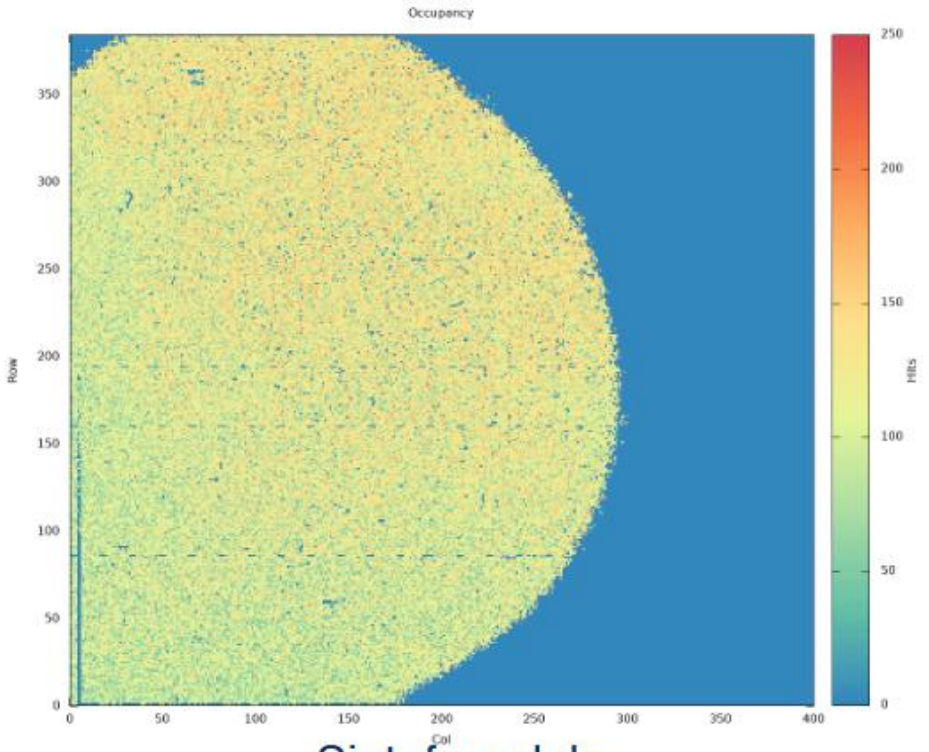


Source scan results

- Source scan tested with self-trigger functionality



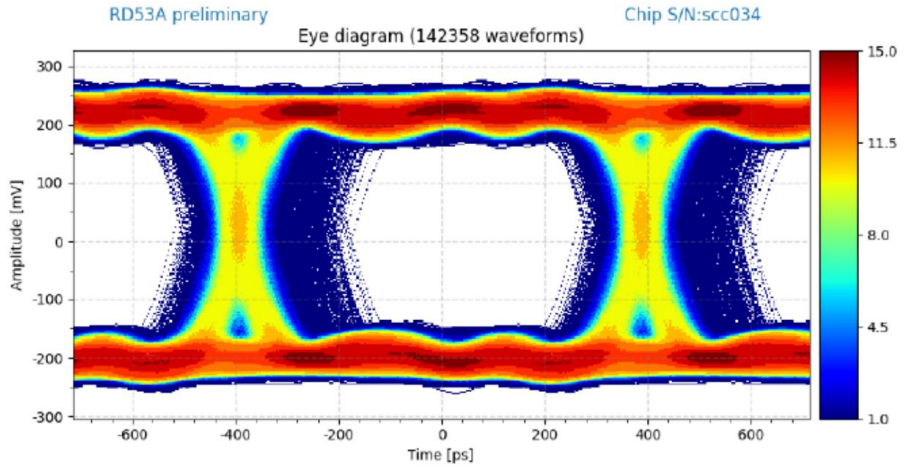
Micron module
(structure created by masking washer)

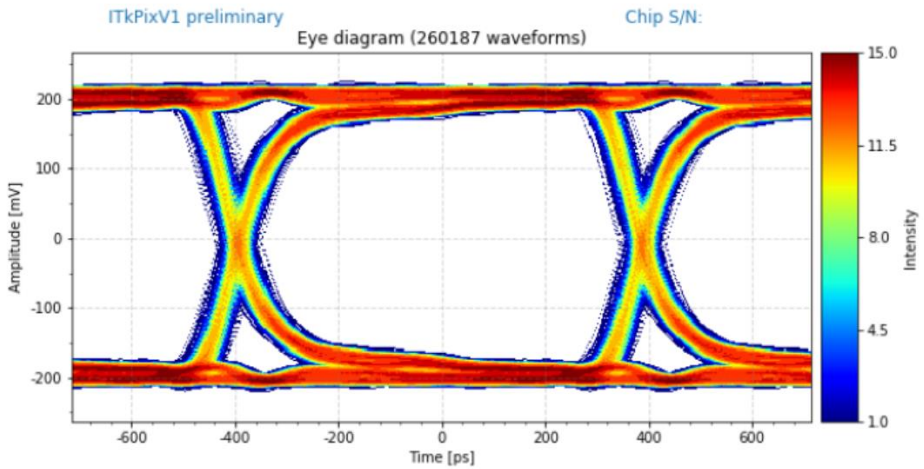


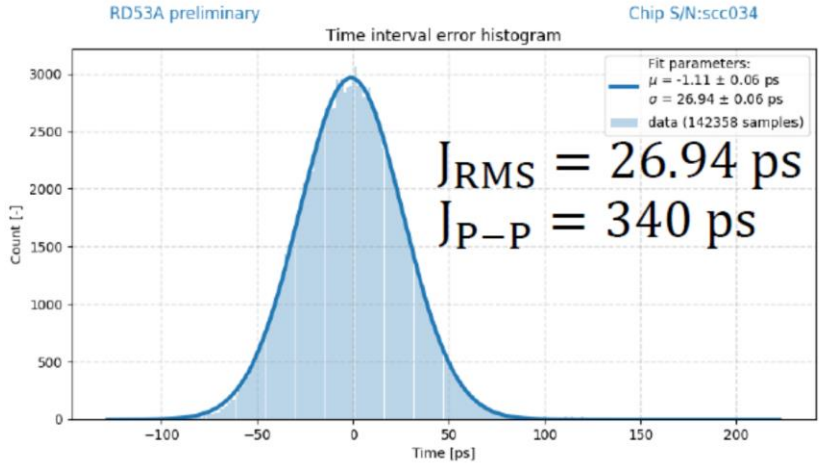
Sintef module
(note disconnected pixels)

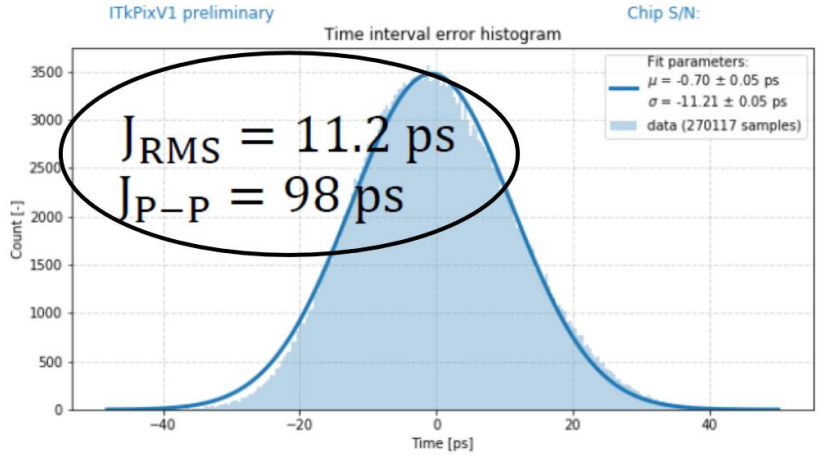
CDR/PLL

- **Great improvement in terms of jitter and start-up reliability compared to RD53A**



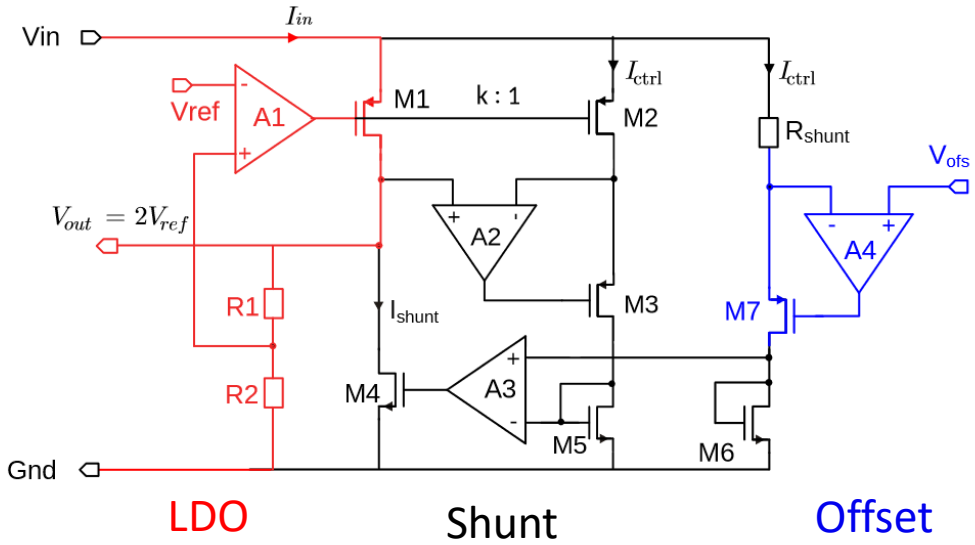




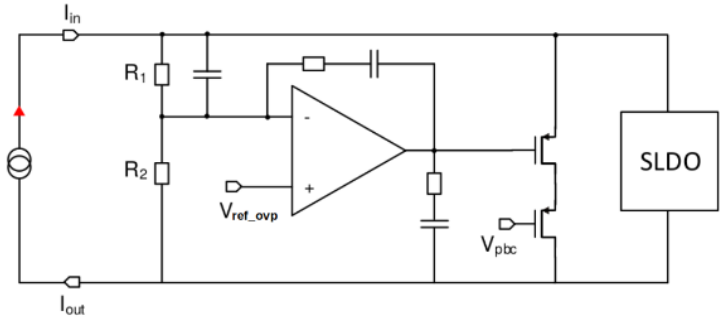


Shunt-LDO circuit

Simplified Shunt-LDO circuit

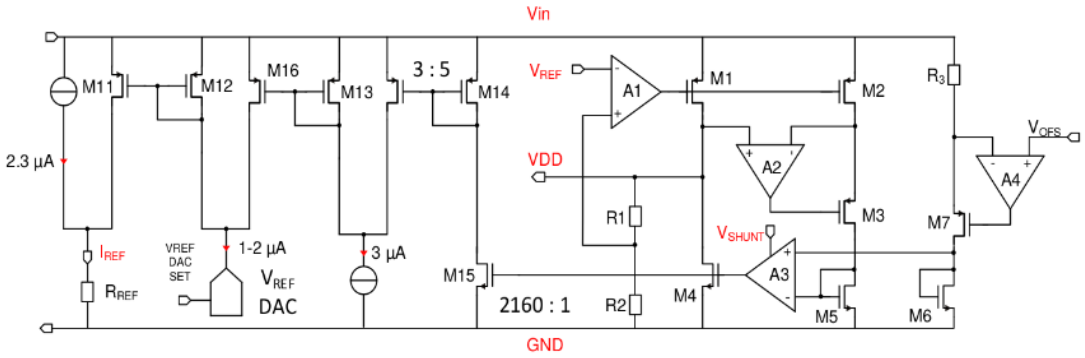


Overvoltage protection (OVP)



- Shunts any surplus current if VIN > 2V

Under shunt protection (USP)



- Reduces Vout of LDO if low shunt current detected