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Test results of RD53B chips for ATLAS and CMS phase-2 pixel upgrades

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Following the RD53A demonstrator, the ItkPix (ATLAS) and CROC (CMS) pixel readout chips are being developed within the RD53 collaboration for the HL-LHC pixel detector upgrades of the two experiments. The two chips are based on a common design, called RD53B, in 65nm CMOS technology and are optimized for very high rate (3GHz/cm2) and radiation levels (>500Mrad). The ATLAS pre-production chip ItkPixV1 was submitted in March 2020 and the CMS pre-production chip CROCv1 is being submitted in May 2021.
This contribution gives a general overview of the chip architecture and discusses the characterization and testing of the pre-production chips.

Summary (500 words)

The RD53 collaboration is a joint effort between ATLAS and CMS to develop pixel readout chips for the HL-LHC pixel detectors of the two experiments. The harsh environment in the innermost layers of the detectors is setting stringent requirements on the pixel chip design. The readout has to be capable to cope with very high hit rates of 3 GHz/cm2 and trigger rates of 1 MHz in combination with a trigger latency of 12.5 us. A very high radiation tolerance of over 500 Mrad and 2x10^16 neq/cm2 is required as well as the support for a serial powering scheme.

A half-size demonstrator chip, called RD53A, was submitted in 2017 and has been tested exhaustively to qualify the different IP blocks and the general architecture for the development of the final pixel chips. It has also been used extensively for sensor characterization as well as for system studies giving viable input to the module designs and system architecture of both experiments.

The next generation RD53 chips, called RD53B, are designed as full sized pre-production chips and incorporate all production requirements defined by the experiments. There are two experiment specific versions of RD53B: the ATLAS version, called ItkPixV1 and the CMS version, called CROCv1. The two chips are two separate instances of the common RD53B design framework. The main difference between them is the pixel matrix size (400x384 for ATLAS and 432x336 for CMS) and the pixel analog front end.

The RD53B generation is as the RD53A designed in 65nm CMOS technology and features 50um x 50um sized pixels. Among the many added features are data-merging between neighbouring chips, data compression to reduce the data rate by a factor of 2 and a self-trigger capability. The PLL/CDR and the Shunt-LDO power regulator circuits have improved greatly allowing for a reliable operation. Protection features against overvoltage and overload have been added together with an optional low power mode. To mitigate Single Event Effects (SEE) a Triple Modular Redundancy (TMR) strategy was adopted including self-correction and a triplicated clock tree with skew for critical parts.

The ATLAS pre-production chip ItkPixV1 was submitted in March 2020 and has since been extensively tested and characterized. The CMS pre-production chip CROCv1 is being submitted in May 2021 and incorporates bug fixes and few additional monitoring and diagnostic features.

A general overview of the chip architecture will be given and the characterization and testing of the pre-production chips will be discussed based on results of the ItkPixV1. Depending on the availability of the chip, also preliminary test results of the CROCv1 will be shown.

Primary author: KOUKOLA, Dominik (CERN)

Presenter: KOUKOLA, Dominik (CERN)

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