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Implementation and testing of Design For Testability methodologies in 65 nm ASICs for HL-LHC.

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The development of the MPA and SSA ASICs is approaching the production phase with a volume of more than 1000 wafers. The importance of yield management in the construction of the Outer Tracker modules requires rigorous testing methods capable to identify all defective parts. This contribution presents customized Design for Testability methods to replace the currently used functional tests that show limited coverage and long testing time. Scan-chain design, memory and Logic Built-In-Self-Test have been adapted for radiation-hard ASICs and introduced on-chip for a novel testing approach. Design flow and implementation choices will be presented together with silicon results.

Summary (500 words)

CMS Outer Tracker Front-End ASICs, namely MPA and SSA, are required to work in a harsh environment for an extended time period (10 years, ~53 Mrad) without any maintenance. The impact of faulty chips is aggravated by their combined assembly into expensive modules and for this reason production testing represents a fundamental step. On the other hand, the increasing complexity and integration in VLSI technology have a significant impact on the cost and difficulty of this phase.

To face the challenge, over the past decades, the industry has developed new approaches and methods to ensure quality and feasibility, replacing functional tests which simply exercise the circuit behaviour according to functional stimuli. Manufacturing defects are grouped into models representing the digital behaviour of physical defects and automatic algorithms have been elaborated to detect faults. Due to the complexity of these procedures, additional circuitry is needed to guarantee controllability and observability of internal nodes: these additional developments, referred as Design For Testability solutions, must be integrated during development.

Different methods have been studied to test different parts of the FE ASICs hardware: Built-In Self-Tests for SRAMs and Latch-based memory blocks, Scan-Chain Design approach and BIST circuitry for the remaining combinational and sequential logic.

SRAM blocks features an integrated BIST which performs a MARCH C- algorithm on a 512x128 cells matrix and detects SRAM faults with 10n operations, n being the memory lines. Stimulating its dual port behaviour at working speed (40 MHz), it allows to identify the SRAM failures in less than 7ms. A checkerboard test was implemented in hardware for Latch memories, allowing to discover in around 50 us stuck-at faults in the sequential elements with a 4n complexity. Control signals and results for both BISTs are fully manageable internally via I2C protocol and radiation tolerance is preserved with Triple Module Redundancy (TMR) strategy, making the additional hardware transparent during the normal operation of the chip.

Core digital logic can be instead successfully tested within the Scan-Chain Design approach, which allows to exploit the powerful ATPG algorithms. The structural modifications foreseen in the commercial flow for scan chain insertion present radiation tolerance issues for sensitive test signals and therefore are not directly applicable in our design. A flow compatible with TMR design and Single Event Effects resistant was developed and scan chains were inserted to test the peripheral processing logic of the chips. Additional Logic BISTs and compressed scan chains were integrated in the MPA to provide the ASIC with the capability of automatically testing its pixel matrix.

Studies have been carried out to reduce power overhead, eventually limited to few percent's and maintained within specification, and to assess the best trade-off between fault coverage, timing closure and routability constraints. Testing phase demonstrated the correct functionality of the structures and extensive SEU tests proved the radiation hardness of the ASICs.

This contribution will present a novel testing approach from design consideration to silicon testing results for a reliable and cost effectiveness testing procedure.

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