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CIC2: a radiation tolerant 65nm data aggregation ASIC for the future CMS tracking detector at LHC

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The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-II CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). This data aggregator, designed in 65nm CMOS technology, will be a key element of the tracker front-end chain. A first prototype, CIC1, was tested successfully in early 2019 and was followed by the development of a final radiation tolerant version of the chip: the CIC2. CIC2 design, implementation, and complete test results, are presented.

Summary (500 words)

The Concentrator Integrated Circuit (CIC) ASIC is a front-end (FE) chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker (OT) upgrade at the High-Luminosity LHC (HL-LHC). This 65nm CMOS radiation tolerant data aggregator is a fundamental element on the future detector FE chain.

The main OT feature will be its inclusion at the first level of the CMS trigger system. 40MHz readout of the detector is therefore necessary. To this end, a very innovative detection element, the pT-module, has been developed. The main principle, two silicon layers separated by a few mm, is relatively standard in current tracking systems. Readout electronics, on the other hand, is entirely original. Indeed, for the first time, the signal of the 2 layers will be put in coincidence directly at the module level, thus allowing a significant reduction of the detector output data rate. This coincidence will be performed by a set of 3 very front-end ASICs types: CBC and SSA/MPA for 2S and PS modules respectively. Each pT-module will contain 16 such ASICs, each of them handling the readout of around 120 detection channels.

The CIC handles the data produced by those chips and performs another data compression stage. It receives different input streams from 8 FE chips, either MPAs or CBCs (there are 2 CICs per module), processes them, and finally sends out a standardized data stream to one lpGBT ASIC which transmits the data of both CICs. In average the CIC reduces the data throughput by an order of magnitude. It has to be compatible with both module flavors (different hybrids, voltages, input streams) and his therefore highly configurable.

In order to validate the CIC model, a first physical version, the CIC1, was developed and implemented, along with a complete standalone testbench. This chip, which incorporates all the functionalities of the final system along with the same footprint, was successfully tested in 2019. These results paved the way for a fast second iteration in 2020: the CIC2.

CIC2 could be considered as a pre-production version. It is radiation tolerant and satisfies all the technical requirements of the final CIC chip in terms of data transfer rates and power budget. CIC2 chips were extensively tested in 2020. In particular, SEU and TID test campaigns were conducted in order to qualify the chip behaviour under radiations. All these tests did not revealed any major issue, thus qualifying the CIC2 as a potential candidate for the final version of the chip. However, few minor modifications will be implemented in order to further improve the chip performance. The final chip, CIC2.1, will be produced along with the CIC2 in 2021.

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