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Experimental characterisation of the RD50-MPW2 High Voltage-CMOS sensor chip

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The CERN-RD50 collaboration aims to develop and study High Voltage-CMOS (HV-CMOS) sensors for use in very high luminosity colliders. Measurements will be presented for the RD50-MPW2 chip, a prototype HV-CMOS pixel detector with an active matrix of 8 x 8 pixels. The active matrix is tested with injection pulses, a radioactive source and a proton beam. This talk will cover the FPGA based DAQ system, the software and firmware developed to take and analyse data. Proton test-beam telescope measurements will be presented as well as the detector gain and noise characterisation using charge injection and radioactive source measurements.

Summary (500 words)

RD50-MPW2 is a prototype pixel detector chip in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry. It contains several circuits and test structures, including an 8 x 8 active matrix with two flavours of high granularity pixels (60 µm x 60 µm) that use different methods to reset the sensing diode. These methods are named continuous-reset and switched-reset. Pixels with continuous-reset use a continuous current to reset the Charge Sensitive Amplifier (CSA) after a particle hit, resulting in a dead time that is proportional to the number of electrons collected by the sensor. With this pixel flavour, it is possible to process a particle hit that generates 10k electrons within 90 ns only. Pixels with switched-reset use the output of the discriminator to switch on and off a larger reset current. The switched current resets the CSA in 15 ns and shortens the dead time to 45 ns, independently of the number of collected electrons. As the larger reset current is active for a very short time only, the power consumption is kept low.

The DAQ system to measure RD50-MPW2 is composed of a Xilinx ZC706 FPGA board, a Caribou data acquisition board and the dedicated chip board. The Zynq-7000 XC7Z045 SoC on the ZC706 is programmed with a custom version of the Peary Caribou firmware, a processor side coded in C and logic side coded in VHDL. A custom C++ GUI has been developed to communicate with the firmware to configure and readout the chip. This allows a simple interface to be used to select a pixel for injection, perform a hit map scan, generate a response curve to calculate the gain, generate s-curve data to calculate the noise, modify the internal DACs of RD50-MPW2, adjust the internal DC baseline level, set thresholds and control the analogue multiplexer. An overview of the entire DAQ chains hardware and firmware/software will be presented.

Results of a recent test-beam at the Northumbria Rutherford Cancer Centre in the UK will be presented. Measurements were taken using an IBA Proteus One –S2C2 Synchrocyclotron proton beam, using a range of energies from 70.2 to 200 MeV.

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