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FastIC: A Fast Integrated Circuit for the Readout of High Performance Detectors

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This work presents the 8-channel FastIC ASIC developed in CMOS 65nm technology suitable for the readout of positive and negative polarity sensors in High Energy Physics experiments, Cherenkov detectors and Time-of-Flight systems. The front-end can be configured to perform analog summation of up to 4 single-ended channels before discrimination in view of exploiting area segmentation. The outputs encode the Time-Of-Arrival information and linear Energy measurement in the 5uA –20mA input range, with a power consumption of 12mW/ch with preset settings. Measurements of Single Photon Time Resolution with a red-light laser source and a Hamamatsu SiPM S13360-3050CS are ~140ps FWHM.

Summary (500 words)

This work presents the 8-channel FastIC (Fast Integrated Circuit) developed in 65 nm technology suitable for High Energy Physics experiments, Cherenkov detectors and, other Time-of-Flight systems, based on the classic multi-branch architecture (i.e., time, energy, and trigger information) with similarities to the HRFlexToT ASIC. The front-end stage processes the signals in current mode with an input impedance below 20 Ω and can be programmed to cope with positive and negative polarity sensors, such as photo-multiplier tubes, microchannel plates, and Silicon Photomultipliers. The 8 channels can be configured to work as 4 differential channels. Alternatively, 4 single-ended sensor signals can be summed, and the discrimination is performed on the resulting pulse. This active summation functionality is integrated to explore the impact of segmenting a large sensor area to improve time jitter.

Each FastIC channel provides the information of Time-Of-Arrival and a linear energy measurement of the detected photons. Time measurement is generated through a leading-edge comparator whose output provides a non-Linear ToT response encoding the arrival time of the events in the rising edge of a pulse. The signal processing path for energy measurement generates a binary pulse whose width is proportional to the collected charge (using the same processing scheme as the HRFlexToT ASIC) with a linearity error below 3% over the entire dynamic range from 5 uA to 20 mA. Different trigger methods with configurable thresholds are available to indicate when a valid event is captured. The output driver can be programmed in CMOS single-ended or differential Scalable Low-Voltage Signaling. Alternatively, internal analog signals can be readout by means of a high-speed analog driver per channel.

The power consumption of FastIC is 12 mW/ch in single-ended mode (full channel functionality) or 6 mW/ch when only the time branch is used (non-linear ToT operation). The maximum hit rate per channel is 2 MHz using the linear ToT and about 50 MHz when employing the non-linear ToT. Simulation results using a Hamamatsu SiPM S13360-3050CS model at 4.5 V over-voltage and parasitic interconnections, resulted in a predicted electronics jitter of 30.9 ps rms Single-Photon Time Resolution (SPTR) in single-ended positive polarity configuration. This predicted SPTR decreased to 16.8 ps when segmenting this 3x3 mm2 sensor into four 1.5x1.5 mm2 SiPMs.

SPTR laboratory measurements using a red-light laser source and a Hamamatsu SiPM S13360-3050CS are ~140 ps Full Width at Half Maximum (FWHM) at 10.6 V over-voltage. The HRFlexToT ASIC tested in the same conditions yielded an SPTR of 161.5 ps FWHM at 10.5 V over-voltage and thus showing that FastIC provides a lower electronic jitter. Note that the measured SPTR is the convolution of the SPTR of the sensor, the laser FWHM and the electronic jitter. A Hamamatsu PMT R5900 producing pulses with ~5 ns FWHM, and a theoretical transient time spread of 330 ps FWHM, was tested using the same red-light laser resulting in an SPTR of 340 ps FWHM after time walk correction showing that the FastIC does not degrade the time response for this detector, nor the pulse shape.

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