Verification methodology of a multi-mode radiation-hard high-speed transceiver ASIC

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The second version of Low Power Giga Bit Transceiver (lpGBTv1) addresses the functional and radiation-related issues discovered during the testing of lpGBTv0 prototype. Considerable changes to the chip configuration architecture and flow were required. The Universal Verification Methodology (UVM) based verification environment was extensively refactored to address the functional verification challenges posed by the architectural changes in the chip. Additionally, a novel SEE verification strategy was proposed and implemented. In this paper we present the revamped UVM verification framework of lpGBTv1 and discuss the verification process, tools, techniques and metrics used to sign-off the design before submission.

Summary (500 words)

In modern ASIC development, verification accounts for about 60% of the overall project time. Effort spent in improving the quality of the radiation tolerant ASIC designs before manufacturing greatly minimizes the risk of running into unexpected functional errors and Single Event Effects (SEEs) in the fabricated chip which in-turn saves time-consuming silicon debug effort and costs of respin. The primary focus of any verification activity is to ensure the highest possible quality of the design under test by identifying functional errors and SEE vulnerabilities in the design before tape-out. To efficiently address the challenges of verification, the underlying verification framework must be capable of supporting modular implementation of constrained random verification content along with the required checkers and coverage.

The lpGBT is a versatile radiation-hard ASIC designed to provide high speed multi-purpose bidirectional links for high energy physics experiments. The versatility of the chip is managed through the vast configuration space exposed to the user through multiple configuration interfaces. This configurability coupled with supported configuration flows increase the state space of the chip resulting in verification complexity.

The new lpGBTv1 testbench architecture, built using UVM, is modular and extensible, which enabled easy development of highly randomized functional tests closely representing the use-cases of the chip. Various advanced UVM techniques such as agent/sequence layering and register abstractions were used while developing the UVM environment. The refactored UVM environment also enabled thorough SEE verification with same level of randomization in the stimuli as used for functional verification. High level of randomization implied that each test had to be rerun multiple times with different random seeds to completely cover the state-space of the stimulus. Oracle Grid Engine (OGE) based batch system was extensively used to parallelize multiple test executions. Metrics such as code coverage, functional coverage, fault coverage, regression pass-rate and verification plan score were used and tracked over the project life-cycle to obtain quantitative view of the progress and quality of verification. The contribution will present processes, technologies, tools, techniques and metrics used during the verification and sign-off of lpGBTv1 along with a brief summary of the bugs discovered in the process. Besides providing examples worth replicating in verification of complex SEE robust ASICs, we will also discuss approaches that did not work.

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