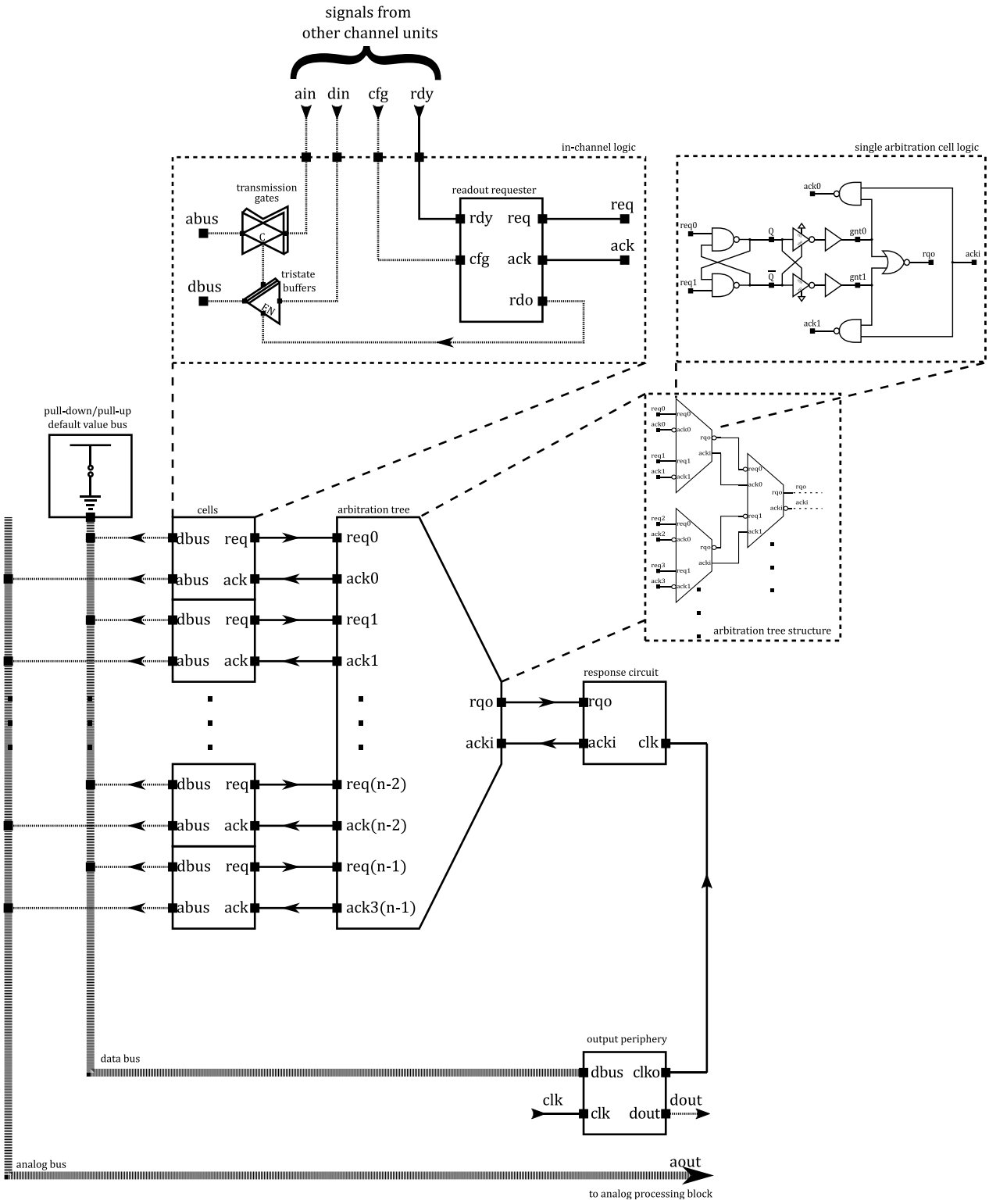

Figure 1 The presented readout system

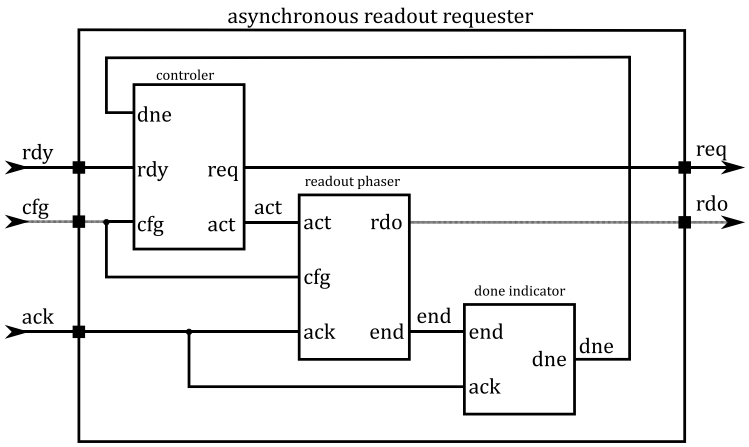

Figure 2 Block diagram of the in-channel logic

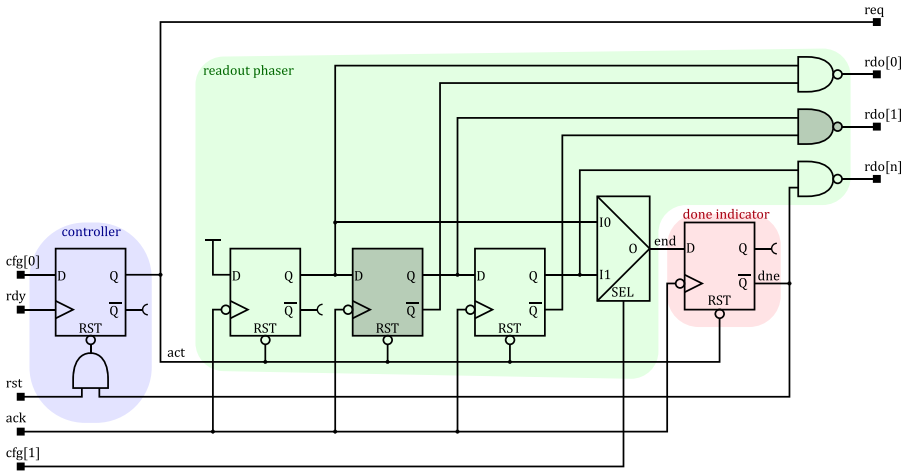

Figure 3 Implementation of logic in the channel

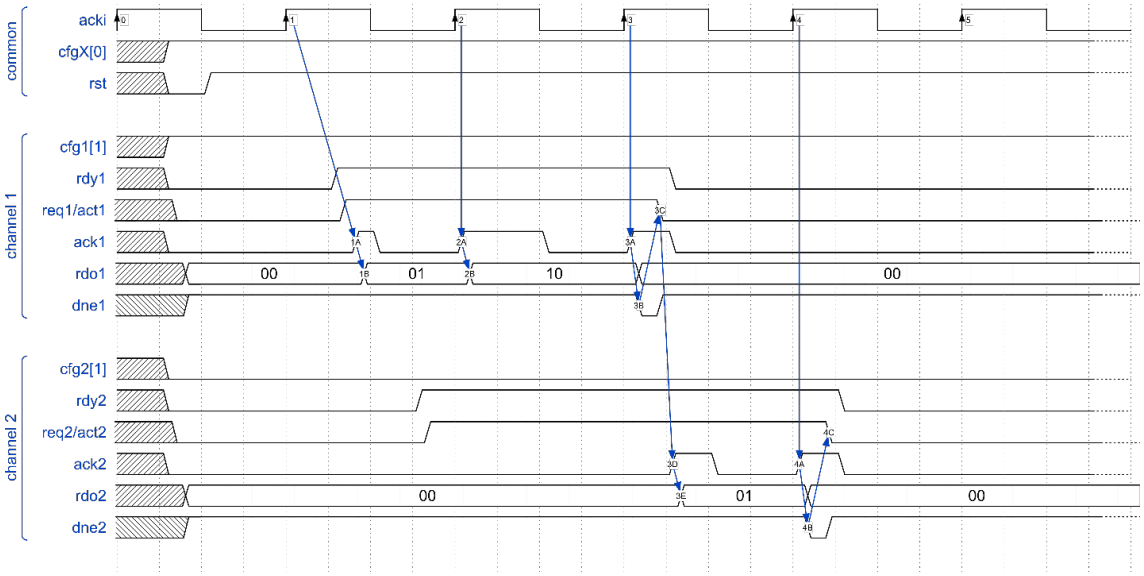

Figure 4 Waveforms showing successive readouts from two different channels