Contribution ID: **100** Type: **Poster**

Certification of the amplifier-shaper-discriminator ASICs produced for the ATLAS MDT chambers at the HL-LHC

Tuesday, 21 September 2021 17:35 (3 minutes)

The front-end electronics of the ATLAS muon drift-tube chambers will be upgraded in the experiment's phase-II upgrade to comply with the new trigger and read-out scheme at the HL-LHC. A new amplifier shaper discriminator chip was developed in 130 nm Global Foundries technology for this upgrade. A preproduction of 7500 chips was launched in 2019 and tested in 2020. The functionality of the chips, the test set-up and test procedure and results showing a yield of 92% are presented. The certification of the preproduction was followed by the production of 80,000 chips in fall 2020 showing 92% yield.

Summary (500 words)

The upgrade of the front-end electronics of the ATLAS muon drift tube (MDT) chambers is part of the phase-II upgrade of the ATLAS detector for HL-LHC. The present amplifier shaper discriminator (ASD) chip for the MDT chambers was designed in Agilent 500˜nm technology which has become obsolete. For the upgrade a new ASD chip was designed in Global Foundries 130˜nm CMOS technology. The design of the new chip follows the design of the present chip, but incorporates a fix of a specific design error of the present chip in the output logic. he chip has a differential charge sensitive preamplifier, bipolar shaping with ion tail cancellation and a Wilkinson ASD for time-walk corrections to the discriminated signals. Each channel is connected to a discriminator providing LVDS output signals. A discriminator threshold common to all the channels can be programmed and generated inside the chip. A preproduction of 7500 chips was launched in 2019 and tested in 2020. The tests were carried out manually using a test board provide by the ATLAS muon group of the Ludwig-Maximilians University of Munich.

The chip tests proceed along the following steps:
* Reject chips which cannot be powered up or cannot be put into operation;
* Reject chips which draw abnormal currents;
* Reject chips with channels that have wrong output LVDS levels;
* Reject chips with dead channels;
* Reject chips with two large thresholds spreads;
* Reject chips with abnormal ADC counts for an input charge of -20˜fC.

For the last three tests in the list above pulses with predefined charges are injected to the eight channels of the chip one after the other.

More than 91% of the tested chips pass all criteria. 0.07% of the chips cannot be put into operation. 0.22% chips have bad LVDS output levels. 0.07% of the chips have too low total currents. 1.87% of the chips have dead channels. 1.87% show too large threshold spreads and 4.02% give bad ADC values.

The same very high yield as for the preproduction was found for a sample of 1000 production chips. The remaining 79,000 ASD chips will be tested by a company in a automated procedure.

Primary authors: ABOVYAN, Sergey (Max-Planck-Institut fur Physik (DE)); DANIELYAN, Varuzhan (Max--Planck-Institut fur Physik (DE)); GRASSER, Andreas (Max-Planck-Institut für Physik); KORTNER, Oliver (Max--Planck-Institut fur Physik (DE)); KROHA, Hubert (Max-Planck-Institut fur Physik (DE)); RICHTER, Robert (Max--Planck-Institut fur Physik (DE)); SIMEONOV, Simeon (Max-Planck-Institut für Physik)

Presenter: KORTNER, Oliver (Max-Planck-Institut fur Physik (DE))

Session Classification: Posters ASIC

Track Classification: ASIC