Contribution ID: **136** Type: **Poster**

QTIA, a 2.5 or 10 Gbps 4-Channel Array Optical Receiver ASIC in a 65 nm CMOS Technology

Tuesday 21 September 2021 17:47 (3 minutes)

The Quad Transimpedance and limiting Amplifier (QTIA) is a 4-channel array optical receiver ASIC, developed using a 65 nm CMOS process. It is configurable between the bit rate of 2.56 Gbps and 10 Gbps. QTIA offers careful matching to both GaAs and InGaAs photodiodes. At this R&D stage, each channel has a different biasing scheme to the photodiode to look for the optimal coupling. A charge pump is implemented in one channel to provide a higher reverse bias voltage, mitigating radiation effects on the photodiodes. QTIA circuit functions pass preliminary but successful tests.

Summary (500 words)

High-speed optical data communication is widely used for on-detector readout electronics in high-energy physics (HEP) experiments. In these applications, the transmitter and receiver of the optical link need to be radiation tolerant to the detector operation environment. In applications near the interaction points, radiation-induced degradation of the photodiode is the most challenging issue nowadays. This degradation causes many parameters to change and is different between GaAs and InGaAs photodiodes. There are many studies on photodiodes in radiation, mostly by CERN. For InGaAs photodiodes, radiation results in an increase of the dark current (up to 1 mA) and a rise in the junction capacitance (up to several pF). GaAs photodiodes suffer from a significant loss in responsivity due to radiation. Based on these findings, we designed and prototyped a quad transimpedance and limiting amplifier (QTIA) ASIC to research mitigation options.

QTIA is selectable to operate at 2.56 or 10 Gbps data rate. It adopts a fully differential architecture. Photodiodes are AC coupled to the TIA using on-chip capacitors. The integrated bias circuits provide proper biasing to the photodiode. The bias circuits in all channels are different. The Up-bias circuit is realized by PMOS with source degeneration in channel 2. The Down-bias circuit is composed of NMOS with source degeneration in channel 3. Both Up-and Down-bias circuits are used in channel 1 and channel 4. The bias voltage is tied to a 2.5 V power supply in channel 2 and channel 3. A charge pump (CP) is implemented in channel 1 to raise the bias voltage to photodiode to a level determined by its leakage current. In channel 4, the bias voltage is provided through an external power pad.

A fully differential cascade TIA with programmable feedback resistance is designed to achieve low noise and high bandwidth. The limiting amplifier has two stages with shared inductors and two active feedback stages to simultaneously achieve high gain and bandwidth. The output driver has adjustable output amplitude and drives a 100-ohm differential output load.

QTIA is 2 mm × 2 mm. It has been fabricated and assembled in the ultra-small and lightweight optical module, QTRx, together with a 4-channel array laser driver, QLDD. Preliminary tests at 2.56 Gbps indicate that channel 4 with the bias circuits on both sides and the external bias voltage display the best performances, with a sensitivity of −17 dBm for a BER of 1E-12. For -6 dBm input, the total jitter is 46.7 ps with a random jitter of 2.7 ps and a deterministic jitter of 12.5 ps. The preliminary and conservative result of channel 1 sensitivity is -12 dBm with the charge pump output over 6.5 V. The nominal differential output amplitude remains 400 mVpp even for small input signals. The power consumption is below 72 mW per channel (without CP). A full set of optical and irradiation test results with different photodiodes will be carried out. We will present the results we have by the time of the conference.

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Session Classification: Posters ASIC

Track Classification: ASIC