A 20 Gbps PAM4 Data Transmitting ASIC for Particle Physics Experiments

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Introduction

Physics and detector developments call for high data bandwidth. The lpGBT [1] ASIC developed for the high-luminosity LHC (HL-LHC) upgrades achieves a non-return-to-zero (NRZ) data rate of 10.24 Gbps. We propose to double the transmission data rate in the same fiber by re-using design blocks of lpGBT and adding the Pulse Amplitude Modulation 4-level (PAM4) combiner . Figure 1 is the proposed overall optical link architecture. On the on-detector side, we prototype an Application Specific Integrated Circuit (ASIC) named GBS20 that operates up to 20.48 Gbps. GBS20 can directly drive a VCSEL, making it possible to build a compact optical transmitter module called GBT20. On the off-detector side, another module GBR20, which includes a PD, a TIA, and a PAM4 decoder, is under design. The output of GBR20 is a 20 Gbps NRZ signal, providing a variety of choices for FPGAs .

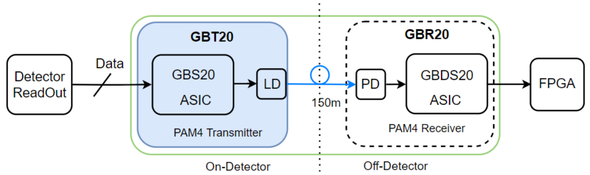


Figure 1.Overall optical link architecture in particle-physics experiments

Chip design

GBS20 is manufactured in a commercial 65 nm CMOS technology. The ASIC size is 2 mm x 2 mm. GBS20 operates at either 10.24 Gbps or 20.48Gbps data rate. The Overall structure of GBS20 is shown in figure 2. Sixteen input user-data channels, each at 1.28 Gbps, are divided into Least Significant Bits (LSBs) and Most Significant Bits (MSBs) and sampled in two aligners. The input data are scrambled with an internal 2^7-1 Pseudo-Random Binary Sequence (PRBS) test pattern and fed to two serializers. The serializers are based on the design of lpGBT. A low-jitter Phase-Locked Loop (LJPLL) provides clocks for all the digital parts. The outputs of two serializers are combined into a PAM4 signal through a five-stage limiting amplifier.

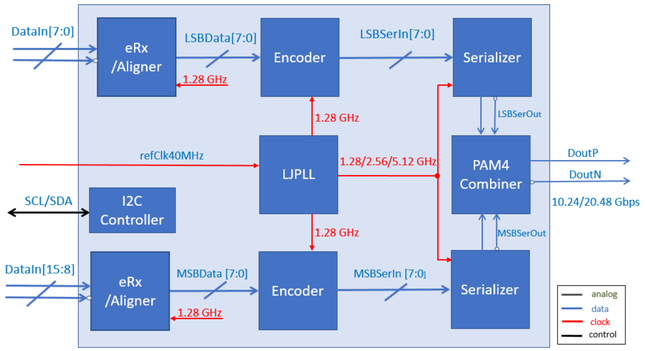


Figure 2. Overall structure of GBS20

The current ratio of the LSB channel and the MSB channel is normally 1:2. In our design, the current of the LSB or MSB channel can be independently adjusted to decrease the possible nonlinearity in the system. The LSB or MSB driver can be turned off, providing a way to check each serializer's NRZ output. The bandwidth of the PAM4 output driver can be adjusted by using a shared inductor and a CTLE structure. A programmable capacitive load is added to damp overshooting, which is more of a problem in the PAM4 signal case than in the NRZ one.

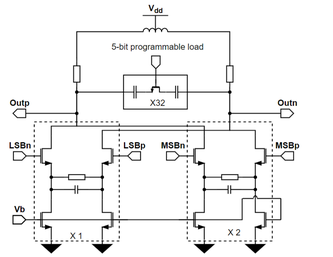


Figure 3.Schmatic of the PAM4 combiner

Test result

To fully characterize GBS20, a test board was assembled with a commercial 25 Gbps 850 nm TOSA. Figure 4 shows the photograph of the test setup. A Cyclone 10GX EVB generates 16 channels of user data. An Si5338 EVB provides clocks to an oscilloscope and the boards. Using low-dropout regulators on the test board, only a 4 V voltage supply is needed.

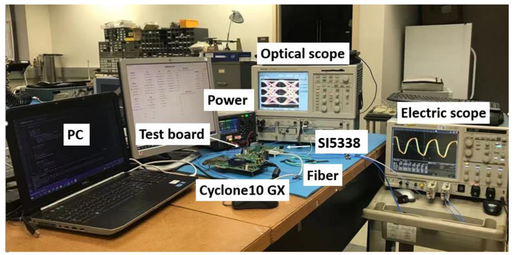


Figure 4. photograph of the test setup.

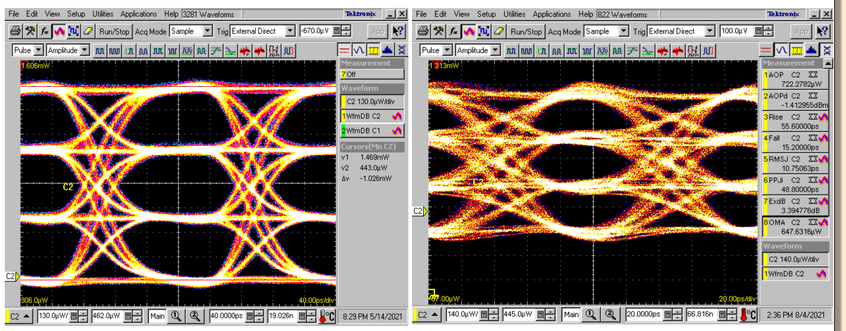


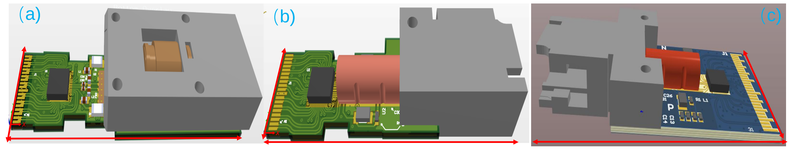
Figure 5.The test result of 10 Gbps, (a) and the test result of 20 Gbps(b)

The test results show the maximal OMA is about 1 mW at 20 Gbps. The power dissipation is less than 250 mW when the PAM4 driver works at a 2.5 V power supply and the VCSEL operates at the maximal bias and modulation currents. In some low-power dissipation applications, the power dissipation can be reduced to 164 mW by decreasing the supply voltage of the PAM4 driver.

Programmable capacitive load and independently bias currents were proved to be useful. Based on the KC705 board, bit error rate was tested. No error occurred within 3 hours. Limited by the test equipment, the TDECQ has not been measured and the test will be arranged soon.

GBT20 module

The figures below show the 3D models of the GBT20 modules. The modules will be assembled with a TOSA or a VSCEL diode under an LC lens. Compared with the TOSA, the LC lens is more compact. GBT20 modules will be submitted for fabrication by the end of this month.



Size:40 x13x5.75 (unit :mm) Size:40 x12x6.5 (unit :mm) Size:40 x19x6.5 (unit :mm)

Figure 6. GBT20 3D models: a firefly connector plus a TOSA (a). a firefly connector plus a LC lens (b). a OSFP connector plus a LC lens .

GBR20 design

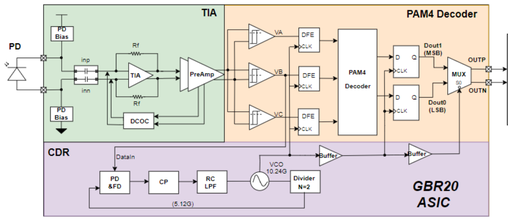


Figure 7.Block diagram of GBR20.

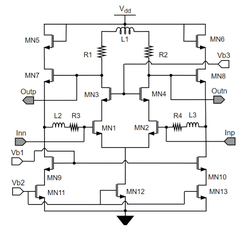


Figure 8. Schematic of the TIA.

The GBR20 block diagram is shown in figure 7. GBR20 includes a low noise TIA, a PAM4 decoder, and a clock data recovery (CDR). The goal of GBR20 is to translate the 20 Gbps PAM4 optical signal to the 20 Gbps NRZ electric signal for an FPGA. The schematic of a fully differential cascade TIA is showed in figure 8. A peaking inductor is used in the feedback path. After the multistage linear amplifiers, the voltage is higher enough for a PAM4 decoder. The design of GBR20 is still ongoing.

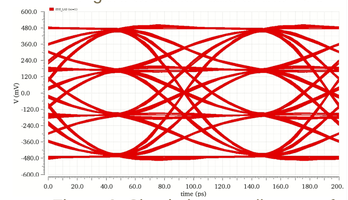


Figure 9. Simulation eye diagram of the Linearity amplifier output.

Conclusion and outlook

We present the design and test results of GBS20. GBS20 successfully operates at 20.48 or 10.24 Gbps. GBT20 transmitter modules and GBR20 are under development. Irradiation tests will be performed in the future.

Reference: [1] Paulo Moreira et al, The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, TWEPP 2019 September 2-6