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The Front End and Trigger Unit for an Analogue Transient Recorder ASIC

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A front end and trigger circuit was developed at GSI which is foreseen to be used in a transient recording read out ASIC. It consists of an input buffer with configurable low pass characteristics and a trigger which could be operated as leading edge discriminator as well as switched capacitor trigger which is sensitive to the first derivative of the input signal. The front end was produced on a test ASIC and characterisation results will be presented.

Summary (500 words)

Currently at GSI a set of read out ASICs is under development which is based on an analogue transient recorder backend. To interface this transient recorder with external front ends an input buffer with a hit detection circuit was developed.

The input buffer is a differential buffer with a high input impedance and an amplification of 1. To suppress high frequency noise and to avoid aliasing effects a configurable low pass filter was realized by integrating switchable feedback capacitors.

The hit detection can be operated in two modes. The first operation mode is using a comparator as a simple leading edge discriminator. The threshold voltage is generated by an internal 10 bit digital to analogue converter. The second operation mode is called switched capacitor mode. Here two operation phases controlled by the sampling clock alternate. In phase one the summ of the momentary input voltage and the threshold voltage is stored in a switched capacitor stage. During phase two the input voltage is compared with the output of the SC stage and the comparator decision is taken at the end of clock phase 2.

This way the trigger is sensitive to the first derivative of the input signal and so the sensitivity of the trigger circuit for low frequency interferences e.g. 50 Hz hum is strongly suppressed.

The front end and the hit detection circuit have been produced on a separate test ASIC in a 180 nm CMOS technology. All main characteristics of the front end, the leading edge discriminator and the switched capacitor trigger have been determined and will be presented. For the presentation of the over all transient recorder and digitising ASIC another abstract (#143) was submitted.

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