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A Family of Transient Recorder ASICs for Detector Readout

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A set of highly integrated read out ASICs with a common digitising and data aquisition back end but different front ends is currently under development at the GSI electronics department. The concept consists in using an analogue transient recorder stage for an efficient application of the area and power consuming analogue to digital converter. A focus of these ASICs is the read out of detectors with a large dynamic range. Possible applications could be the electromagnetic calorimeter of the PANDA detector or the GEM TPC of the Super-FRS at FAIR.

Summary (500 words)

Two read out ASICs are under development at GSI with different front ends but a common digitizing and data acquisition back end. This backend is based on an analogue transient recorder which is able to store transients of 16, 32 or 64 samples in an analogue memory. After a pulse is detected the transient is fixed and digitized with an on chip 12 bit pipeline ADC. On chip digital processing is able to correct cell to cell variations of the analogue memory and to extract amplitude and time from the digitised transients.

Two different front ends have been developed. A simple input buffer which can be used to receive signals from external front ends e.g. charge sensitive preamplifiers. The other option is a charge sensitive amplifier (CSA) with an adaptive feedback to obtain a very large dynamic range of five orders of magnitude. This CSA design abstain from a resistive feedback for continuous reset but uses a switched reset which is synchronised to the transient recorder.

The ASICs are designed in a 180 nm CMOS technology and integrate the read out electronics for 16 channels. Each four channels share a pipeline ADC. The maximum sampling rate of the transient recorder is 100 MS/s while the ADCs convert the transients with 33 MS/s. Both front ends have been characterised on separate test chips. For the presentation of the results of these characterisations two dedicated abstracts have been submitted. The analogue memory and the ADC were characterised in previous test ASICs as well and the results will be presented in this contribution. The design of both 16 channel prototypes is finished and taped out to the foundry.

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