Low Noise Amplifier With Adaptive Gain Setting (AWAGS) ASIC

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Introduction

The GSI ASIC design group developed a new **A**mplifier **W**ith **A**daptive **G**ain **S**etting - the AWAGS chip. In particular the designed input stage allows to use the ASIC in a wide application field for readout different detector types. The presented readout is also used as input stage for the transient recorder ASIC [1] (Poster 143).

Architecture

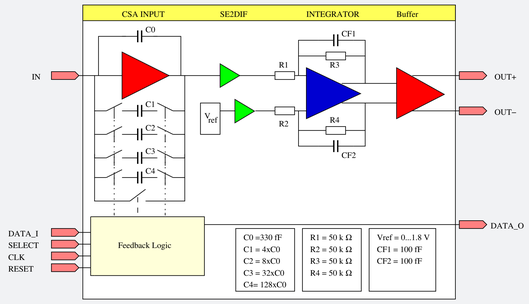

Fig. 1: Architecture of the the AWAGS ASIC

The architecture of the AWAGS chip is shown in figure 1. For the input stage a charge sensitive amplifier is developed connected with switches to the feedback capacitances. Due to missing resistive feedback an active reset is implemented to adjust the operating point of the amplifier after charge detection. The bidirectional communication is realized with an on chip interface to read/write feedback capacitances and DAC values. The input stage is followed by a fully differential stage and output buffers. A picture of the ASIC is shown in figure 2.

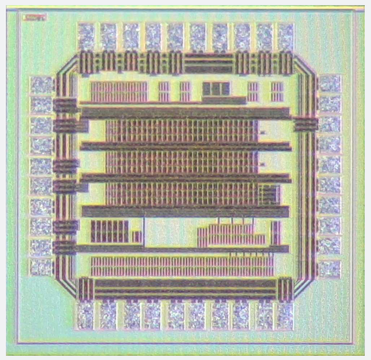

Fig. 2: Picture of the AWAGS ASIC produced in UMC 180 nm CMOS process

Measured Results

The input stage of the AWAGS ASIC is based on a folded cascode architecture[2] with a n - MOS input transistor. In difference to common charge sensitive amplifier architectures the new input stage features five separate feedback capacitors with values from 0.35 pF to 55 pF. Using the automatic mode depending on the incoming charge the capacitances are dynamically added to the feedback to avoid saturation of the amplifier while keeping the sensitivity as high as possible.

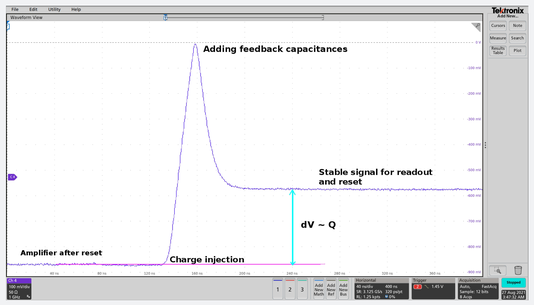

Fig. 3: Transient measured with the adaptive gain setting mode of the AWAGS chip

- Transient recorded in automatic gain setting mode of the amplifier
- To avoid the amplifier from saturation next feedback capacitance is added
- After max. 100 ns the output signal is stable for readout and subsequent reset
- The charge value is proportional to the output voltage and the present gain

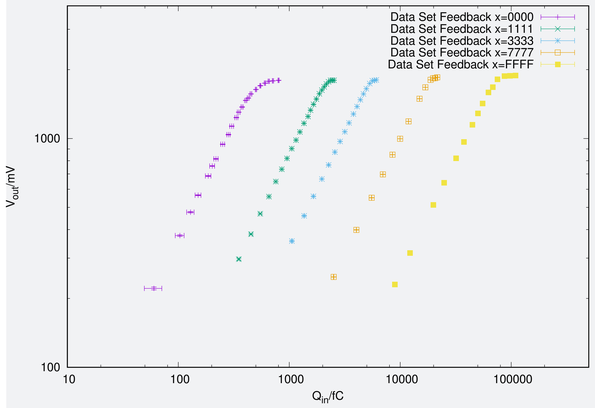

Fig. 4: Dynamic for manual gain setting

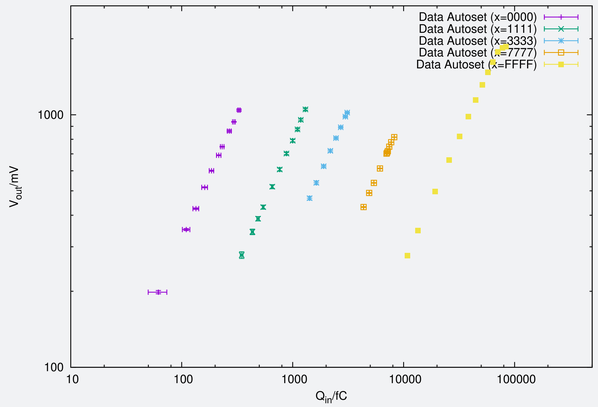

Fig. 5: Dynamic for automatic gain setting

Figure 4. presents the dynamic range measurements for different feedback capacitances in manual gain setting mode. It shows the saturation of the preamplifier at about 1.5 V. In figure 5. the dynamic range measurements for the automatic gain setting mode is shown. In comparison to the manual mode the gain decreases before the amplifier saturates.
The lower limit of the dynamic range is given by the noise measurements. The upper limit is determined according to the one - dB - compression point definition for power amplifiers. Table 1. shows the summary of the measured results.

	Manual Mode	Automatic Mode	Unit
Gain M(C_0)	$3.70281 \pm 1.08 \times 10^{-2}$	$3.195 \pm 8.21 \times 10^{-3}$	mV/fC
Gain M(C_{ALL})	$0.02569 \pm 6.01 \times 10^{-5}$	$0.0256 \pm 3.21 \times 10^{-5}$	mV/fC
Noise:	$0.38521 \pm 3.25 \times 10^{-2}$	$0.4163 \pm 2.16 \times 10^{-2}$	fC
Max. measured charge:	79 671	81 307	fC
Dynamic range:	1 493 (per config)	204 757	1
Risetime (M(C_{ALL})):	8.145 ± 0.261	7.633 ± 0.142	ns

Tab. 1: Summary of the measured results

Conclusion

To compare the performance of this adaptive gain setting amplifier (AWAGS) ASIC with other developments following O'Conner[3] the power over speed and dynamic range quotient is used as a figure of merit (FOM). With $\tau_s = 100\,\text{ns}$ and $P = 12\,\text{mW}$ one gets

$$FOM = \frac{P \times \tau_s}{Q_{max}/\sigma_Q} = 5.86\,fJ.$$

As shown in figure 6 this is a factor of ≈ 250 better than for conventional designs.

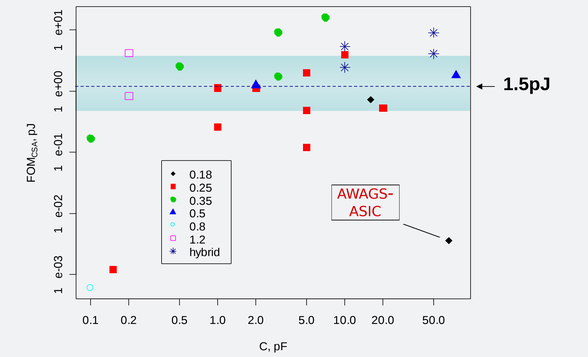

Fig. 6: FOM comparison of amplifiers including the present AWAGS - chip

This could be obtained by combining a good noise performance at minimum feedback capacitance with the large dynamic range of the adaptive gain setting.

Summary

The presented prototype produced in an MPW run end of 2020 show excellent results, especially regarding the noise and the dynamic range. The adaptive gain setting technique yields in a dynamic range of over 200 000 in a linear way.

References

[1] H.Flemming, A Family of Transient Recorder ASICs for Detector Readout, 2021, TWEPP Poster ID 143
[2] Chang, Z.Y., Low Noise Wide-Band Amplifiers in bipolar and CMOS technologies, Kluwer Academic Publishers 1991.
[3] Paul O'Conner, Noise and Power Tradeoffs in CMOS Front Ends, 2006, Presented at VIth International Meeting on Front End Electronics FEE2006, Italy