2.56 Gbps CML transceiver for the data concentrator ASIC

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2.56 Gbps CMOS CML-transceiver is presented. The key feature of the design is capability of working with a specific inductive load at both power consumption and radiation tolerance constraints. The transceiver was designed as an interface part of the HUBv1 data concentrator ASIC [1], intended for the front-end electronics of the time-projection chamber of the MPD experiment at NICA nuclotron (Dubna) [2].

Interface surrounding

Problem: CPGA120 package + small prototype size require high-speed operation over inductive wiring and coaxial cable load.

Wires inductance estimate: *3-5 nH*
Mutual wires inductance: *0.5 nH*
uCoaxial cable (AWG36) length: *up to 1 m*
Unbalanced parasitic loads on FEC and DAQ boards: *up to 3 pF*
Radiation tolerance as for [2].

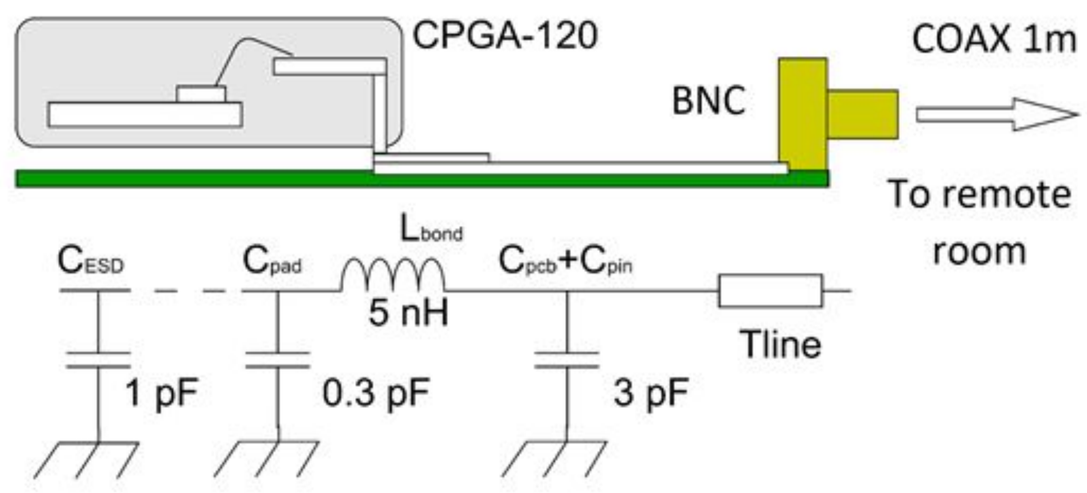

Figure 1. CML-interface equivalent circuit

Transceiver structure

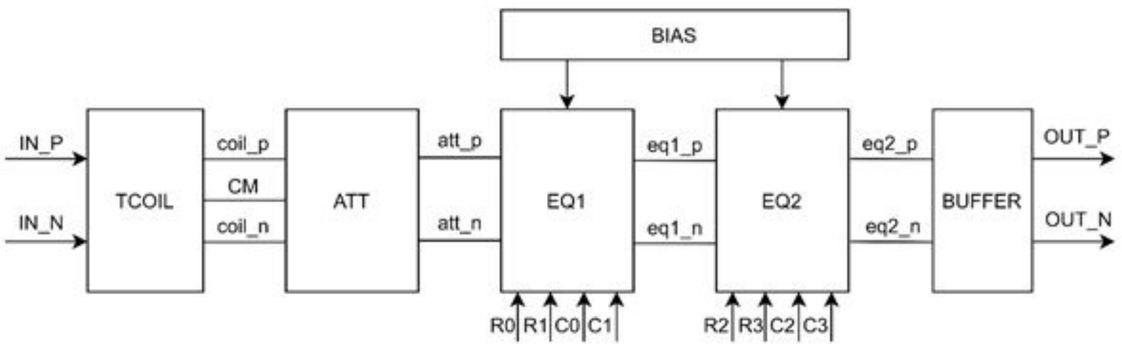

Figure 2. CML-receiver block diagram

TCOIL - inductive-capacitive bridge
ATT - attenuator / range adjust
EQ - equalizers (CTLE)

Electrostatic protection (ESD) of the circuit results in unbalanced capacitance and mismatches impedance in the channel. To reduce the influence of the ESD capacitance, a T-shaped TCOIL bridge is used. ESD protection is connected between the inductances of the bridge, separating the high-frequency component from the useful signal.

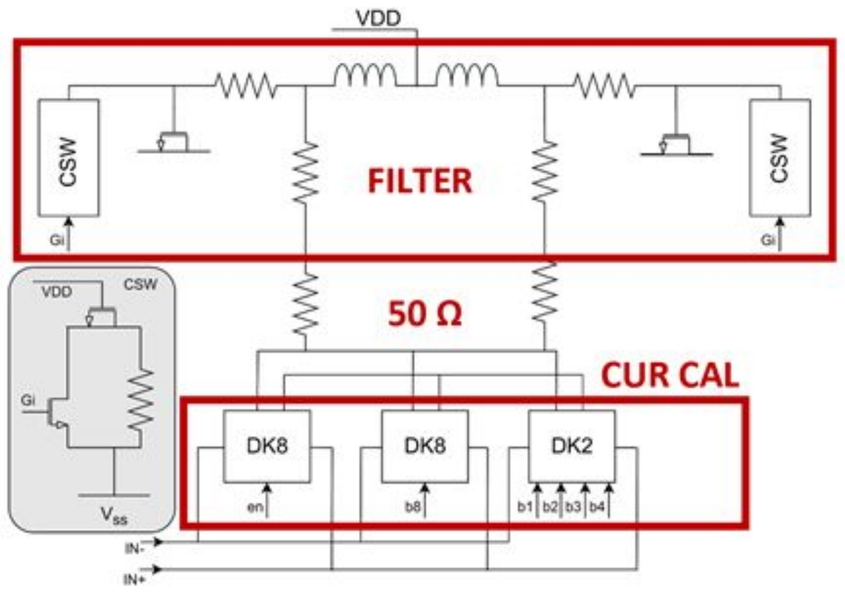

Figure 3. CML-transmitter output stage

Transmitter architecture employs *3 successive amplification stages with x2, x2 and x4 current gains*. To be able to match transmitter output impedance with external parasitics, *transmitter output impedance adjustment* was implemented. For efficient data transmission through the channel, the corresponding protocol was modified and *line balancing* was employed. Balancing allows to compensate for the voltage drop over the communication channel impedance at medium frequencies. These measures allowed for eye-opening of *300 mV at 2.56 Gbps.*

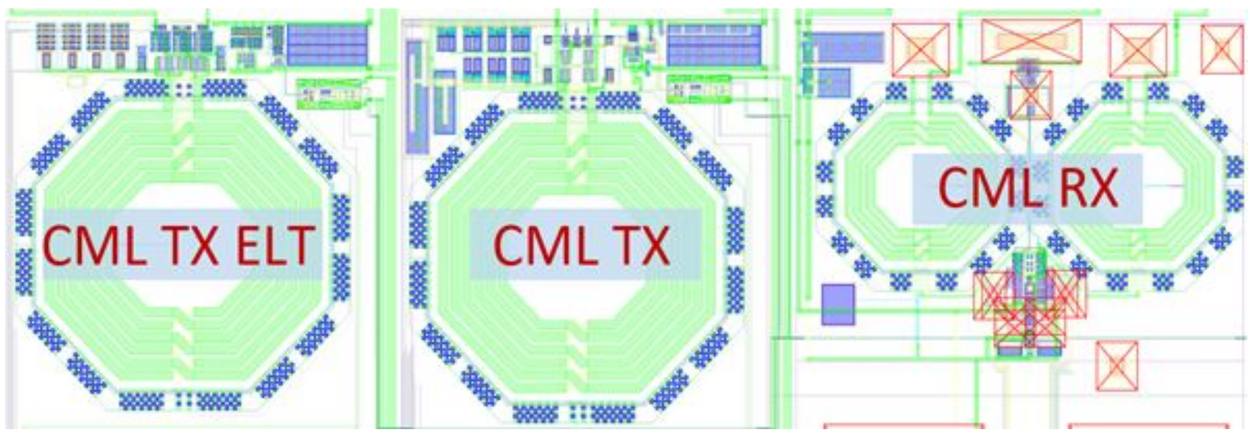

Figure 4. CML-unit layout

Radiation tolerance constraints were taken from the MPD experiment [2]. In particular, to reduce the leakage currents due to ionizing radiation and prevent the latching effect caused by high-energy charged particles hits, the *parameterized model of the N-channel ring transistor* [3] for TSMC 65 nm was developed, adopted in a CAD system and used in the project.

Outcomes

CML transceiver was designed and manufactured in TSMC 65 nm LP process as a part of HUBv1 ASIC.

CML transceiver characterization board was designed and evaluated.

Next, radiation tolerance tests will be conducted at PNPI, Gatchina.

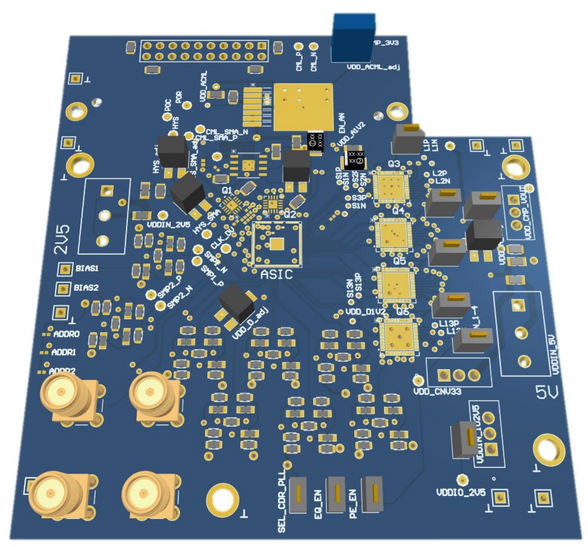

Figure 5. Characterization board

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The reported study was funded by RFBR according to the research project № 18-02-40093

Reference

[1] Atkin, E., Serazetdinov, A., et al.,Development of Data Concentration Method and Its Implementation in a Radiation-Tolerant CMOS Application Specific Integrated Circuit (2021) Physics of Particles and Nuclei, 52 (4), pp. 752-756.

[2] Vereschagin S., Movchan S., Zaporozhets S. Front-end electronics development for TPC/MPD detector of NICA project // J. of Instr., 2020, V.15, pp. C09044.Lee H.T. et al. // J. Nucl. Mater. 2011. V. 415. P. S696– S700.

[3] Semenova I. Simulation of Dose and Fluence Quantities inside/outside MPD using FLUKA Monte Carlo code // MPD Technical Board Meeting, November 12, 2019.

[4] A. R. Serazetdinov, E. V. Atkin, and K. O. Khokhlov , "Parametric layout cell design of N-MOS transistor with enhanced radiation hardened properties", AIP Conference Proceedings 2313, 040009 (2020)