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2.56 Gbps CML transceiver for the data concentrator ASIC

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2.56 Gbps CMOS CML-transceiver is presented. The key feature of the design is capability of working with a specific inductive load at both power consumption and radiation tolerance constraints. The transceiver was designed as an interface part of the data concentrator ASIC, intended for the frontend electronics of the time-projection chamber of the MPD experiment at NICA nuclotron (Dubna).

Summary (500 words)

In the course of the experiments carried out at modern spectroscopic facilities, big data flows are expected to be generated from multichannel detectors. Due to the specific radiation environment, data processing is mostly conducted in a remote room. At the same time a high detector granularity leads to the need of high-speed data transfer from the experimental setup to the remote room under constrained power consumption budget.
The paper presents the design results of CMOS building blocks of the CML receiver and transmitter, working at 2.56 Gbps data rate. Both blocks were included in the interface part of the prototype HUBv1 data concentrator ASIC, designed for the frontend electronics of the time-projection chamber of the MPD experiment at NICA nuclotron (Dubna).
The ASIC was prototyped in November 2020 through Europractice in the Low Power (LP) 65 nm CMOS process of TSMC. For the blocks characterization, a test PCB was designed. The chips, received in April 2021, were tested at lab conditions.

The capability of the 2.56 Gbps operation for both CML receiver and transmitter blocks were studied for wire-bonding the ASIC into the CPGA-120 case. The most critical parasitic parameters in such a case are inductances of bonding wires and package pins. These are estimated to be 3-5 nH in total. Mutual inductive coupling between the bonding wires are also of importance. For the two neighboring wires this is equal 0.5 nH. Thus the blocks are required to work with a specific (mostly inductive) load.
According to the accepted concept of the TPC front-end electronics, data transmission to the remote room is provided over a 1 meter light-weight micro-coaxial cable of the AWG36 type having a characteristic impedance of 50 Ohm. At such cable length the effect of high-energy particles on the readout electronics, moved out of the "hot zone", is reasonably reduced. At the same time due to the low cable attenuation the signal-to-noise ratio is maintained. That allows correct data post-processing. At the receiving end, the unbalanced constructive parasitic capacitance is allowed not more than 3 pF.
Thus, in the course of CML-transceiver design the following objectives are to be ensured: 1. signal integrity and matching of the signal paths, 2. complex inductive-capacitive load blocks operation (bonding wire inductance of the leads of CPGA-120 package and capacitive load in a remote room at a distance of 1 m), 3. increased radiation tolerance using advanced design techniques, 4. power consumption reduction.
To compromise these requirements, specific system and circuit solutions were used in the course of blocks design. In particular, methods of waveform restoration using high-frequency correcting circuits and filters were applied. Special attention was paid to the integrity of the power rails in the package with a high value of the bonding inductance. The influence of the PCB parasitics mismatch on the signal integrity was considered, and the circuit of an adjustable calibration filter was designed to ensure the matching of the transmission channel.

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