A radiation-tolerant clock generator for the CMS Endcap Timing Layer readout chip

ETROC PLL is the clock generator of the developing ETROC project, which provides precise clocks with different frequencies (40 MHz, 320 MHz, 1.28 GHz, and 2.56 GHz) to the other functional blocks in the ASIC. It is developed in a 65 nm CMOS process and based on the lpGBT design components. We reassembled the latest version of LJCDR (January 2020) from the lpGBT project at CERN into the ETROC PLL prototype chip for function and radiation tests.

The block diagram is shown in Figure 1. The ETROC PLL core includes the LJCDR, the prescaler, and the feedback divider from the lpGBT project, and an automatic frequency calibration (AFC) block, which is used for LC-VCO calibration. The LJCDR is fixed in PLL mode with CDR mode disabled. The prescaler consists of two parts: the clock generator (N=2) and the clock transfer circuits (from differential CML/single-ended CMOS). The reference voltage generator of 1 V, designed for charge injection and Voltage DAC in each pixel of ETROC, is also implemented in this chip. All power supply voltages, marked in different colors in the diagram, are separated to ease monitoring of power supply currents and avoid power interference.

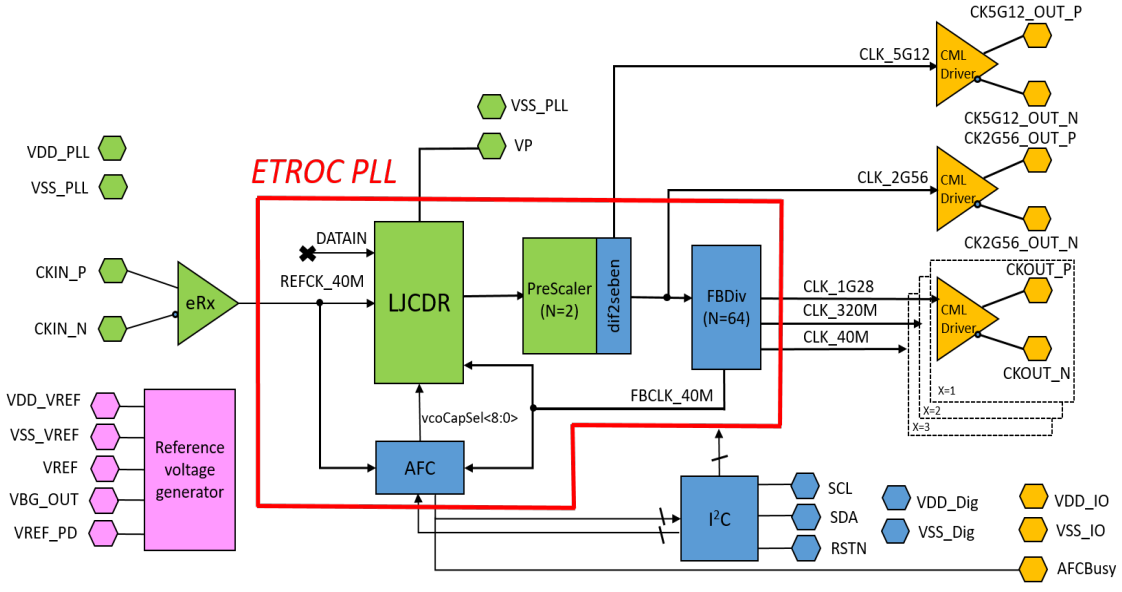

Figure 1: Block Diagram of ETROC PLL

The AFC block with the data protector is implemented for LC-VCO calibration. This digital block searches for the optimal VCO capacitor bank when the tuning voltage is overridden. The calibrated data ("Capsel") is stored and refreshed automatically in the data protector to avoid data crashes and loop unlocks due to SEUs. Figure 2 (a) illustrates how AFC operates with the LC-VCO and the slow control I^2C block. The fully automatic calibration workflow is shown in Figure 2 (b).

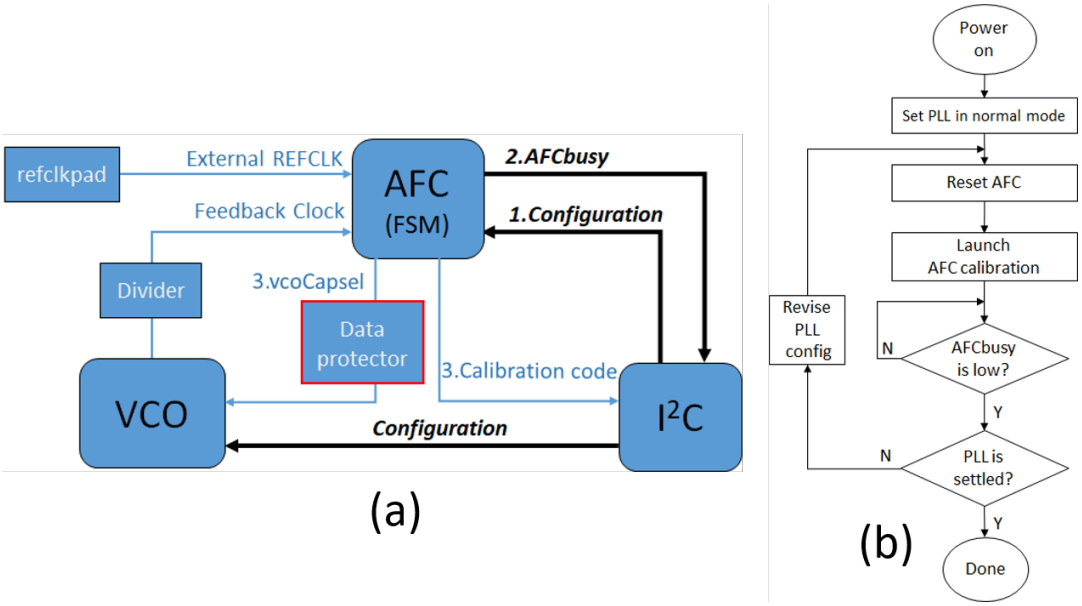

Figure 2: Block Diagram of AFC (a) and its fully automatic calibration workflow (b).

ETROC PLL, with the layout area of 1.2 mm × 0.7 mm, was implemented in a standalone test chip (2 mm × 1 mm). Additional circuitries include the input reference clock receiver, the output CML drivers, and a generic I^{2}C from lpGBT. Figure 3 (a) presents the test setup for the lab bench tests. A photograph of the test board for ETROC PLL is shown in Figure 4 (b), and Figure 4 (c) illustrates how the die was wire-bonding on the test board.

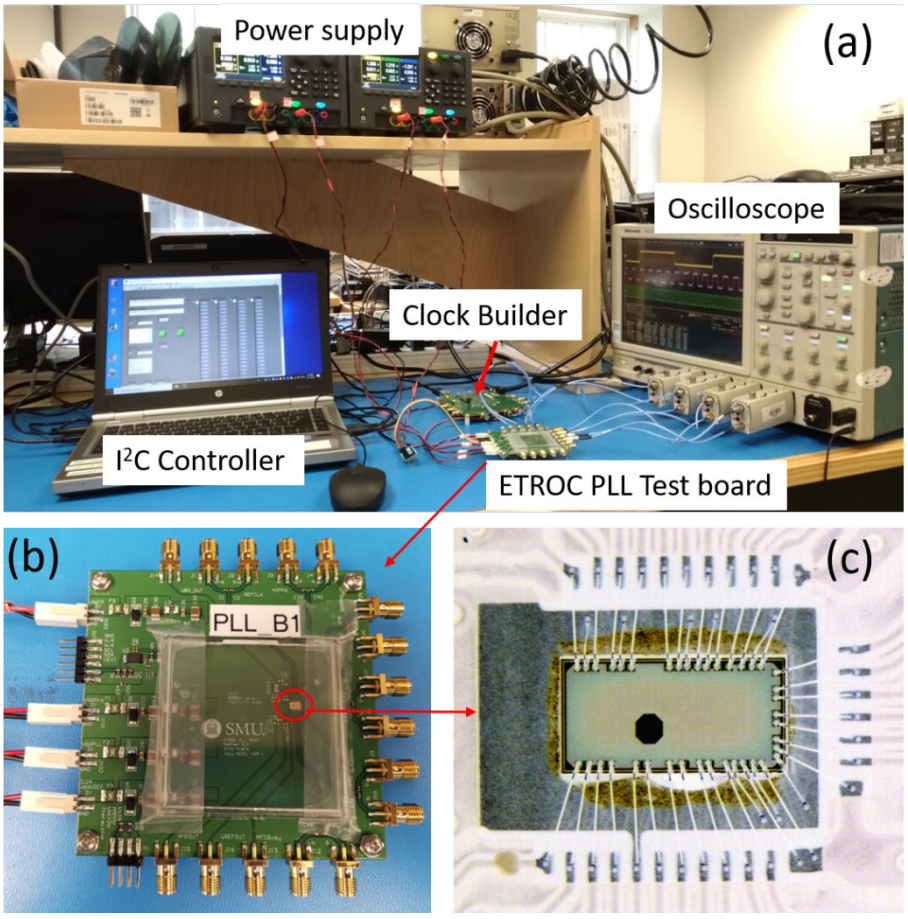

Figure 3: Lab test setup (a), test board (b), and wire-bonded chip (c) of ETROC PLL.

Figure 4 (a) presents the deterministic jitter component on clocks of 320 MHz, 1.28 GHz, 2.56 GHz, and 5.12 GHz above 40 MHz. The Time Interval Error (TIE) jitter is measured to be within ± 5 ps (peak-to-peak).

Figure 4 (b) presents measured phase offsets between the rising edges of the 40 MHz output clock and the 40 MHz trigger clock (not calibrated).

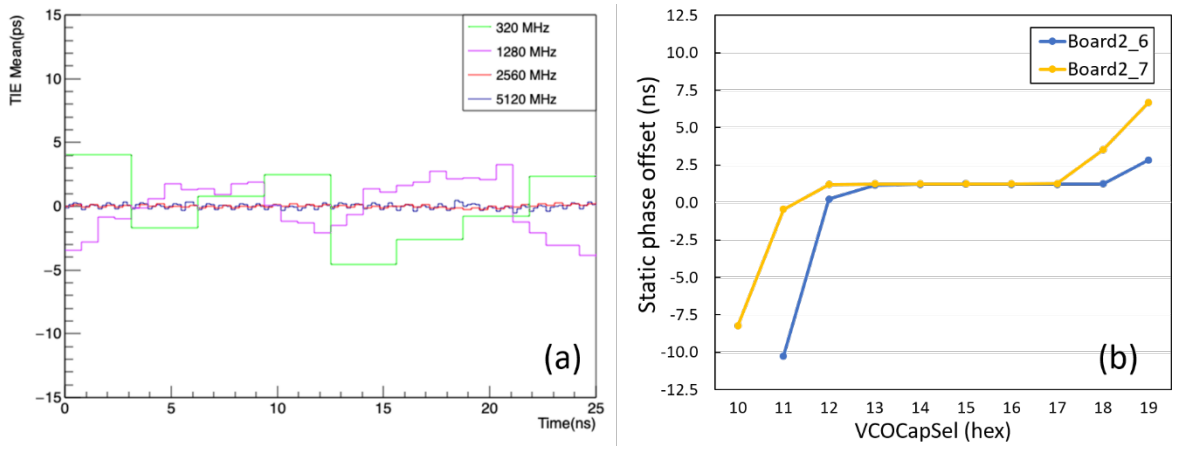

Figure 4: TIE jitter of output clocks with different frequencies (a) and static phase offset versus VCO capacitor bank setting (b).

Figure 5 presents the random sample of positive phase jumps during heavy ion irradiations. The short phase jumps with a magnitude between 50 and 600 ps persists for 1 ~ 3 µs. The saturation cross-section is about 10^{-6} cm^2. The SEE sensitivity outside the PLL loop was observed. We will check with simulations if the additional sensitivity could originate in the IO CML driver biasing.

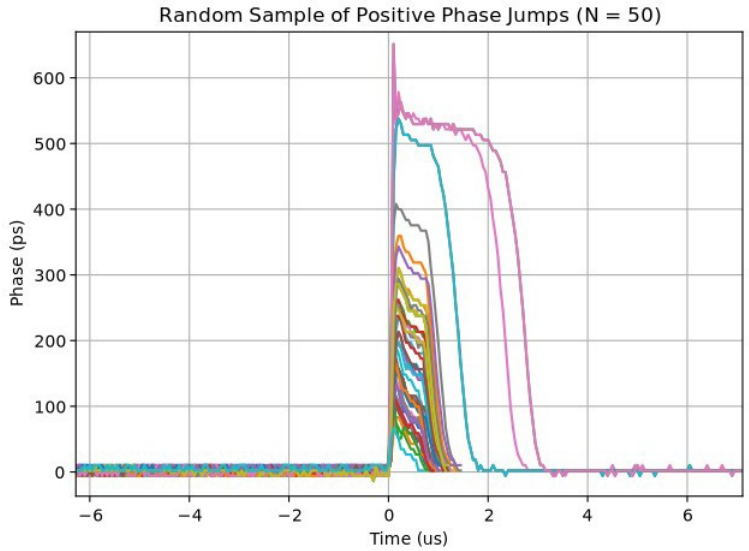

Figure 5: Random sample of positive phase jumps during heavy ion irradiations.