Contribution ID: **138** Type: **Poster**

A radiation-tolerant clock generator for the CMS Endcap Timing Layer readout chip

Tuesday 21 September 2021 17:53 (3 minutes)

We present the test results of the ETROC PLL prototype chip. This chip is based on the latest version of ljCDR from the lpGBT project and is designed to test ljCDR in its PLL mode as the clock generator for the CMS Endcap Timing Layer readout chip (ETROC). An automatic frequency calibration (AFC) block with the data protector is implemented for LC-VCO calibration. Triple Modular Redundancy (TMR) is used for all digital circuits to protect against SEUs. The chip's performance has been extensively tested, including SEU testing with heavy ions from 1.3 MeV.cm2/mg up to 62.5 MeV.cm2/mg.

Summary (500 words)

The MIP Timing Detector (MTD) is a new detector planned for CMS during the High-Luminosity Large Hadron Collider (HL-LHC) era. We have been developing the Endcap Timing Readout chips (ETROC) based on a 65 nm CMOS process as the front-end readout electronics of the Endcap Timing Layer, aiming to measure the arrival time impinging particles with a time resolution of 30˜40 ps. In this work, the test results of the ETROC PLL prototype chip are discussed. As the clock generator of the ETROC project, the output clock frequencies to the functional blocks in the ASIC are 40 MHz, 320 MHz, 1.28 GHz, and 2.56 GHz, with the demand of the RMS jitter within 5 ps. ETROC PLL must survive 100 Mrad Total Ionizing Dose (TID) and be insensitive to SEE effects.

ETROC PLL adapted the latest version of ljCDR (January 2020), a mature clock synthesis circuit inside the lpGBT project. The ljCDR is fixed in PLL mode with a 40 MHz reference clock and an integrated LC-oscillator at 5. 12 GHz. The CDR mode is disabled. The prescaler comprises the clock generator (division is 2) and the clock transfer circuits (from differential CML to single-ended CMOS). The feedback divider (division is up to 64) generates clocks with proportional frequencies and employs Triple Modular Redundancy (TMR) to project against SEUs. An automatic frequency calibration (AFC) block with the data protector is implemented for LC-VCO calibration. This digital block searches for the optimal VCO capacitor bank when the tuning voltage is overridden. The calibrated data ("Capsel") is stored and refreshed automatically in the data protector to avoid data crashes and loop unlocks due to SEUs.

ETROC PLL, with the layout area of 1.2 mm × 0.7 mm, was implemented in a standalone test chip (2 mm × 1 mm). Additional circuitries include the input reference clock receiver, the output CML drivers, and a generic I2C from lpGBT. Lab tests indicated that with a 40 MHz reference clock, the PLL loop locks instantly at 5.12 GHz after AFC calibration. ETROC PLL provides the random jitter within 2 ps (RMS) for all output clocks. The Time Interval Error (TIE) jitter is measured to be within ± 5 ps (peak-to-peak). During operation, the power consumption of the PLL core is about 60 mW.

ETROC PLL test chip was tested at the Heavy Ion facility in Louvain, Belgium. Heavy Ion irradiation was performed with LETs between 1.3 and 62.5 MeV.cm2/mg. The PLL circuit itself performed stably during irradiation: no unlocks have been identified. Comparing to the old version in lpGBT, the update of the ljCDR improves SEE immunity as expected in the test. The protection function of the AFC protector was verified successfully. The AFC "Capsel"code was protected correctly; thus, no large phase or frequency jump of the PLL loop was observed. Detailed results will be presented at the conference.

Authors: SUN, Hanhan (Southern Methodist University); SUN, Quan (Fermi National Accelerator Lab.); BIEREIGEL, Stefan (CERN); GONG, Datao (Southern Methodist University (US)); DE OLIVEIRA FRANCISCO, Rui; Prof. HUANG, Guangming (Central China Normal University); HUANG, Xing (Southern Methodist University (SMU)); KULIS, Szymon (CERN); LEROUX, Paul (KU Leuven); LIU, Chonghan (Southern Methodist University); LIU, Tiankuan (Southern Methodist University (US)); LIU, Tiehui Ted (Fermi National Accelerator Lab. (US)); RODRIGUES SIMOES MOREIRA, Paulo (CERN); PRINZIE, Jeffrey; WU, Jinyuan (Fermi National Accelerator Lab. (US)); YE, Jingbo (Southern Methodist University, Department of Physics); ZHANG, Li; ZHANG, Wei (Southern Methodist University)

Presenter: GONG, Datao (Southern Methodist University (US))

Session Classification: Posters ASIC

Track Classification: ASIC