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A Dual-mode NRZ/PAM4 Transmitter IP Purposed for Advanced CMOS Technology Nodes

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While the potential of PAM4 is becoming more practical, many designs still choose the NRZ approach. This paper presents a customisable dual-mode PAM4/NRZ transmitter IP (with 4/2-tap channel equalisation) deployable in multiple CMOS technologies. IP has been fabricated in 65nm (28Gbps/14Gbps), 180nm (10Gbps/5Gbps) technologies. A radiation-hardened 65nm (20Gbps/10Gbps) flavour is in active development. The serialization process is achieved using 16 self-generated synchronised clocks and produces 2 data streams with 4 equalisation streams to minimise inter-symbol inference. IP can be customised to transmit 1 PAM-4 (non-standard encoding) or 2 NRZ (Aurora 64b66b) data streams (with additional IO) prior to fabrication.

Summary (500 words)

Following on our previous successful design of a 10Gbps Aurora 64b66b NRZ transmitter in 65nm technology, presented at TWEPP 2018, significant design improvements have been made to increase maximum operating frequency, power efficiency and area consumption. Furthermore, the design now generates 2 streams of data and 4 additional streams for channel equalisation to minimise inter-symbol interference. The improved dual-mode transmitter IP makes use of an inductor-capacitor oscillator PLL to produce a high-quality clock, short-channel CMOS circuitry for energy efficient low frequency operations, and current-mode logic for both high performance high frequency operations and to drive the outputs. The IP has been fabricated in 65nm and 180nm CMOS technologies, and a 65nm radiation-hardened flavour is planned for fabrication in December 2021. The target speeds for these devices are 28Gbps PAM4/14Gbps NRZ, 10Gbps PAM4/5Gbps NRZ and 20Gbps PAM4/10Gbps NRZ respectively. The data encoding used by the IP is Aurora 64b66b for NRZ and for PAM4, a non-standard encoding protocol based on 256b257b with grey coding is used. The serialization process, which produces 2 streams of high-speed data, relies on 16 synchronised clocks for interleaved clock multiplexing. The 16 synchronised clocks are generated from a single high-speed clock driving interweaved clock circuitry; this is achieved by high performance flip-flops and multiplexers rather than complex synchronisation circuitry. The architecture has been engineered in such a way that simple modifications can determine whether a twin pair of NRZ serializers or a single PAM4 serializer is produced. This is achieved by swapping the digital encoding module in a hierarchical digital system, and the analogue line-driver circuit that drives the output, with the rest of the circuitry remaining the same. The PAM4 option can be configured (post-fabrication) to operate in NRZ and produce a single stream of data. The fabricated designs produced on Multi-Project Wafer runs and subsequently wire-bonded to test-boards for evaluation. The NRZ lanes will be evaluated by FPGA synthesized PRBS data checkers whereas the PAM4 lanes will be evaluated through eye-diagrams and waveforms from a high sample-rate oscilloscope. The transmission links will be evaluated with varied track lengths and the additional optional use of a TI Retimer IC (NRZ), or a SAMTEC FireFly optical transceiver (NRZ); Performance gain will be evaluated. We will present the results from the electrical characterization, and expand further on the development of the rad-hard 65nm design and the future plans for a planned 28nm design.

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